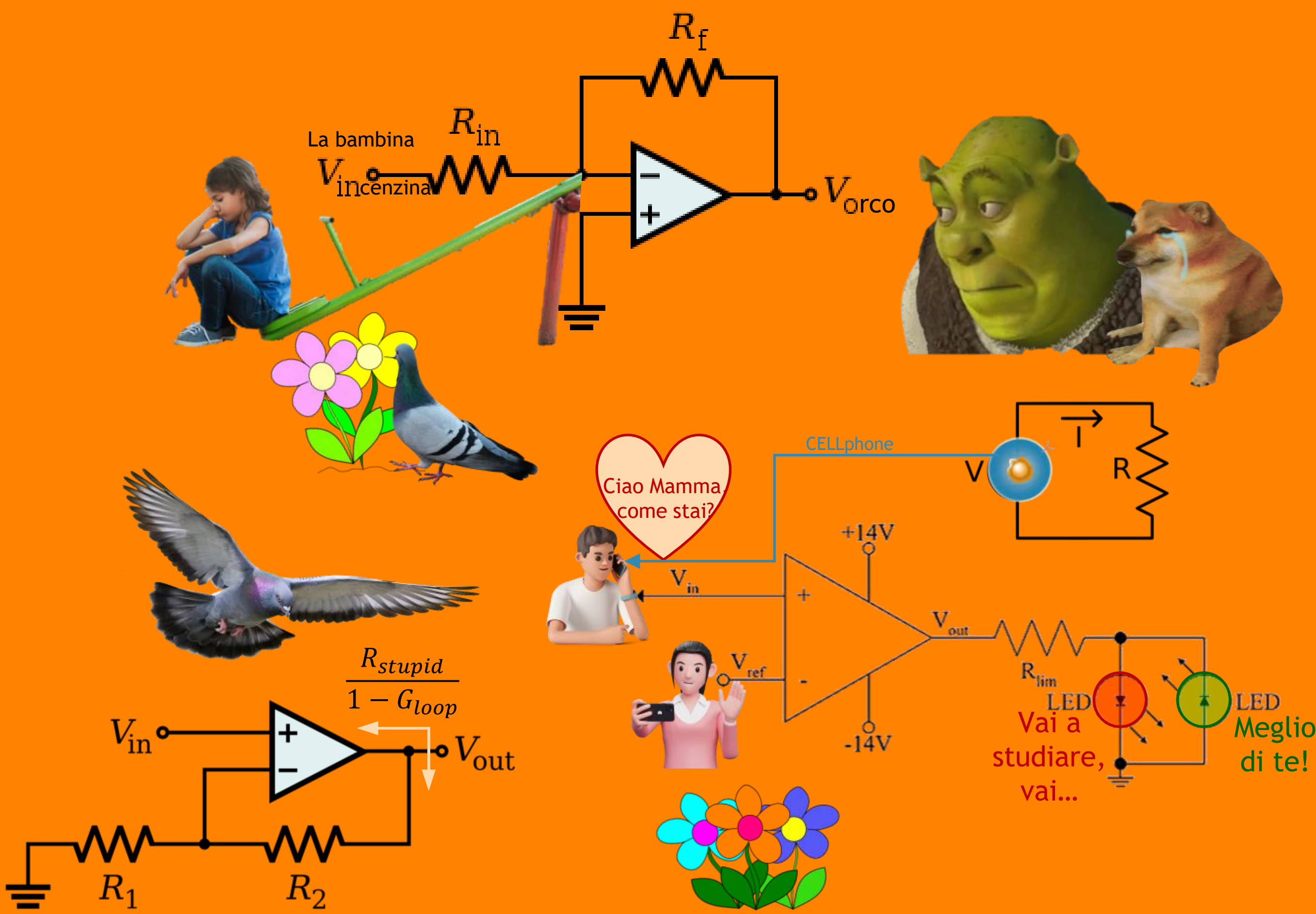
2022/2023



Electronic Systems Exercise Sessions Notes

Noise, advanced Operational Amplifiers and circuits,
Sample&Hold circuits, advanced DAC and ADC converters

Franco Zappa

SOCIETÀ EDITRICE CULAPIO

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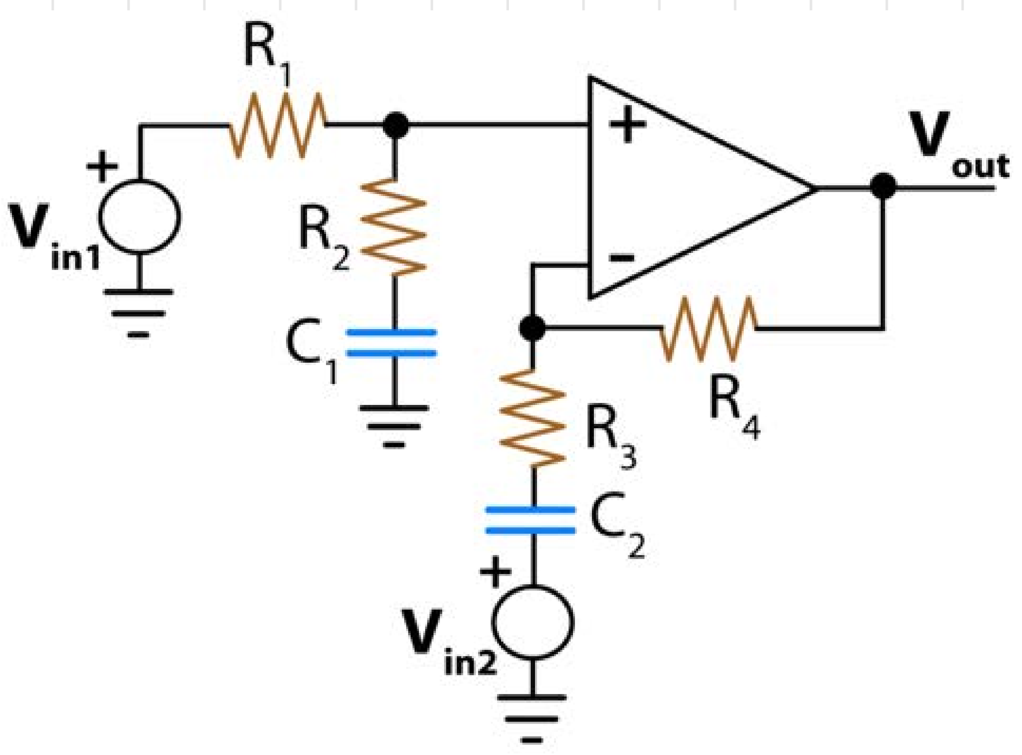
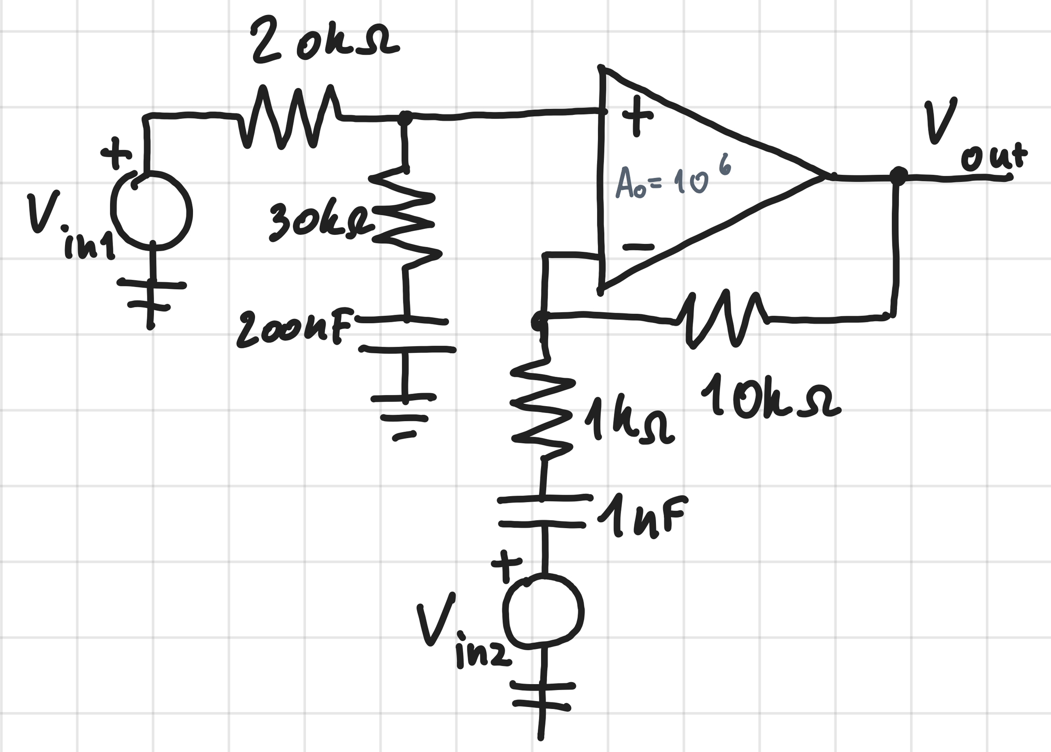


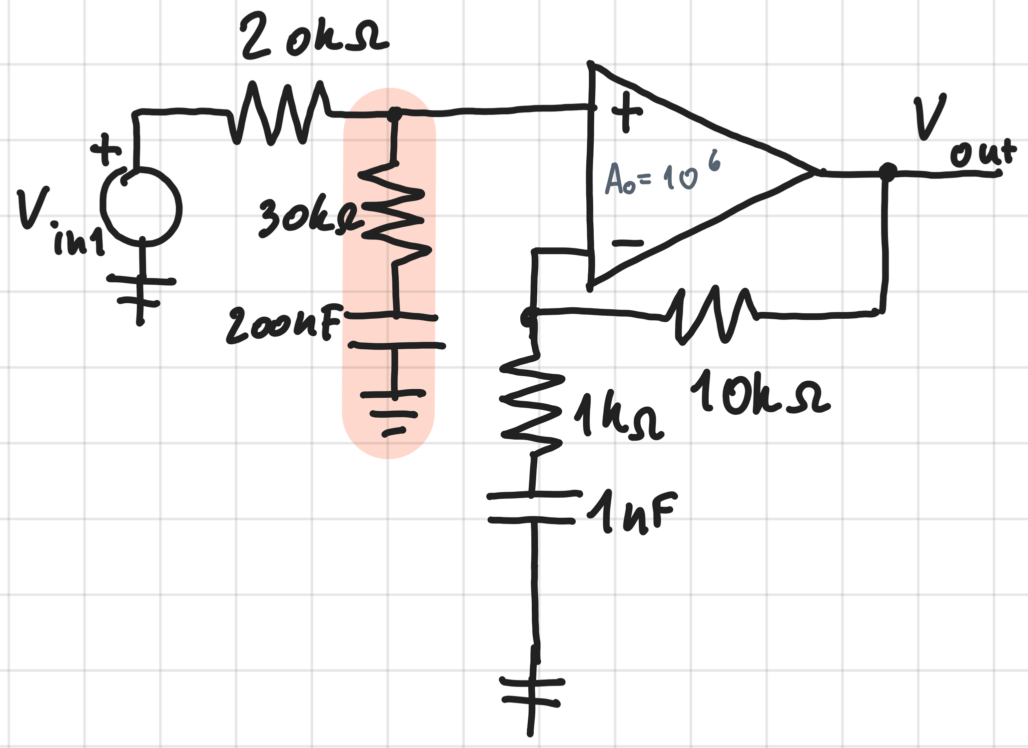


R_1=20kΩ R_4=10kΩ R_2=30kΩ C_1=200nF R_3=1kΩ C_2=1nF
$A_0=10^6$ I_B=10nA f_0=10Hz

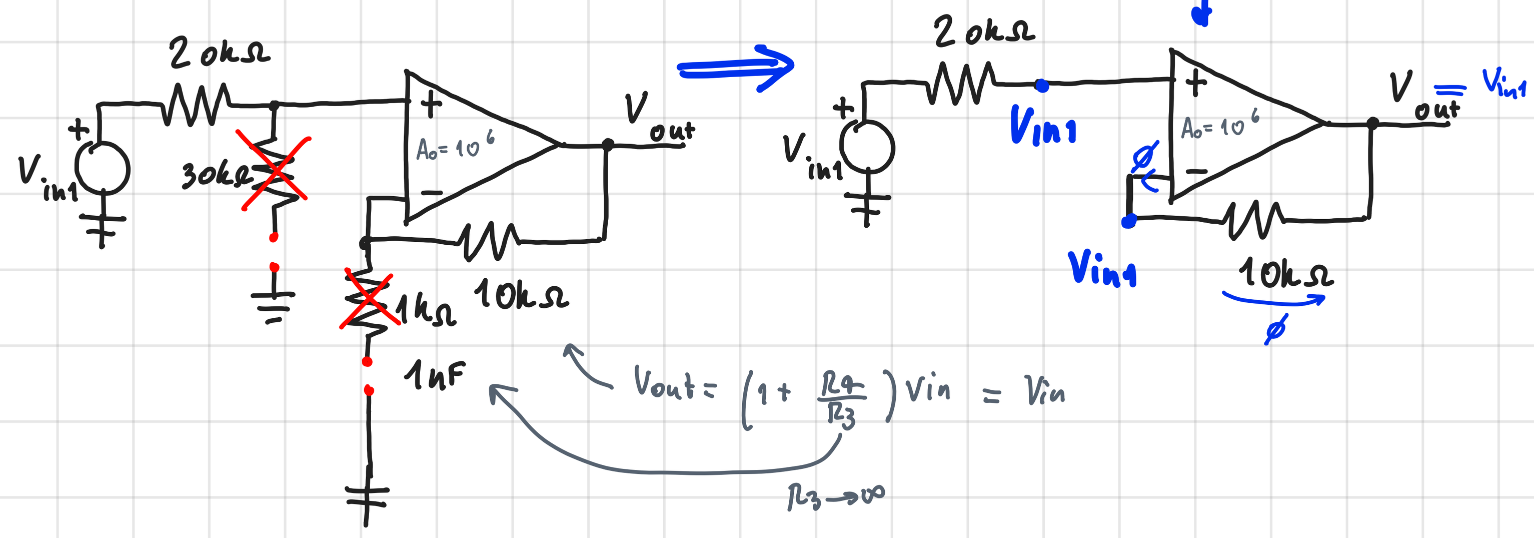
a) Plot the ideal gain $V_{OUT}(f)/V_{IN1}(f)$

b) Plot the ideal gain $V_{OUT}(f)/V_{IN2}(f)$

a)



- at DC [0 Hz]: C_1, C_2 OPEN



$V_{out} = \left(1+\frac{R_4}{R_3}\right)V_{in} = V_{in}$, $R_3 \to \infty$

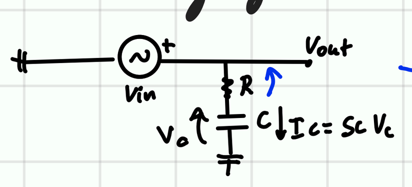
$\Rightarrow G_{DC} = \frac{V_{out1}}{V_{in}} = 1$

- Zeros and poles

– for C1

- ZERO 1: → RC-series hanging at a node case

↳ 3 RC-Series hanging at a node ⇒ a finite ZERO

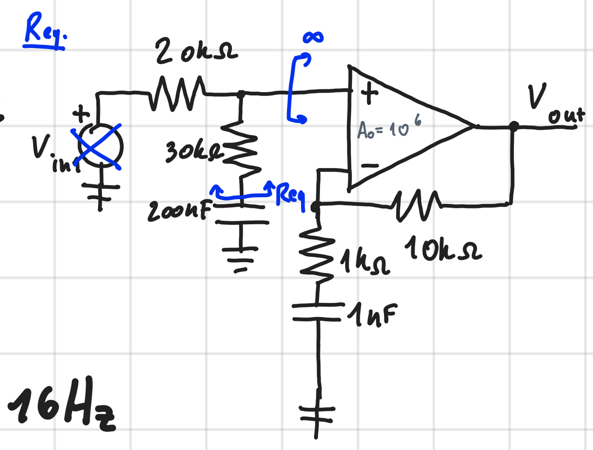


→ Voltage on R equal to V_c:

$RsCV_c = -V_c \rightarrow s = -\frac{1}{RC} \rightarrow f_z = \frac{1}{2\pi RC}$

$\rightarrow zero_1 = \frac{1}{2\pi \cdot 30k \cdot 200n} = 26Hz$

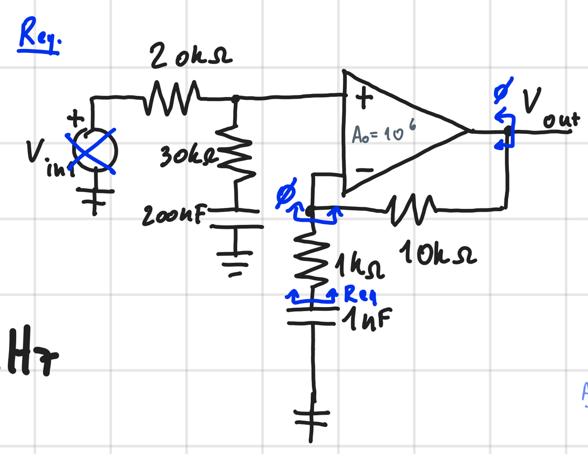
- POLE 1: → R_{eq1} = 20kΩ+30kΩ=50kΩ



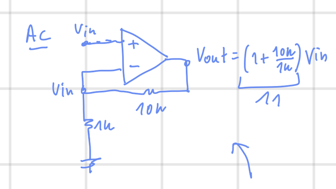
$\rightarrow pole_1 = \frac{1}{2\pi\, 200n \cdot 50k} = 16Hz$

– for C2

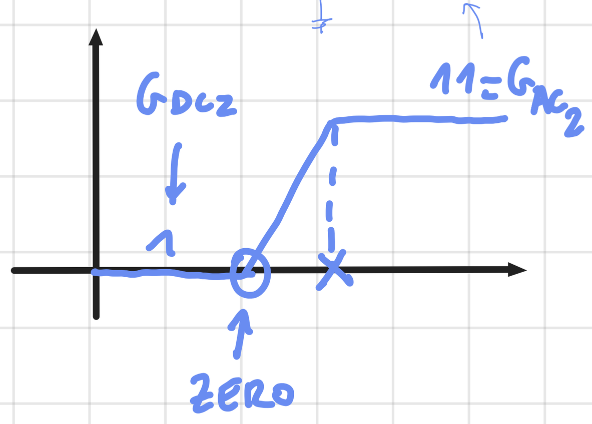
- POLE 2: → R_{eq2} = 1kΩ



$\rightarrow pole_2 = \frac{1}{2\pi \cdot 1n \cdot 1k} = 160\ kHz$



- ZERO 2: → computed through Bode analysis of the stage with C2

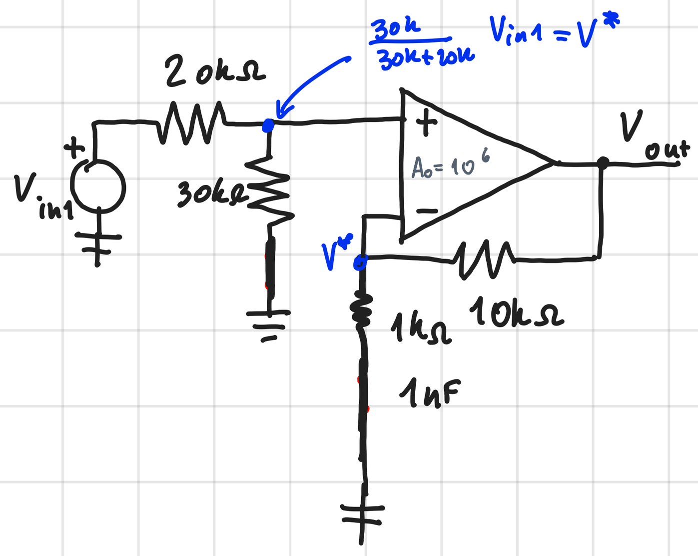


$\rightarrow zero_2 = \frac{pole_2}{\frac{G_{AC2}}{G_{DC2}}} = \frac{pole_2}{11} = 14.5\ kHz$

↳ Note: We can compute the zero of a capacitor that is series to a non-inverting OpAmp config can be computed as:

$zero_2 = \frac{1}{2\pi\, C_2(1k+10k)}$

- at AC [∞ Hz]: C_1, C_2 short circuit

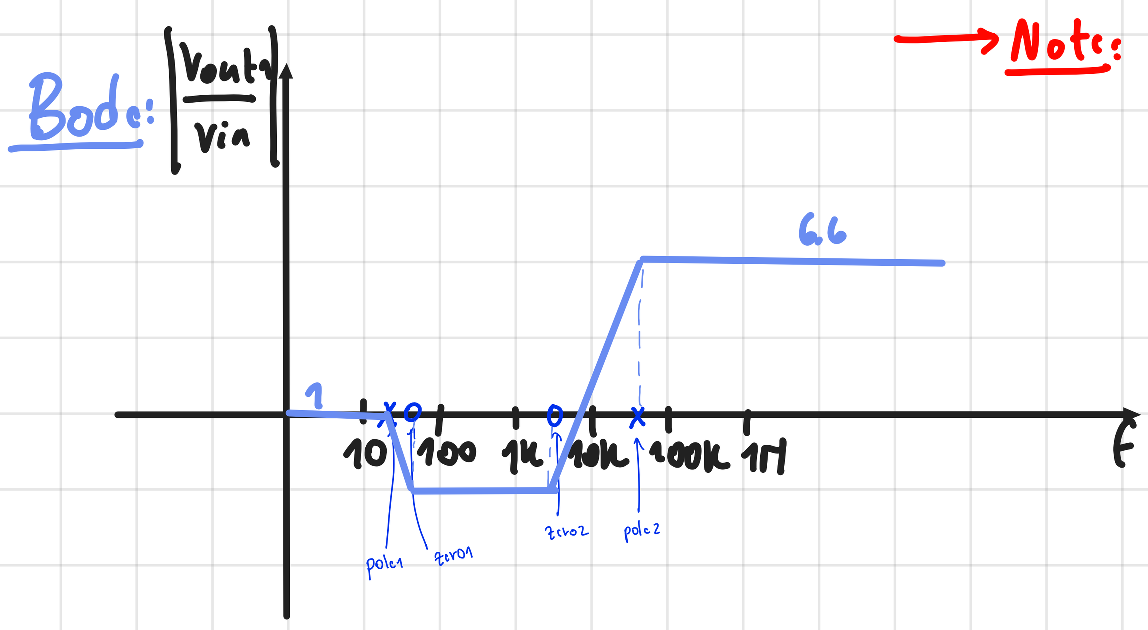


$\frac{30k}{30k+20k} V_{in1} = V^*$

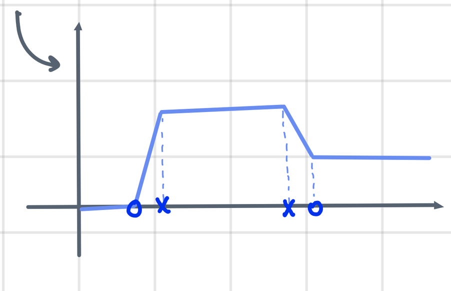
$V_{out} = V^*\left(1+\frac{10k}{1k}\right) = \frac{30k}{30k+20k}\left(1+\frac{10k}{1k}\right)V_{in}$

$\Rightarrow G_{AC} = \frac{30k}{30k+20k}\left(1+\frac{10k}{1k}\right) = 6.6$

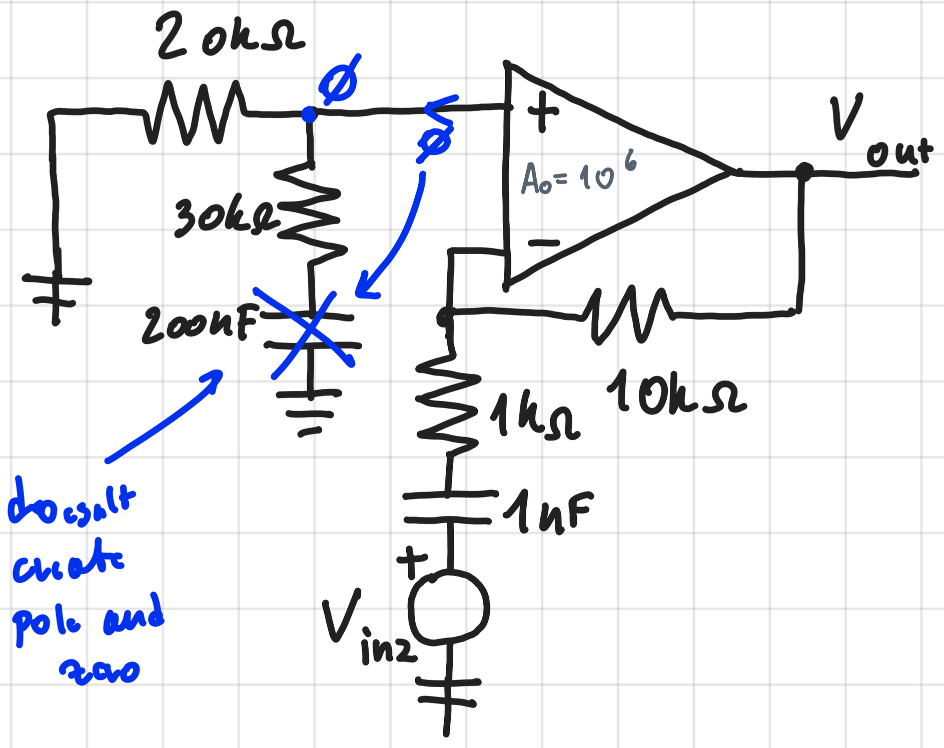
Bode: $\left|\frac{V_{out}}{V_{in}}\right|$



→ Note: this Bode is due to wrong-sizing. It would have been better this type of characteristic

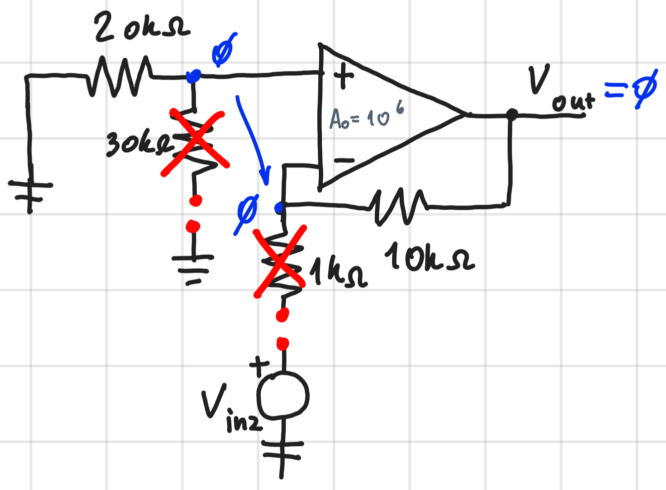


b)



doesn't create pole and zero

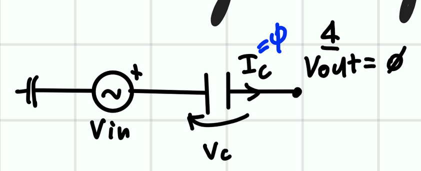
- at DC [0 Hz]: C_1, C_2 OPEN



↳ $G_{DC} = \varnothing$

- Zeros and poles:
  - ZERO2: → Capacitor along the signal path case

Capacitor along the signal path ⇒ ZERO at the origin

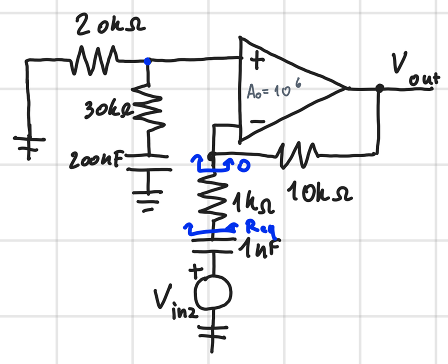


→ I_c must be $\varnothing$: $s=0 \rightarrow f=0$

$i_c(t) = C\frac{dv}{dt} \xrightarrow{\mathcal{L}} I_c(s) = sC\,V_c(s) = \varnothing$

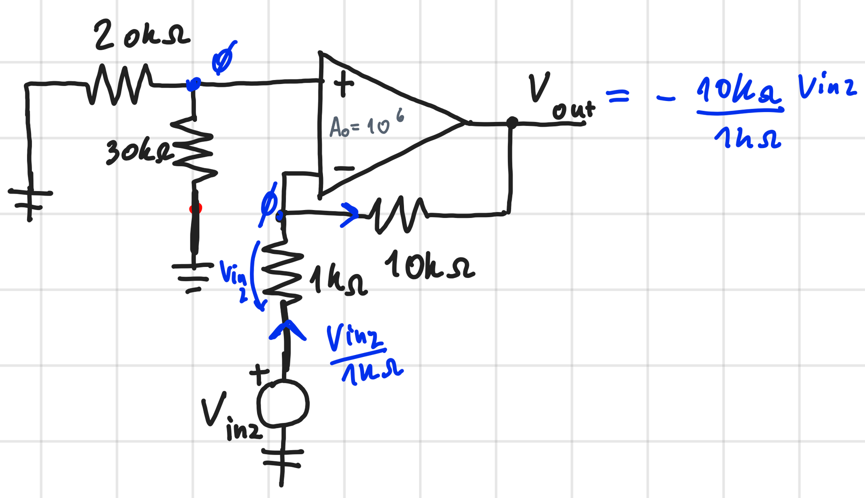
→ zero2 = $\varnothing$

  - POLE2: → $R_{eq} = 1\ k\Omega$



→ $pole2 = \frac{1}{2\pi\, 1k\, 1n} \simeq 160\ kHz$

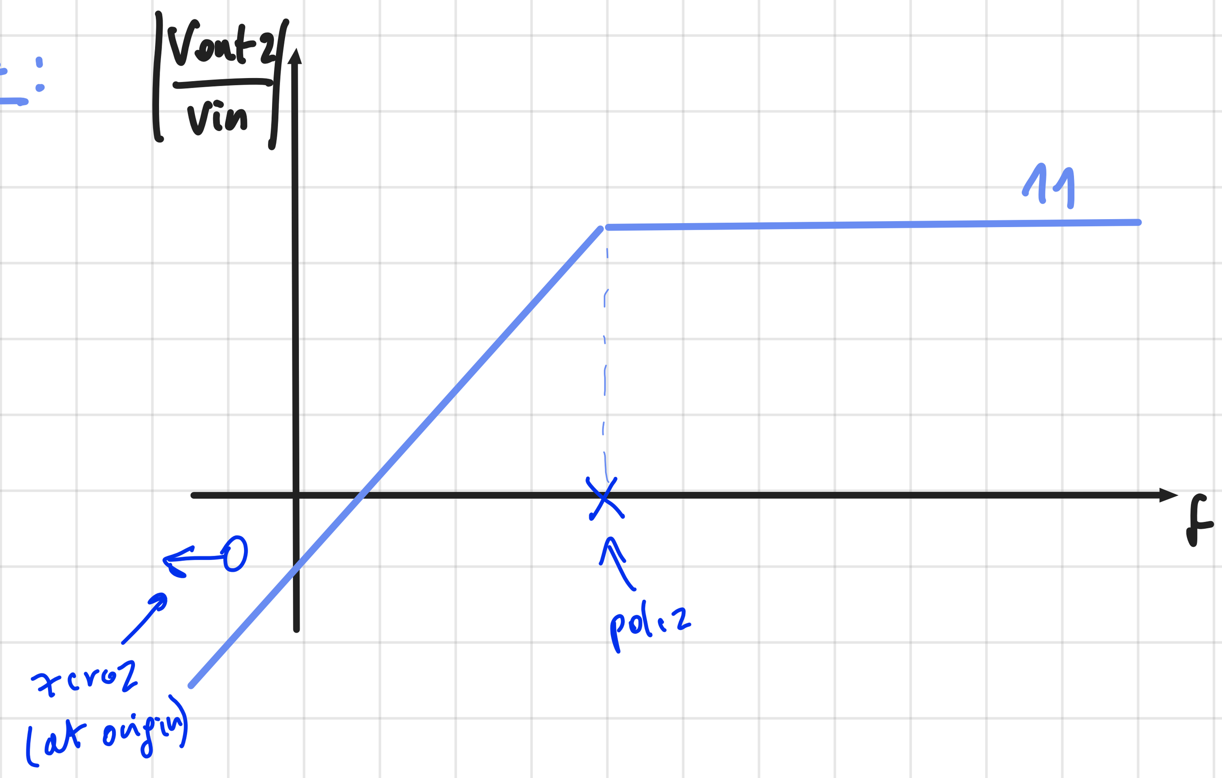
- at AC [∞ Hz]: C1, C2 short circuit



⟹ $G_{AC} = -11$

$|G_{AC}| = 11$

Bode:



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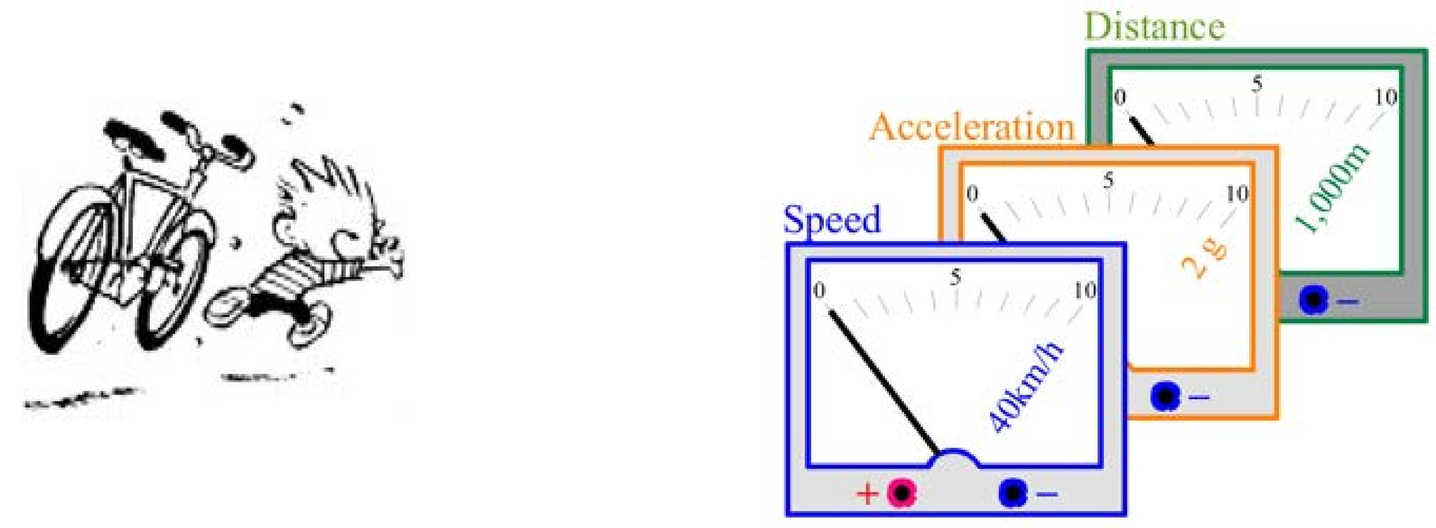


Calvin measures his bike's speed S, by employing Hobbes' speedometer ($v_s = S \cdot 50^{mV}/_{m/s} + 200mV$) and 10V FSR voltmeters

a) Design a circuit for displaying the speed, up to 40km/h, with 3s smoothing

b) Display acceleration/deceleration, up to 2 g ($g=9.81m/s^2$)

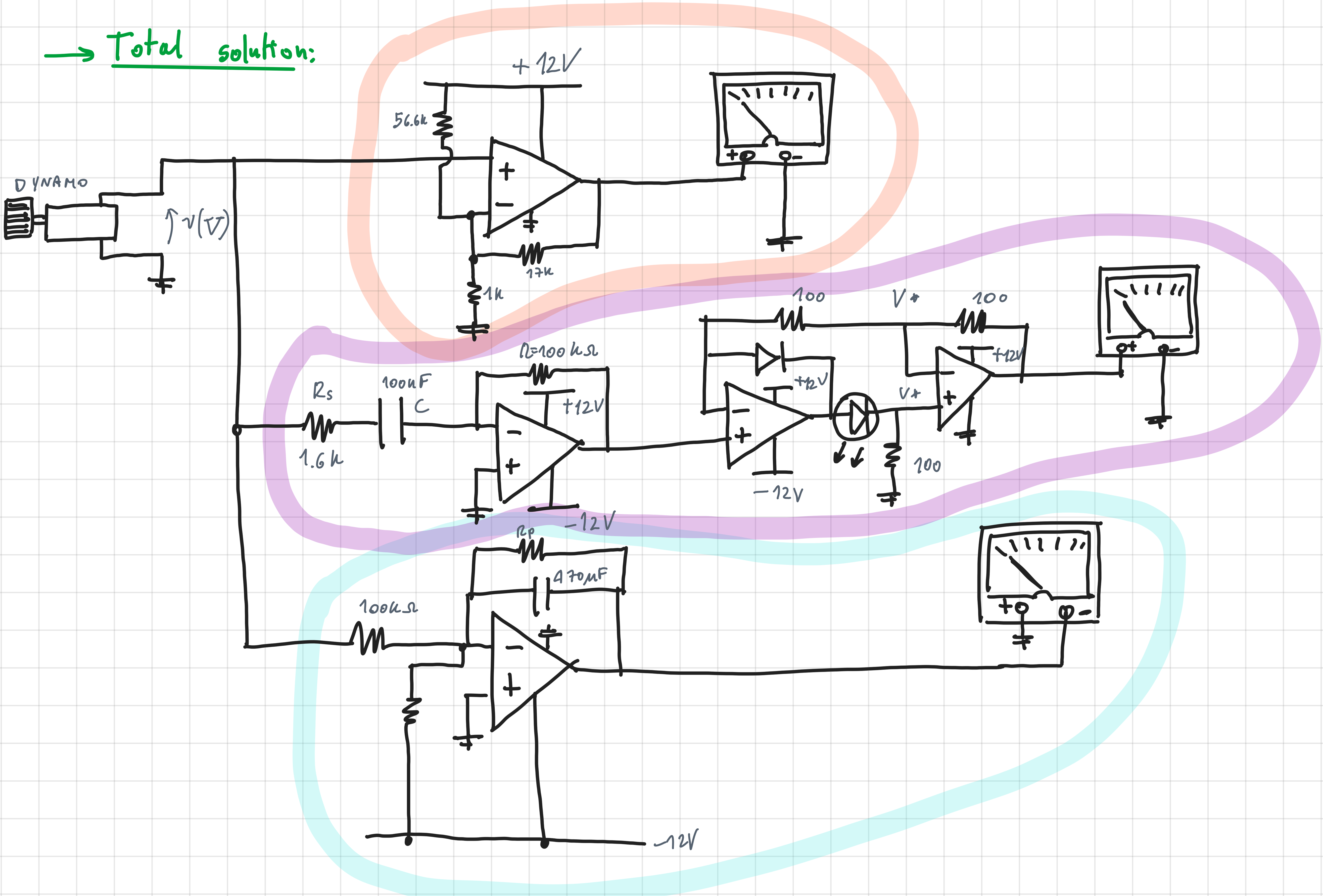
c) Measure and display the ride distance, up to 1km

We want to express speed, acceleration, distance scale with a voltmeter with max value 10 V.

We use a dynamo sensor that converts speed in volts (Hobbes speedometer) following this relation:

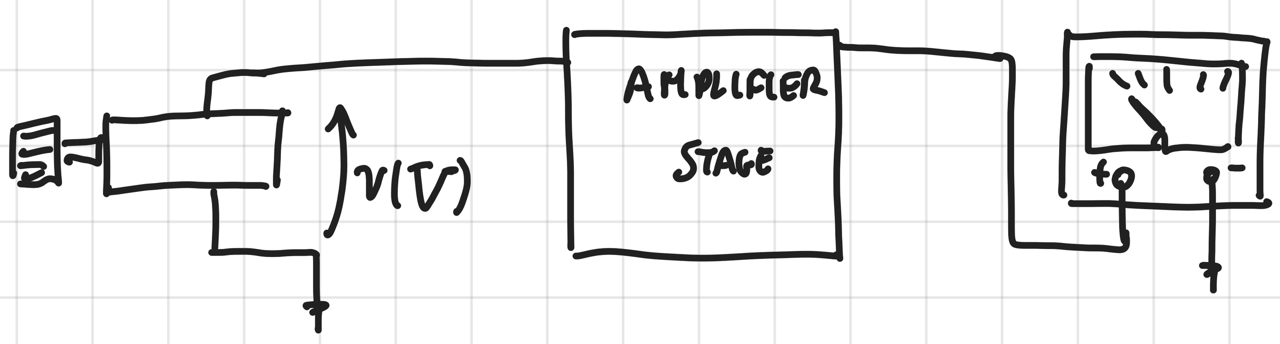
$$\underset{\text{volt}}{v}\,(\underset{\text{velocity}}{V}) = 50\,\frac{mV}{\frac{m}{s}} \cdot V + 200\,mV$$

→ **Total solution:**

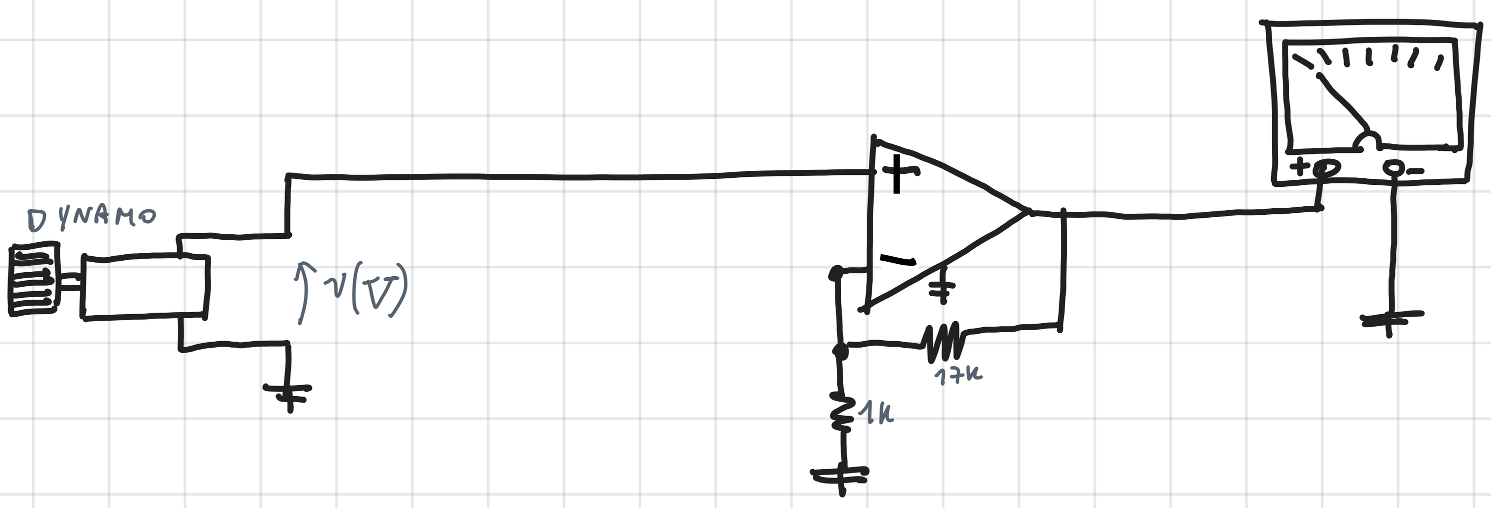


→ **Solution analysis and derivation:**

a) First consider the simple schema:



↳ e.p. Amplifier design in inverting config.:



• Gain computation: We convert the known max speed ($40\,\frac{km}{h}$) in Volts through this equation, and then see the gain proportion wrt the know max voltage (10 V)

$$v\left(40\,\frac{km}{h}\right) = 50\,\frac{mV}{\frac{m}{s}} \cdot \underbrace{\frac{40 \cdot 1000\,m}{3600\,s}}_{40\,\frac{km}{h}} + 200\,mV = 555\,mV$$

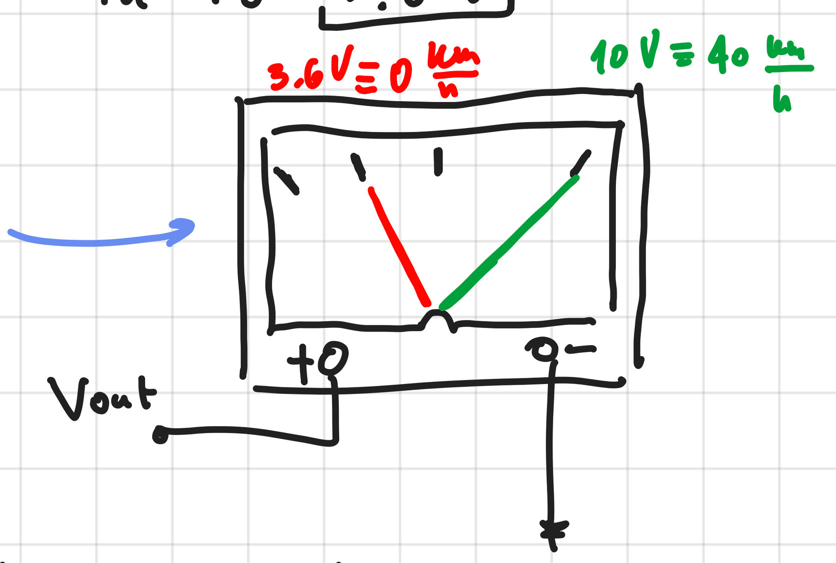
$$\Longrightarrow G = \frac{10\,V}{555\,mV} \simeq 18$$

→ But in this case when we are at ∅ speed we'll still have an offset on the scale due to the voltage offset of 200mV

↳ We need to subtract that offset:

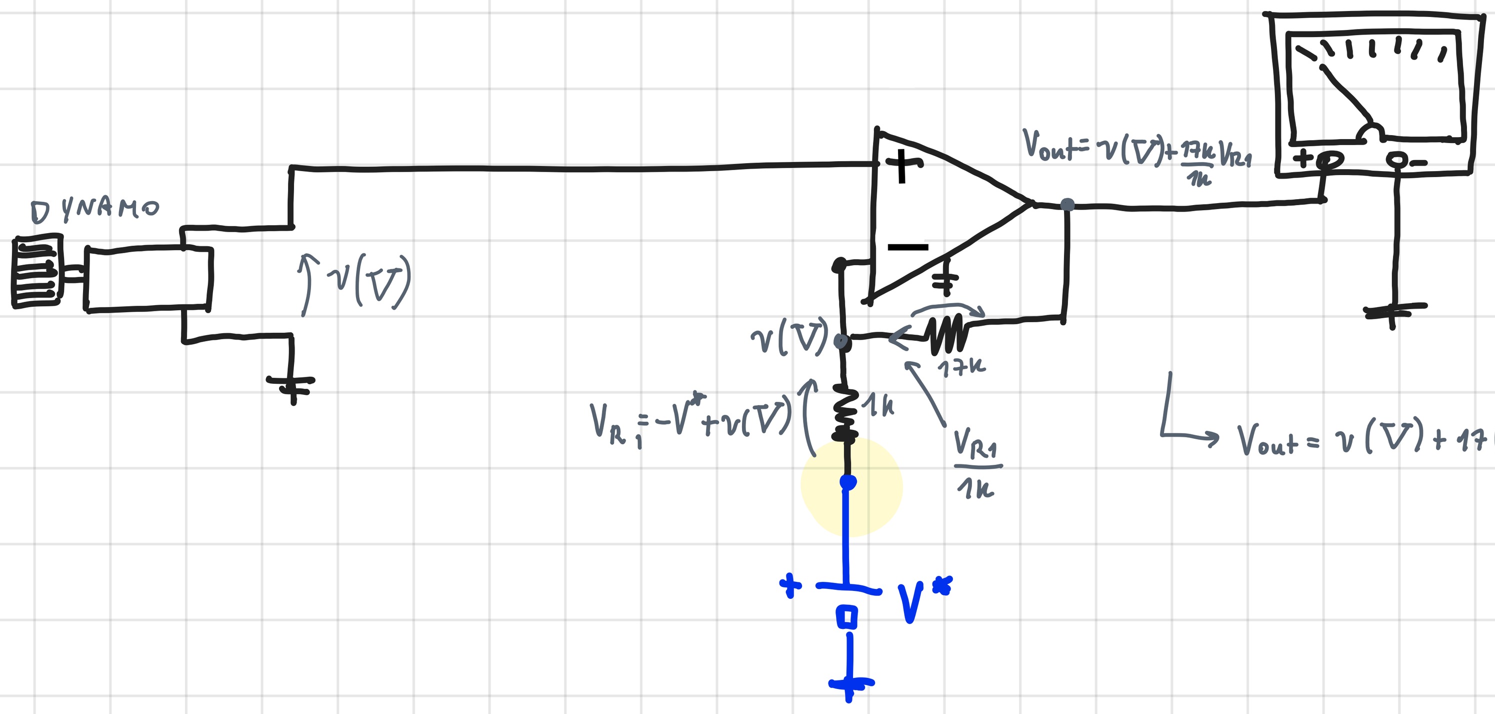
For Ø speed $v_{in} = v(0\,\frac{km}{h}) = 200mV$ ⟶ at the output of amplifier $V_{out} = v_{in} \cdot 18 = \underline{3.6\,V}$

waste of the scale resources ⟶ Ø speed not at the beginning ⟶



1st method

We can put this node not to ground, but to some voltage in such way that multiplied for the gain of 17 equals the 3.6 V to subtract



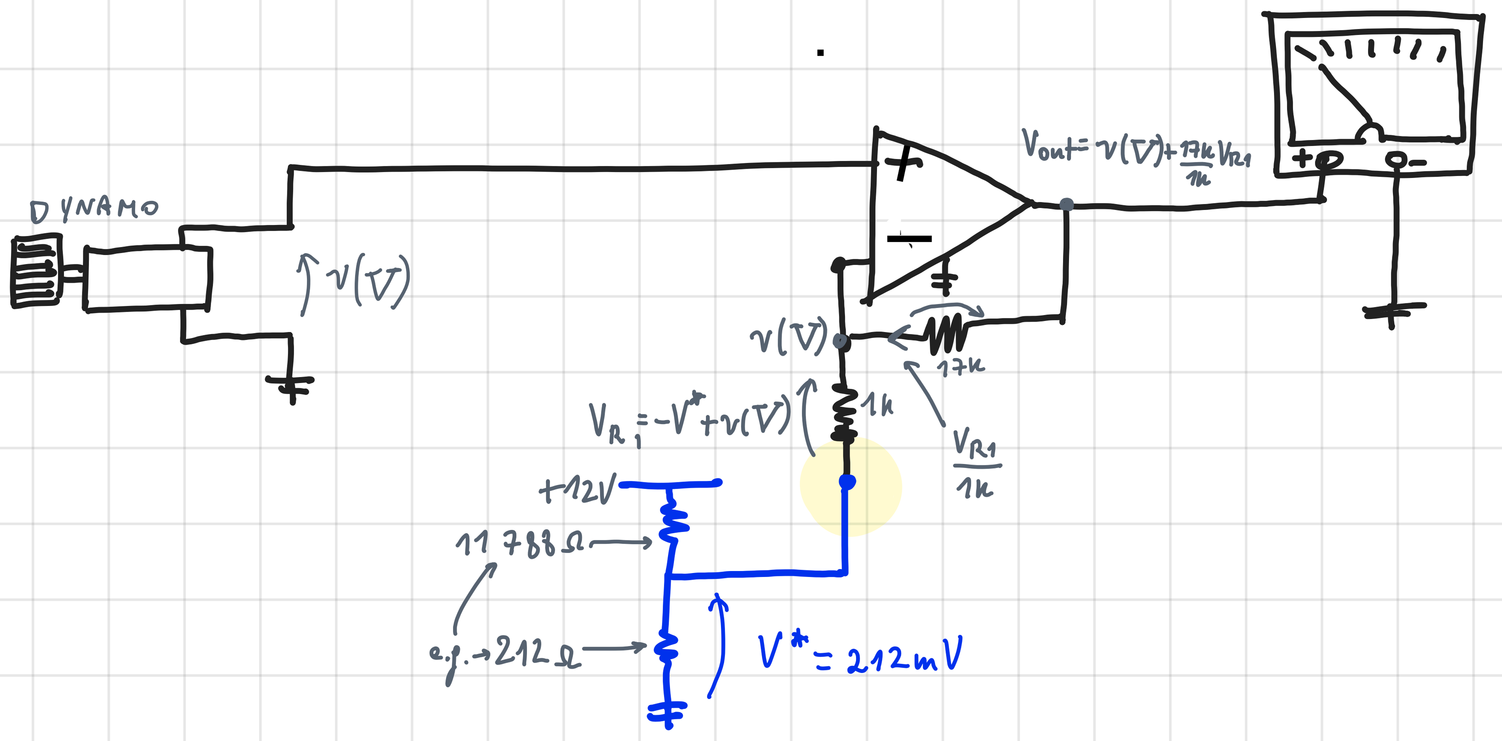
↳ $V_{out} = v(V) + 17(v(V) - V^*) = \underline{18\,v(V)} - 17\,V^*$

⟶ $V^* \cdot 17 = 3.6V$ ⟶ $V^* = 212\,mV$

↳ Indeed: $V_{out}(0\,\frac{km}{h}) = \underline{3.6\,V} - \underbrace{17 \cdot 212\,mV}_{= 3.6V} = 0\,V$

↑ beginning of the scale!

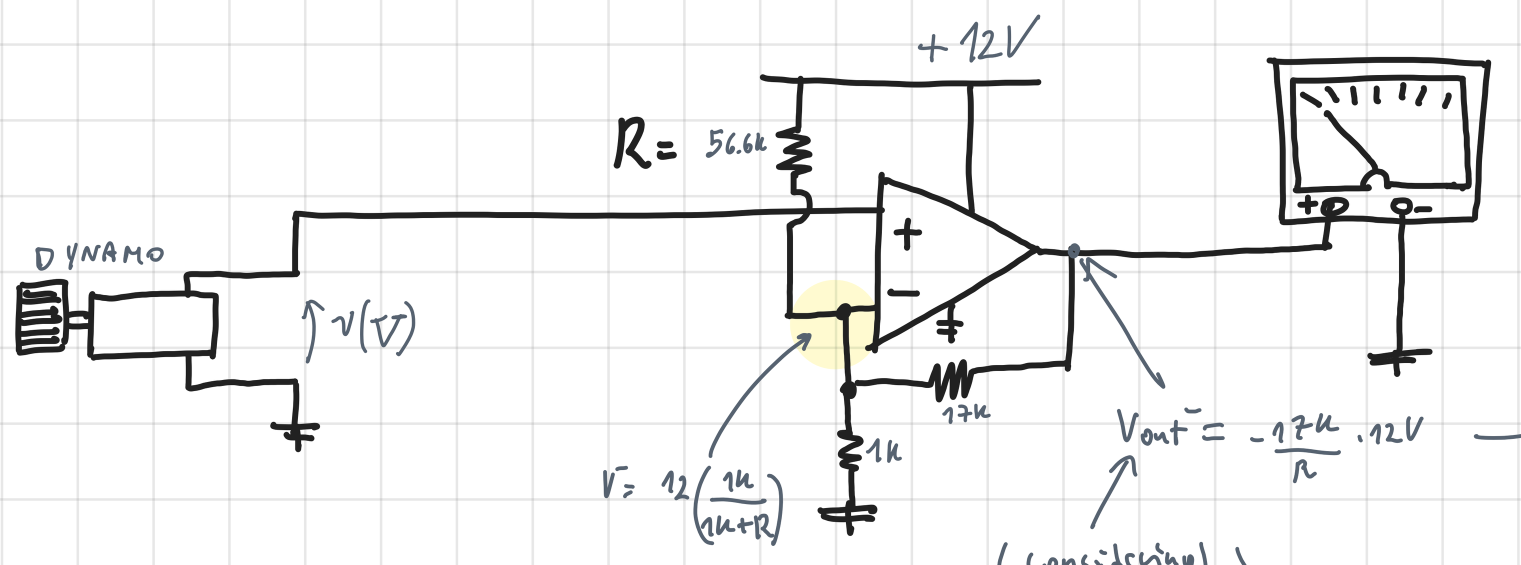
Note: Instead of buying a peculiar battery of 212mV we can obtain this voltage through a proper partition

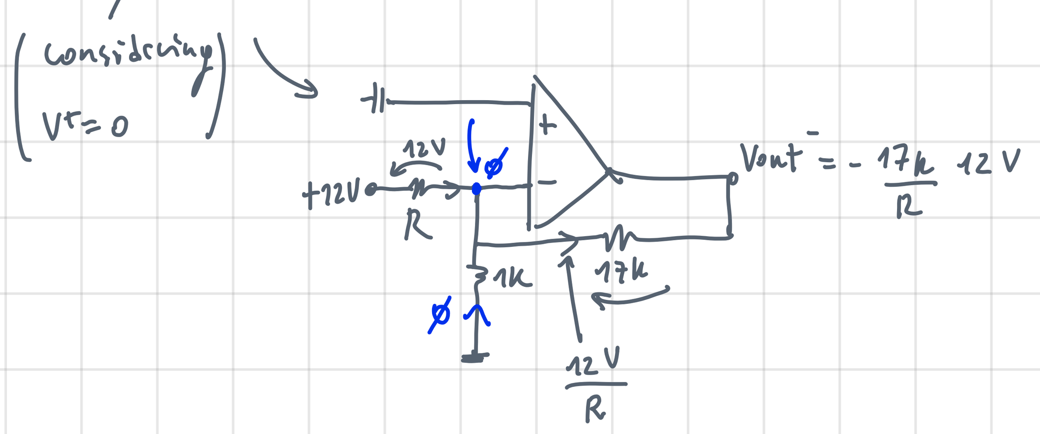


∘ 2nd method

We could also use the Op Amp P.S. to inject current at this node (through a resistor) and choose R such that we have −3.6 V at the output. In this way if we apply the superposition principle for:

(FINAL for speed)





- $V_{in}^+ = 200mV$ ⟶ $V_{out}^+ = 3.6\,V$
- $V_{in}^- = 12\left(\frac{1k}{1k+R}\right)$ ⟶ $V_{out}^- = -3.6\,V$

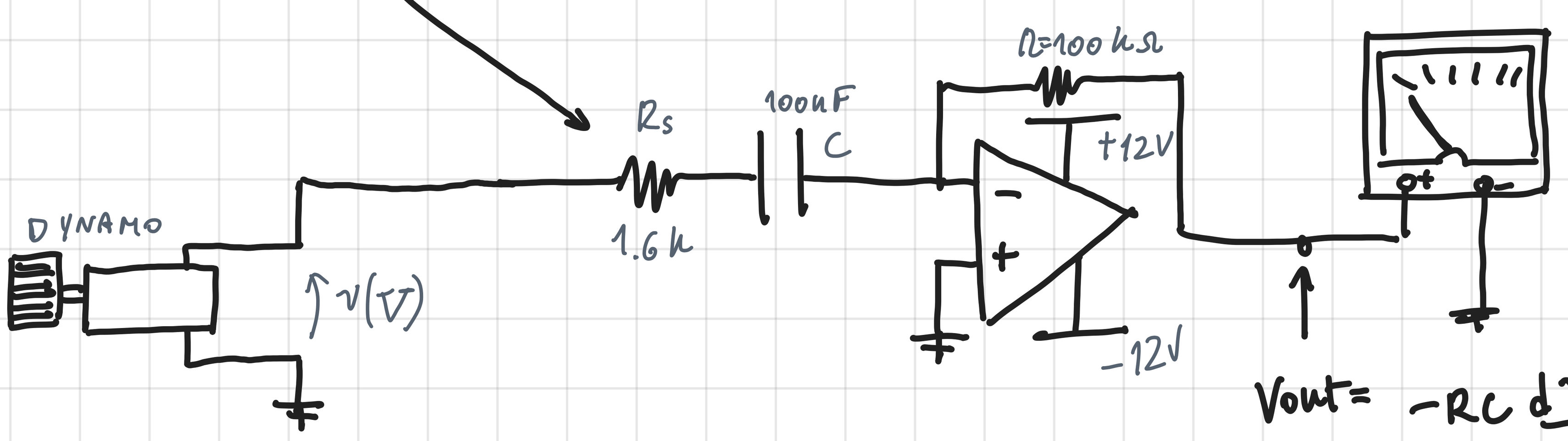
⟶ $V_{out} = V_{out}^+ + V_{out}^- = 0$

$V_{out}^- = -\frac{17k}{R}\,12V = -3.6\,V$

↳ $R = 12V \cdot \frac{17k}{3.6} = 56.666\,\Omega$

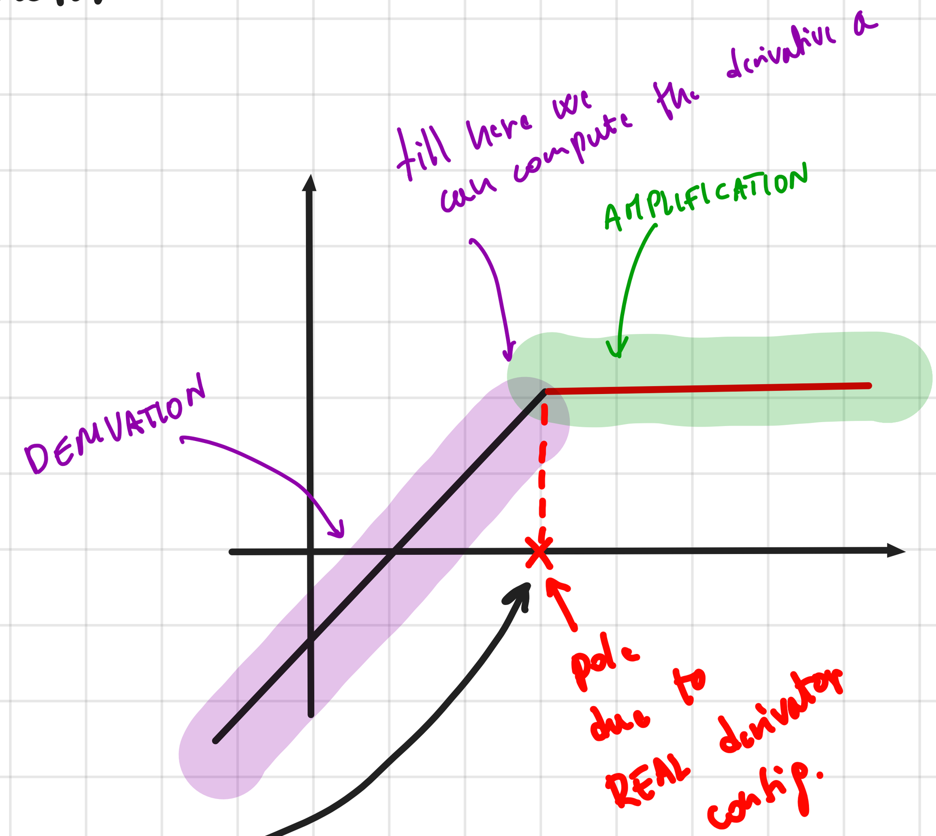
b) For the acceleration we can use the Volt/velocity input and derivate it to a derivator

↳ e.g. real derivator



$a = \frac{dV}{dt}$

$V_{out} = -RC\,\frac{dV_{in}(V)}{dt} = -RC \cdot 50\,\frac{mV}{\frac{m}{s}} \cdot \frac{d\overset{a}{V}}{dt}$



∘ 1st constraint:

↳ the pole will be at $\frac{1}{2\pi R_s C}$ ⟶ e.g. max freq. 1 Hz (1 acc. per second)

• **2nd constraint**: We have to consider the max for the scale

max acc. value: $2g = 2 \cdot 9.81$

$V_{out}|_{max}$: 10 V

$$\Longrightarrow V_{out} = -RC \frac{dV_{in}(V)}{dt} = -RC \cdot 50 \frac{mV}{\frac{m}{s}} \cdot \overbrace{\frac{dV}{dt}}^{a}$$

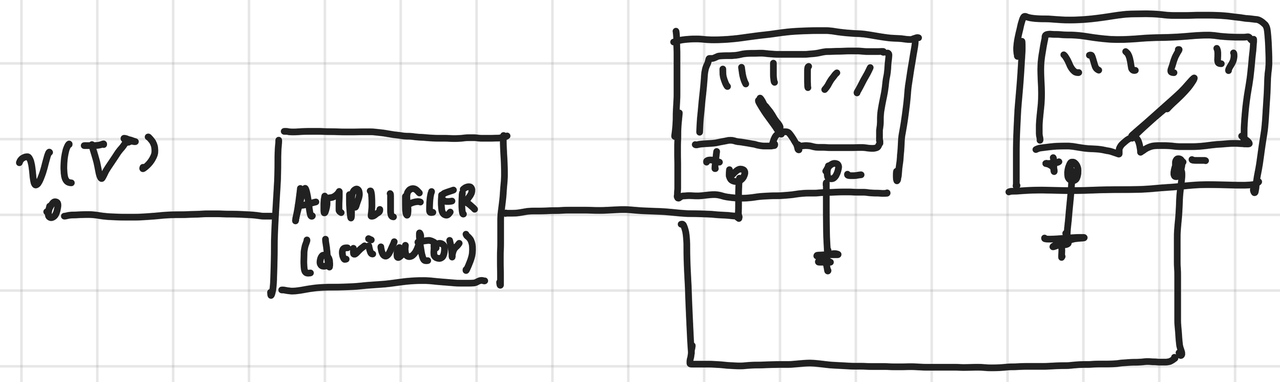
negative sign

$$\hookrightarrow -10\,V = -RC \cdot 50 \frac{mV}{\frac{\cancel{m}}{\cancel{s}}} \cdot 2 \cdot 9.81 \frac{\cancel{m}}{s^{\cancel{2}}} \qquad \longrightarrow RC = \frac{10\,V}{50\,mV \cdot 2 \cdot 9.81} \cong 10\,s$$

↳ Accounting for the constraints we can choose for ex.
$$\begin{cases} C = 100\,\mu F \\ R = 100\,k\Omega \\ R_S \to 1.6\,k\Omega \end{cases}$$
2nd constr.
1st constr.

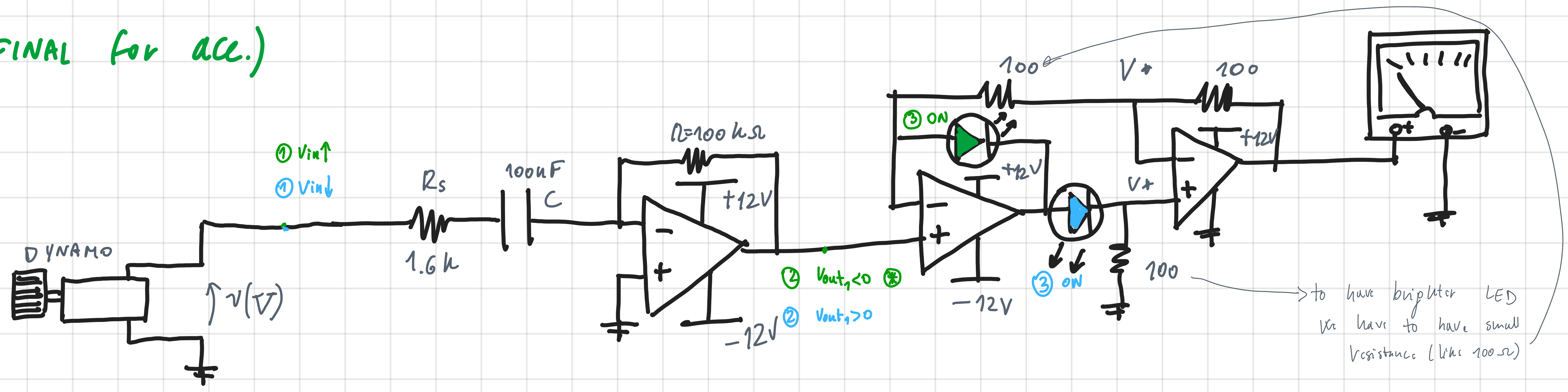
→ To take in account also the fact that the acceleration can be negative

• **1st method** we can attach a scale display with inverted + and − links



• **2nd method** We could also use a double-rectifying circuit → to measure the absolute value of the acc.

(FINAL for acc.)



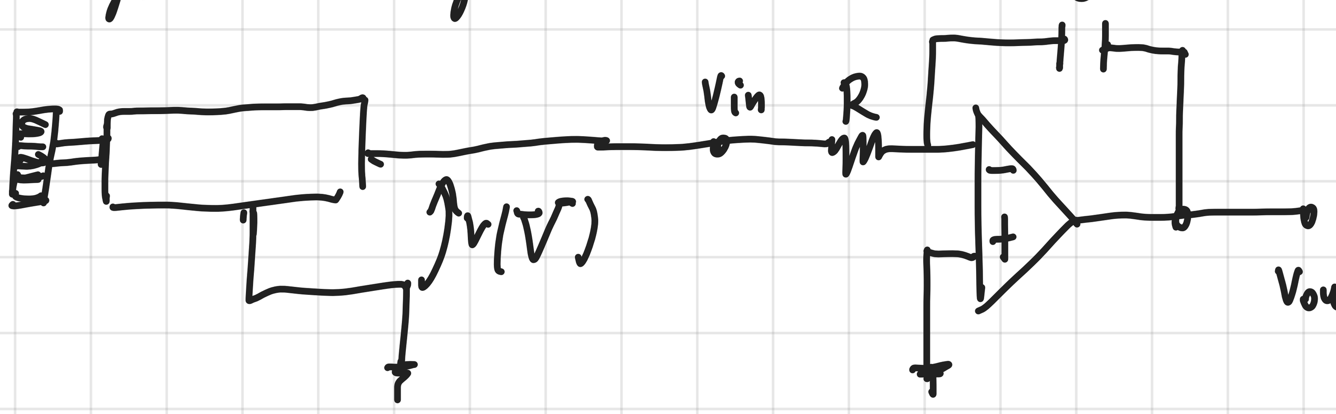
Note: Instead of the diodes we can directly put some LED diodes in this way we can assign a light colour to acceleration/deceleration.

- GREEN DIODE turns ON ⟶ ACCELERATION
- BLUE DIODE turns ON ⟶ DECELERATION

In this way we can know the sign of the acceleration since the output of the double-rectifier will be the acc. absolute value

c) To measure the distance we can use an integrator

↳ e.g. real integrator



RAMP from the volt/speed offset

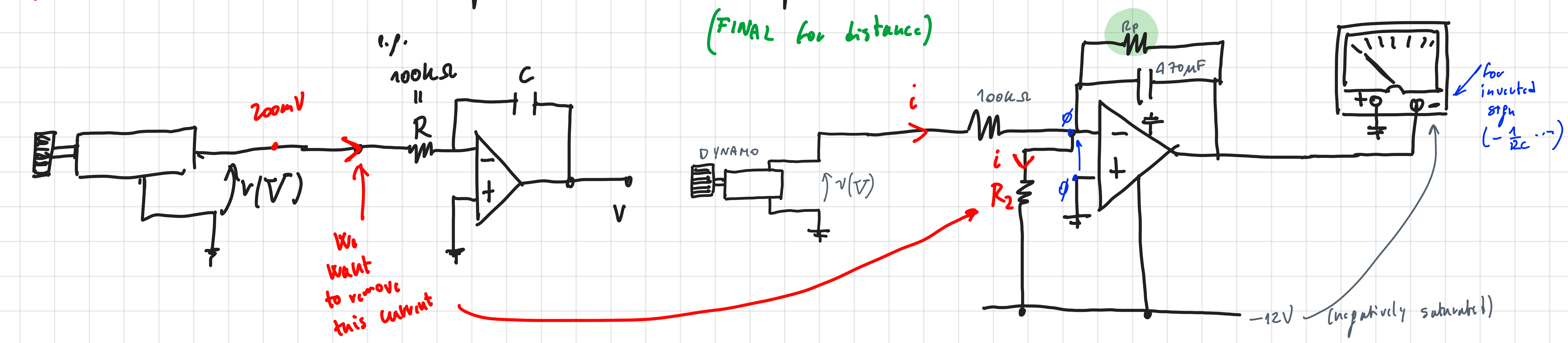
$$V_{out}(t) = \int_0^t \left(50 \frac{mV}{\frac{m}{s}} V + 200\,mV\right) dt \cdot \left(-\frac{1}{RC}\right) = -\frac{1}{RC}\left[50 \frac{mV}{\frac{m}{s}} \underbrace{\int_0^t V(t)\,dt}_{\text{DISTANCE}} + 200\,mV \cdot t\right]$$

↳ **1st constraint**: max value dist. = 10 km ← Prof changed it from the text
max value volt $V_{out}|_{max} = 10V$ ⟶ $V_{out}|_{max} = 10\,V = -\frac{1}{RC} \cdot 50 \frac{mV}{\frac{m}{s}} \cdot \overbrace{10 \cdot 1000}^{10\,km}$

$$\hookrightarrow RC = \frac{50\,mV \cdot 10 \cdot 1k\,[m]}{\left[\frac{m}{s}\right]\ 10\,V} = 50\,s \longrightarrow \text{e.g.} \begin{cases} C = 470\,\mu F \\ R \simeq 100\,k\Omega \end{cases}$$

not exactly 50 μF (tol.)

↳ We have to solve the problem of the ramp due to the +200mV



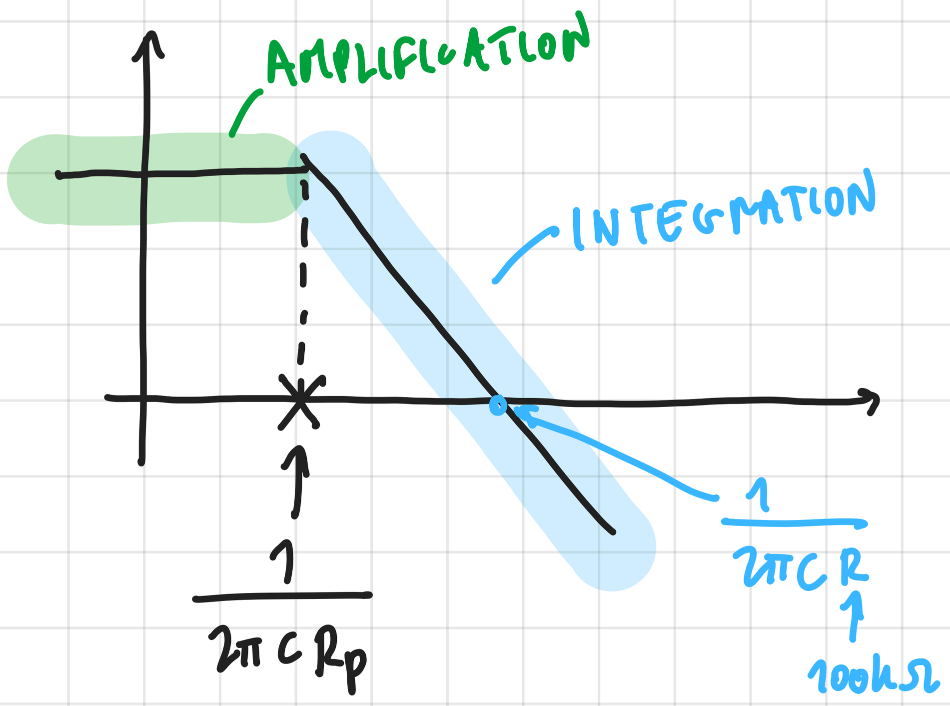
The task of R_2 is to "remove" the current i and prevent it to go through the capacitor so the offset cannot be integrated into a ramp.

$$i = \frac{V_{in}}{R} = \frac{200mV}{100k\Omega} = \frac{12V}{R_2} \longrightarrow R_2 = \frac{12}{0.2} \cdot 100k = 6.4\,M\Omega$$

and the integrator will still produce a ramp out

Note: It's not that possible to have such precise value for R_2, so we'll still have this mismatch for the DC offset 200mV. Since for an ideal integrator the DC gain $\longrightarrow \infty$ we can also limit it with a real integrator (with R_p)

→ With this we saturate the DC gain



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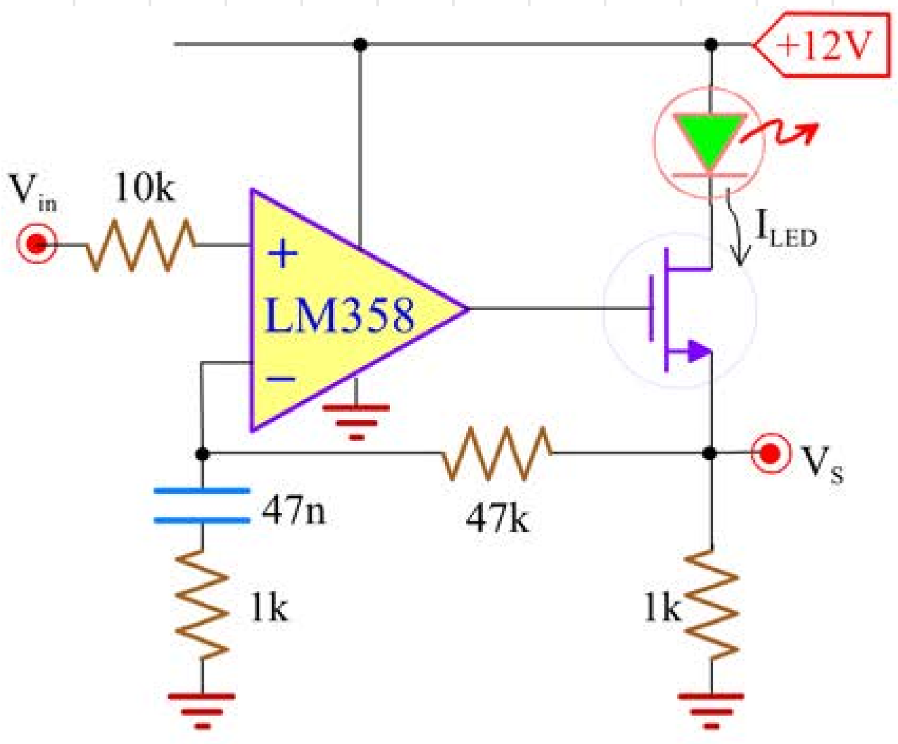
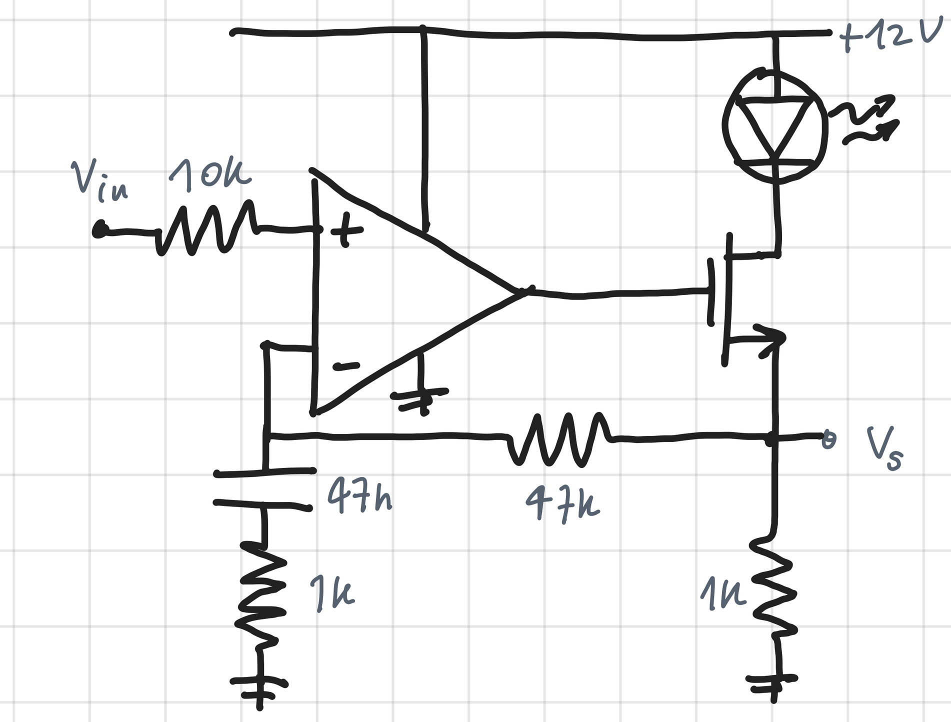




MOSFET: V_T=0.5V $k=1/2\cdot\mu\cdot C_{ox}\cdot W/L=12mA/V^2$ $V_{IN}(t)$ has $\boxed{\text{5V DC}}$ plus a ±100mV sinusoid

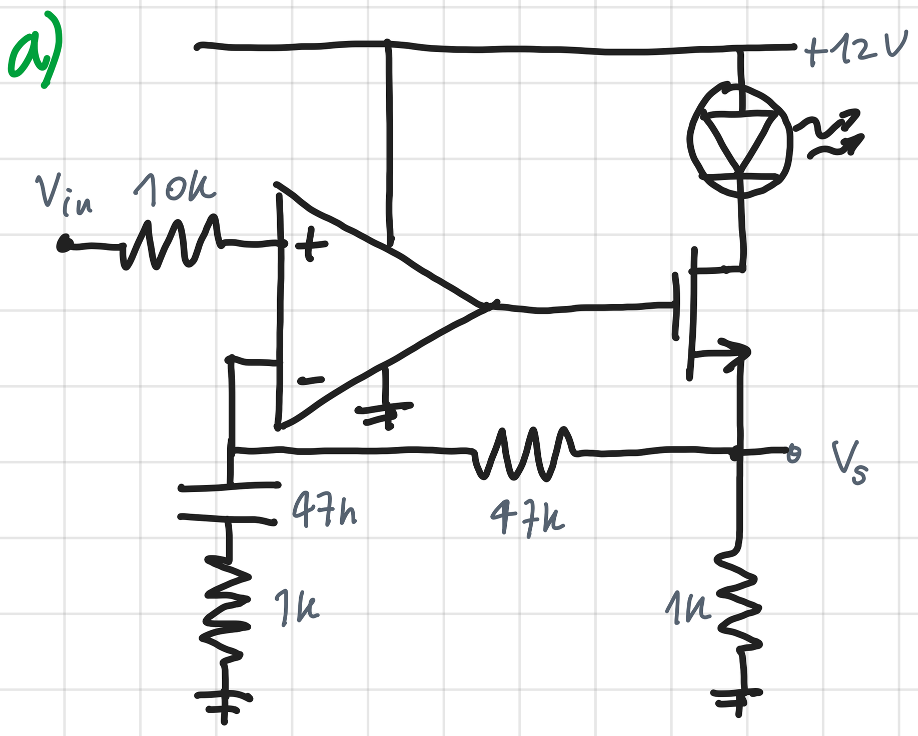
DC VALUE

a) Compute I_{LED}/V_{in} relationship at DC and I_{LED} for V_{in}=5V

b) Plot the Bode diagram of $i_{LED}(f)/v_{in}(f)$

V ⟶ I (TRANCONDUCTANCE)

a)



• at DC: [0 Hz]

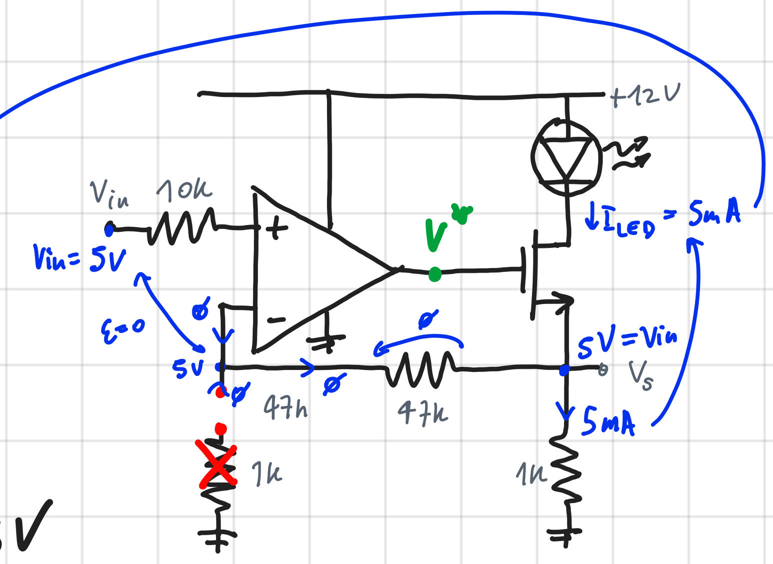
↳ DC value: 5 V

↳ C OPEN

MOSFET:

- $I_{LED} = k V_{OD}^2 = 12\frac{mA}{V^2}(V_{GS}-V_T)^2 = 5mA$
- $V_{GS} = V_T + \sqrt{\frac{5mA}{12\frac{mA}{V^2}}} = 1.15\ V$
- $V_S = 5V$

$V^* = V_{GS}+V_S = 6.15V$ (can supply it with a 12V P.S.)



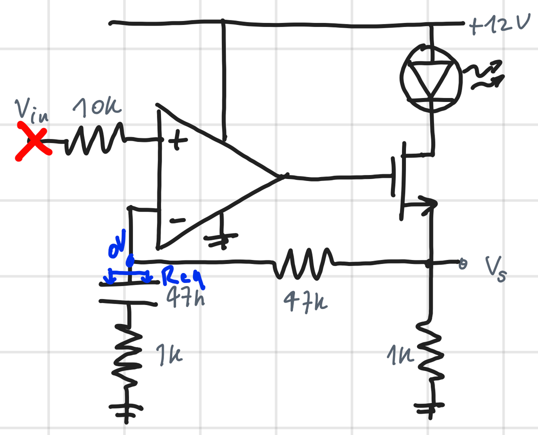
$\Rightarrow G_{DC} = \frac{i_{LED}}{V_{in}} = \frac{V_{in}/1k}{V_{in}} = 1\frac{mA}{V}$

• Zeros and poles

 • Zero (from Bode plot)

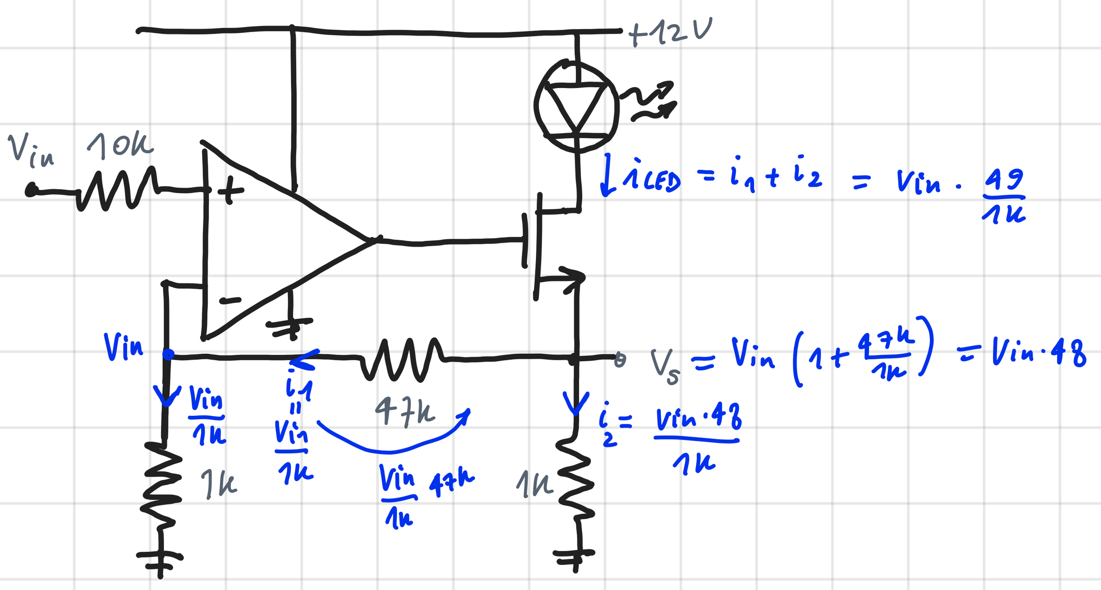
 • Pole $R_{eq} = 1k\Omega$

$$pole = \frac{1}{2\pi C\cdot 1k} = 3.4\ kHz$$

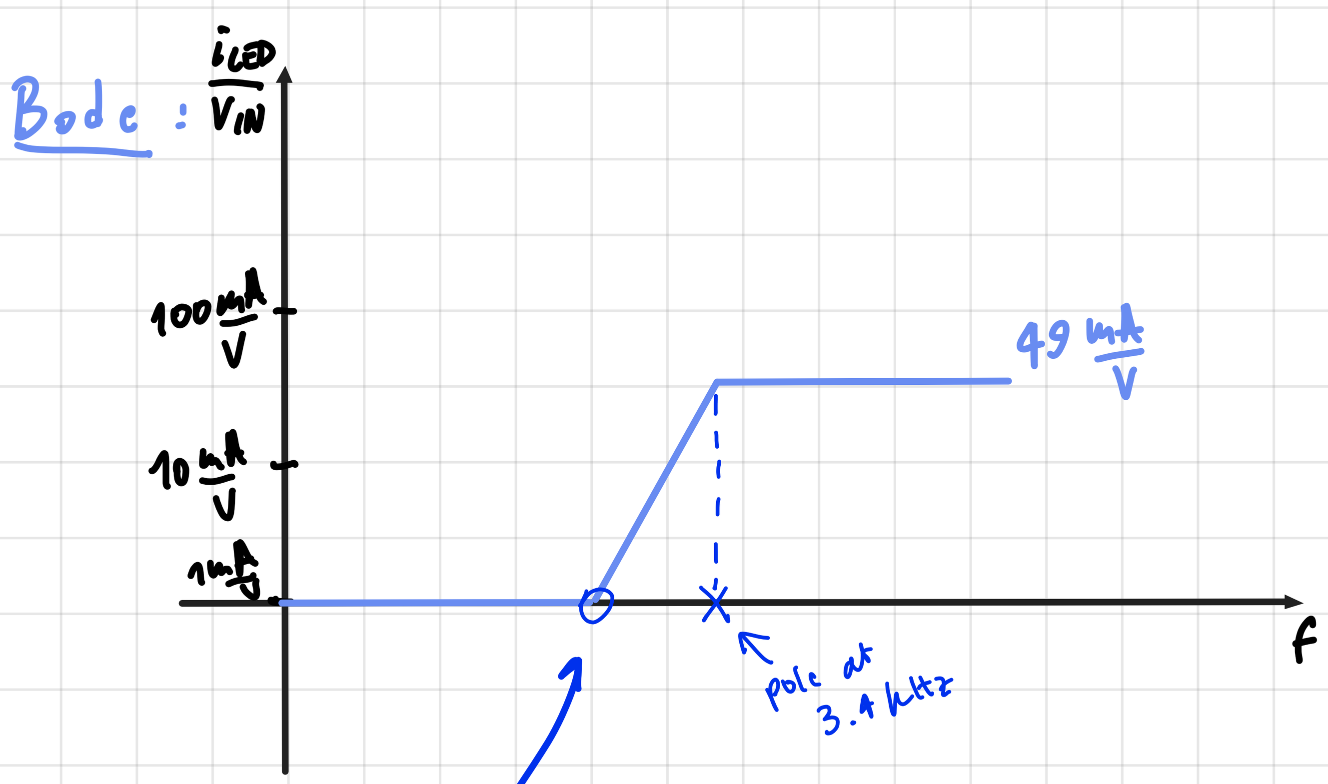


b) • at AC [∞ Hz]

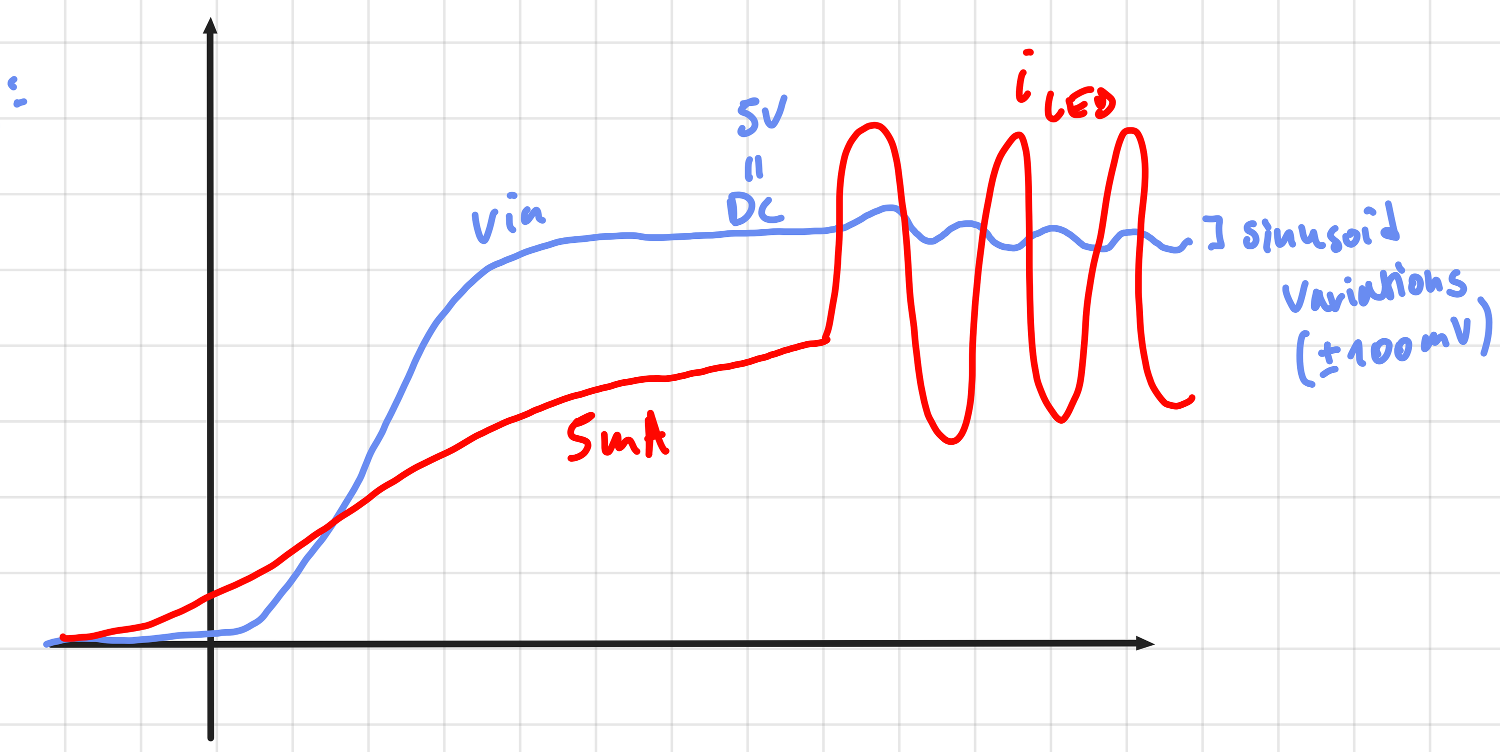
C close



$\Rightarrow G_{AC} = \frac{i_{LED}}{V_{in}} = \frac{49}{1k} = 49\frac{mA}{V}$

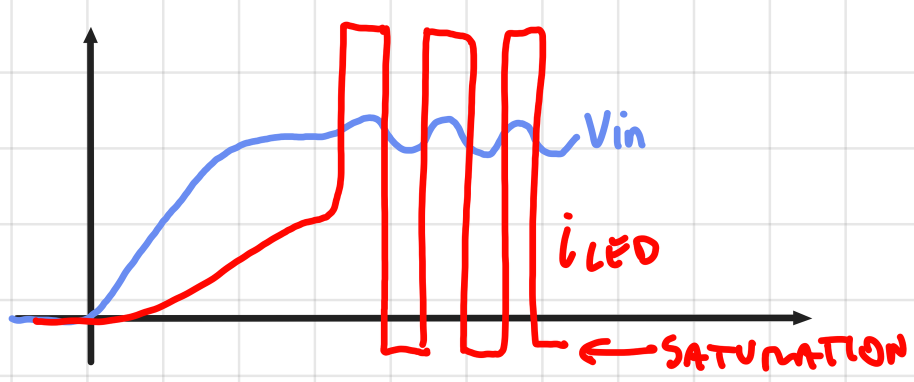


$$zero = \frac{3.4kHz}{49} = 70\ Hz$$



↳ Small signal analysis, from the text we know we have a small signal with DC value 5V ±100 mV sinusoid

↳ Now suppose we have ±1V sinusoid variations ⟶ It means the output will be saturated due to the P.S. (12V)



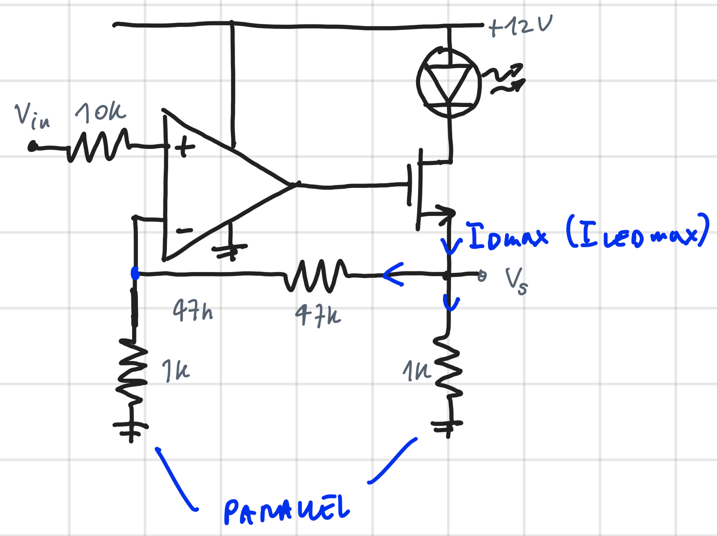
→ Indeed for ±1V $G_{AC} = 49\frac{mA}{V}$ ⟹ $i_{LED} = \pm 49\ mA$ + DC value of 5mA = 54 mA

So V_S = 54V ⟶ so $V_G > V_S$ but V_G is limited to +12 V (P.S.)

→ We can actually compute the maximum current for the max. $V_G = 12V$

↳ $V_G|_{max} = 12V$

$$I_D|_{max} = 12\,\frac{mA}{V^2}\left(V_G - V_S - V_T\right)^2 = 12\,\frac{mA}{V^2}\left(\overbrace{12V - V_S - 0.5}^{11.5}\right)^2$$



$$V_S|_{max} = I_{Dmax}\,(1k \,\|\, 48k) \cong I_{Dmax} \cdot 1k$$

$$\hookrightarrow I_{Dmax} = 12\,\frac{mA}{V^2}\,\overbrace{\left(11.5V - I_{Dmax}\cdot 1000\right)^2}^{I_{Dmax}^2 (1k)^2 - 2\cdot 11.5 \cdot I_{Dmax}\cdot 1k + 11.5^2}$$

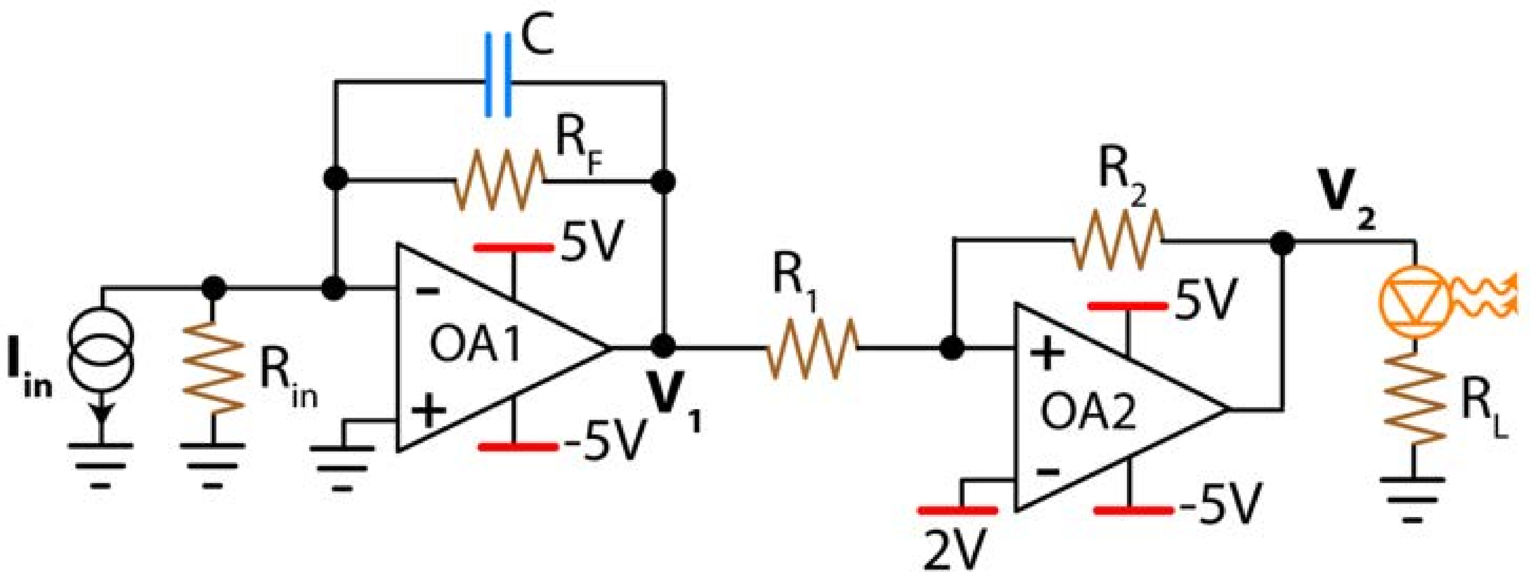
$$\hookrightarrow I_{Dmax}^2 \underbrace{(1k)^2 \cdot 12\,\frac{mA}{V^2}}_{12k} - \underbrace{\left(1 + 12\,\frac{mA}{V}\cdot 2\cdot 11.5\cdot 1k\right)}_{277} I_{Dmax} + \underbrace{12\,\frac{mA}{V^2}\cdot 11.5^2}_{1{,}587} = 0$$

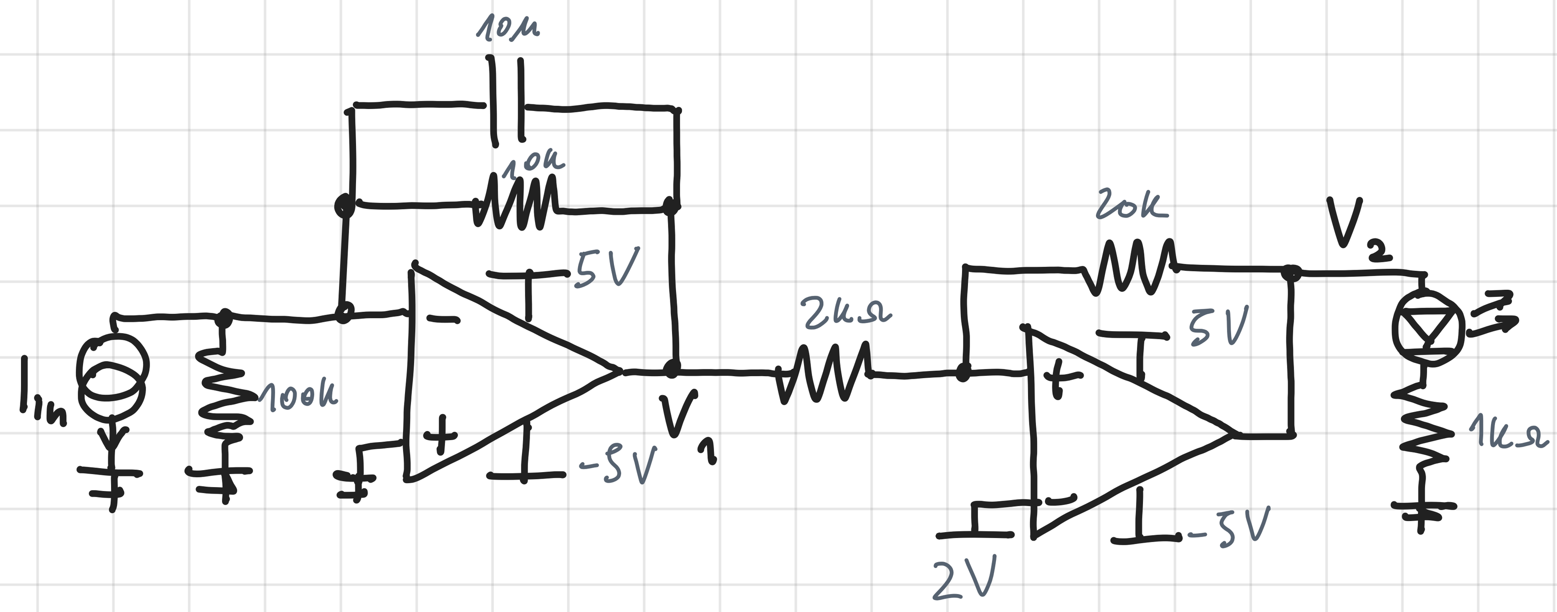
→ $I_{Dmax} = 12{,}5\ mA$ ← MAX one

→ $I_{Dmax} = 10{,}6\ mA$

$$\frac{277 \pm \overbrace{\sqrt{277^2 - 4\cdot 12k \cdot 1{,}587}}^{\sqrt{533} \cong 23{,}156}}{24k} =$$

④





R_{in}=100kΩ R_F=10kΩ   C=10µF R_1=2kΩ R_2=20kΩ R_L=1kΩ

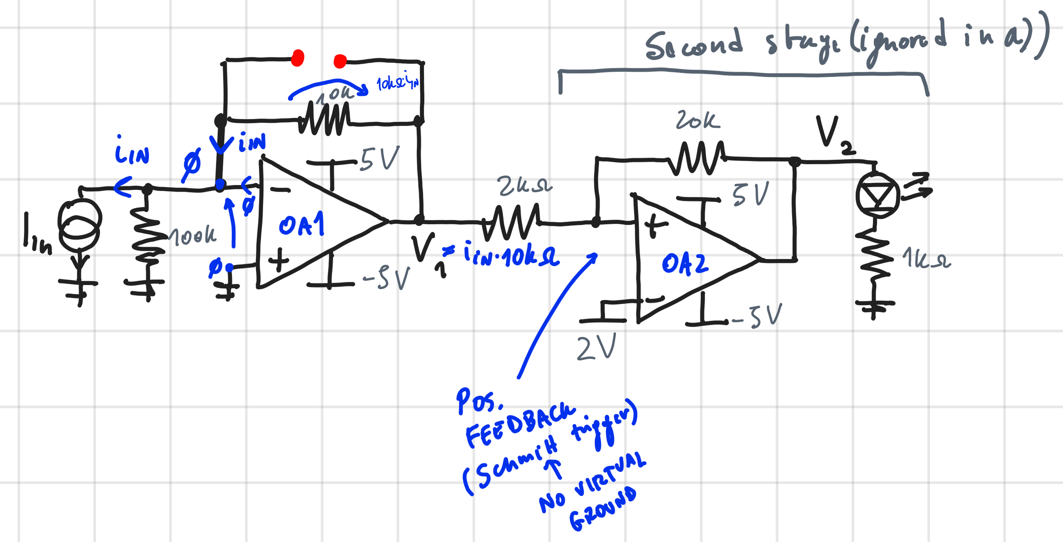
a) Compute the effect of I_B=100nA and V_{OS}=3mV of OA1 on V1

b) Plot the static curve V_1 vs. V_2

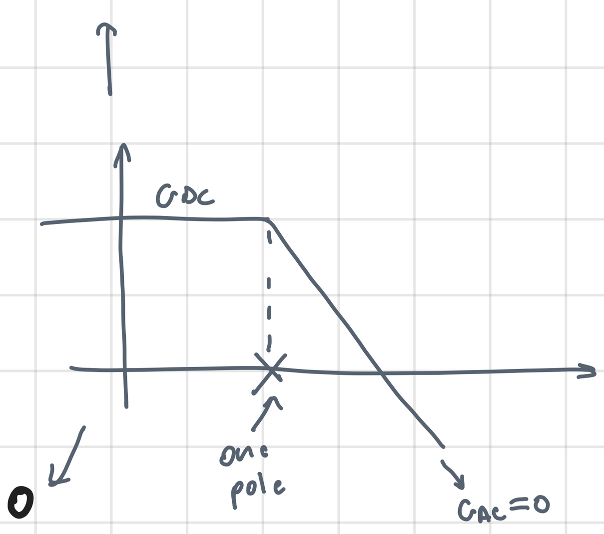
c) Compute the minimum amplitude I_{in} (20Hz sinusoidal) to switch on the LED

a) $\rightarrow \left|\frac{V_1}{i_{IN}}\right|$?

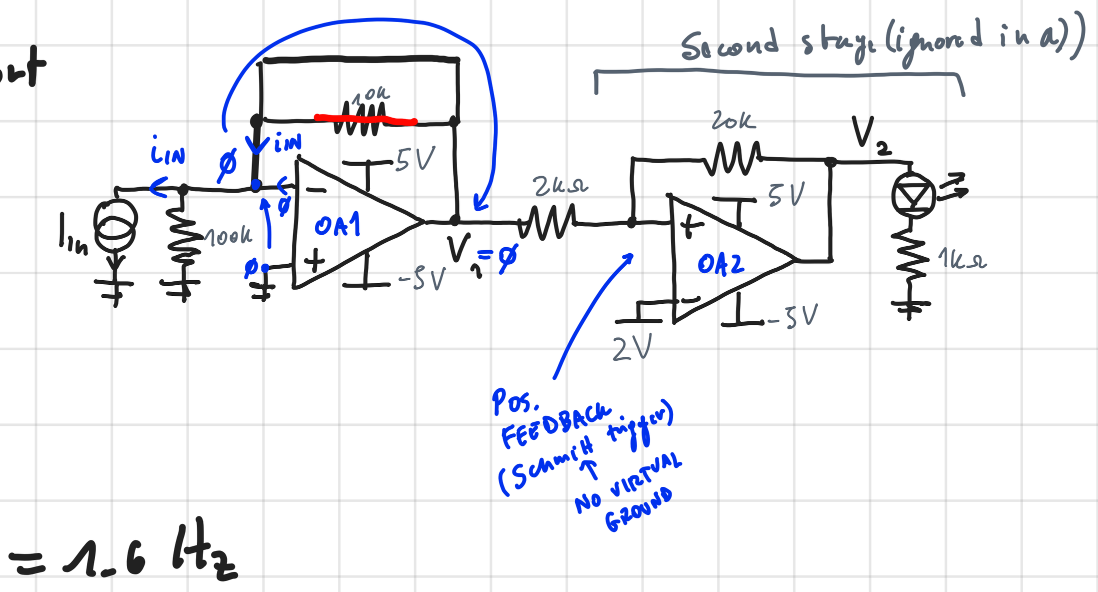
- at DC: [0 Hz]   C → OPEN



$\Rightarrow G_{DC} = \frac{V_1}{i_{IN}}(0) = 10k\Omega$



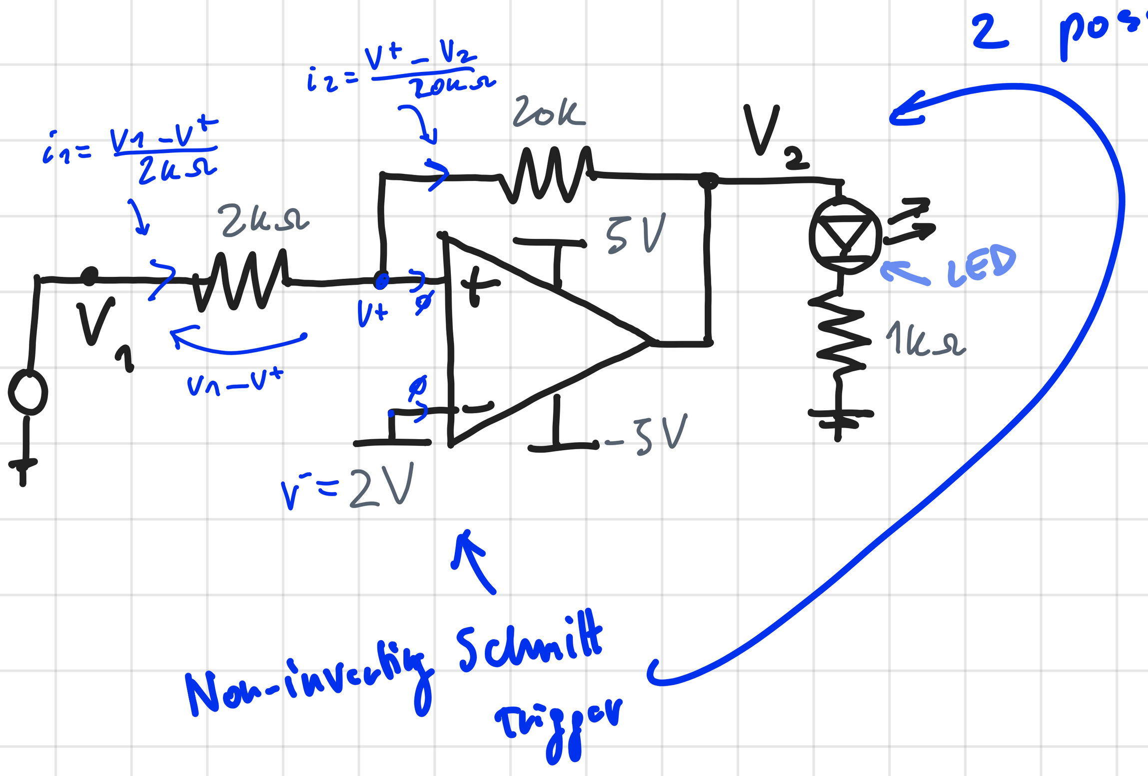
- at AC: [∞ Hz]   C ↪ short



$\Rightarrow G_{AC} = \frac{V_1}{i_{IN}}(\infty) = 0$

- $\text{pole} = \frac{1}{2\pi\, 10\mu F \cdot \underbrace{10k\Omega}_{R_{eq}=R_F=10k\Omega}} = 1.6\ Hz$

b) $\rightarrow \frac{V_2}{V_1}$ SECOND STAGE:



2 possible outputs: +5 / -5

→ current KCL:

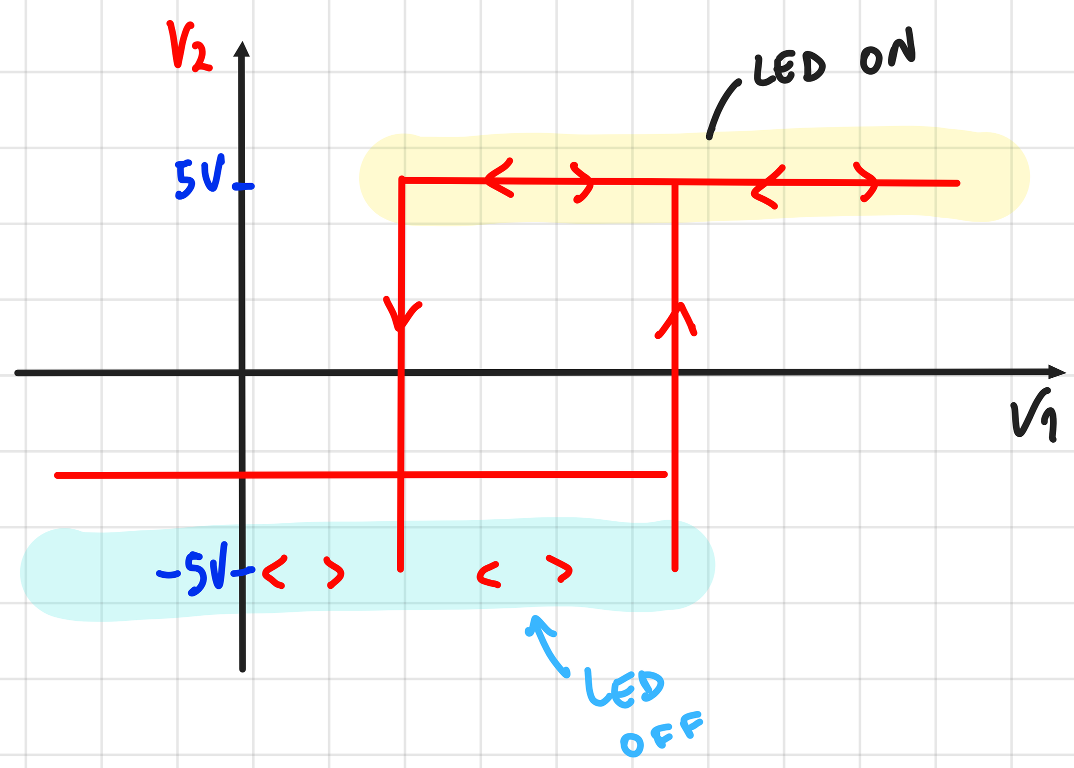
$i_{L1} = i_{L2} \rightarrow \frac{V_1 - V^+}{R_1} = \frac{V_1 - V_2}{R_2}$ Eq.1

→ We analyze when $\varepsilon = 0 \rightarrow V^+ = V^- = 2V$ Eq.2

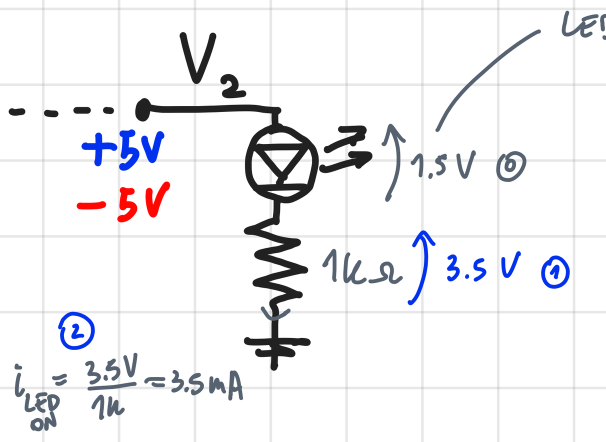
↪ {Eq.1, Eq.2} $\rightarrow \frac{V_1 - 2}{2k\Omega} = \frac{2 - V_2}{20k\Omega}$

→ • for output $V_2 = +5V \longrightarrow V_1 = V_{TL} = \frac{(2-5)V \cdot 2k\Omega}{20k\Omega} + 2V = 1.7\ V$ (low)

• For output $V_2 = -5V \longrightarrow V_1 = V_{TH} = \frac{(2+5)V \cdot 2k\Omega}{20k\Omega} + 2V = 2.7\ V$



c)



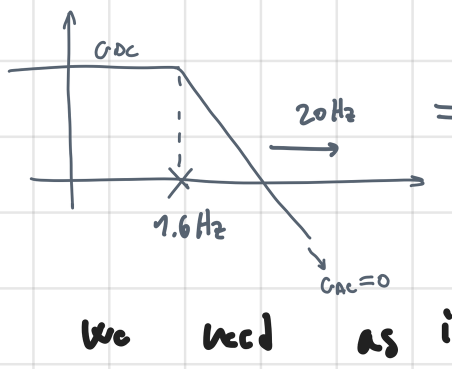
LED usually requires 1.5V

LED is ON → $i_{LED\ ON} = 3.5mA$

threshold to TURN ON: $V_{TH} = 2.7V = V_1$

the gain to obtain $V_1 = V_{TH}$ and turn on the LED is freq. dependent

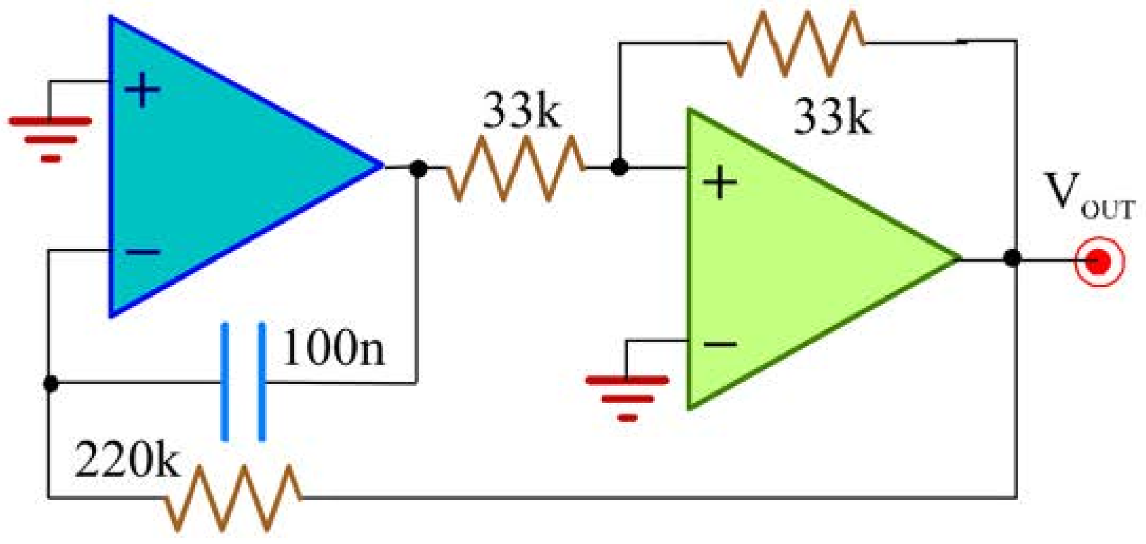
↪ at 20 Hz G(20Hz) but from the previous Bode:

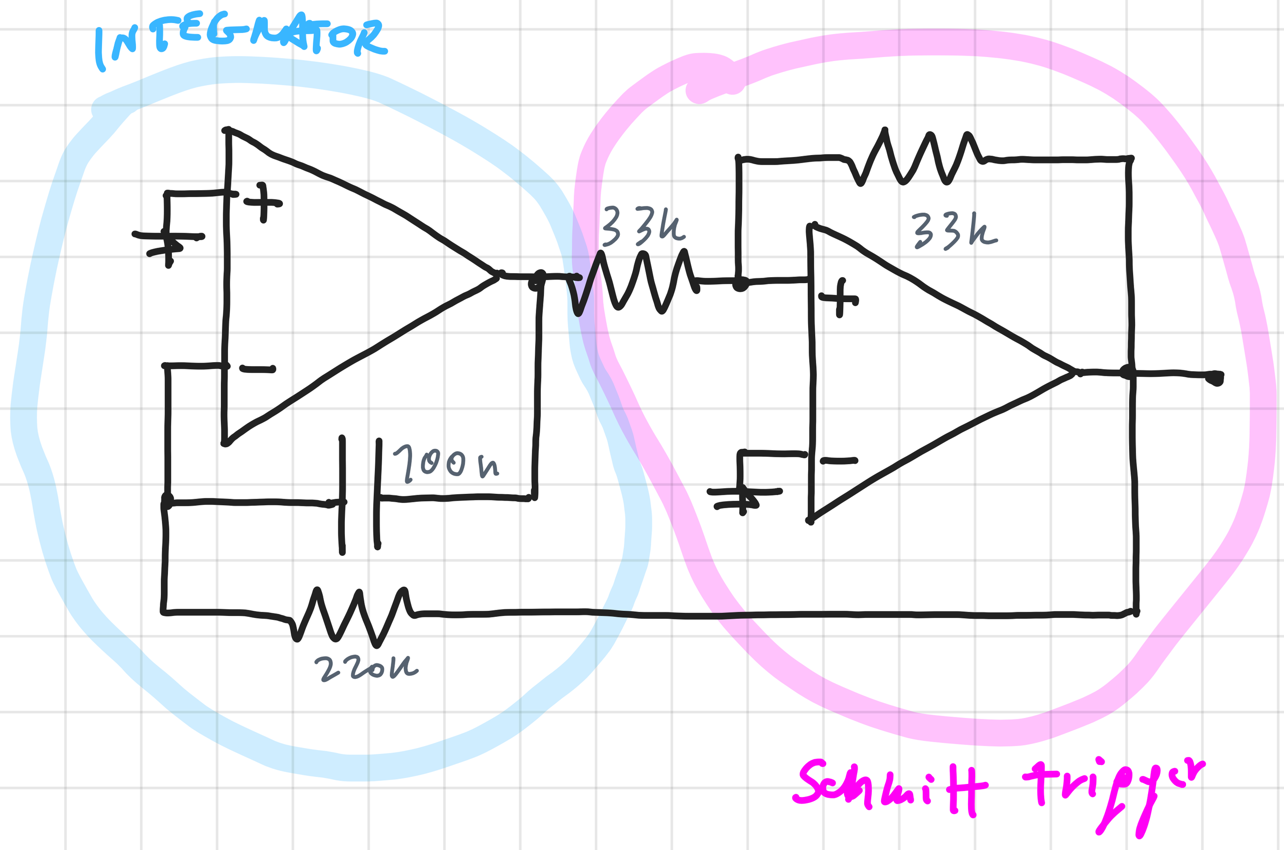


⇒ Small gain ➡ $G(20Hz) = \frac{G_{DC}}{\frac{20}{1.6}} = 0.8 \frac{mV}{\mu A}$

↪ so to trigger the compensator and turn on the LED we need as input to get $V_1 = V_{TH} = 2.7$ through an amplifier with gain G(20Hz) is: $i_{IN} = \frac{2.7V}{0.8\frac{mV}{\mu A}} = 3.4mA$ → then the LED turns ON

5



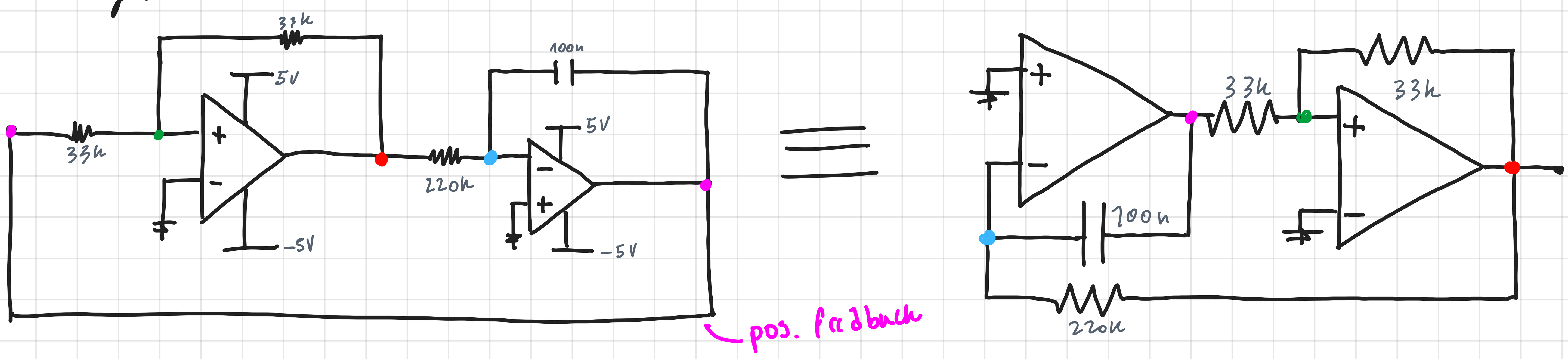


Rail-to-rail OpAmp biased at ±5V. At t=0s, the capacitor is discharged.

a) Plot all waveforms

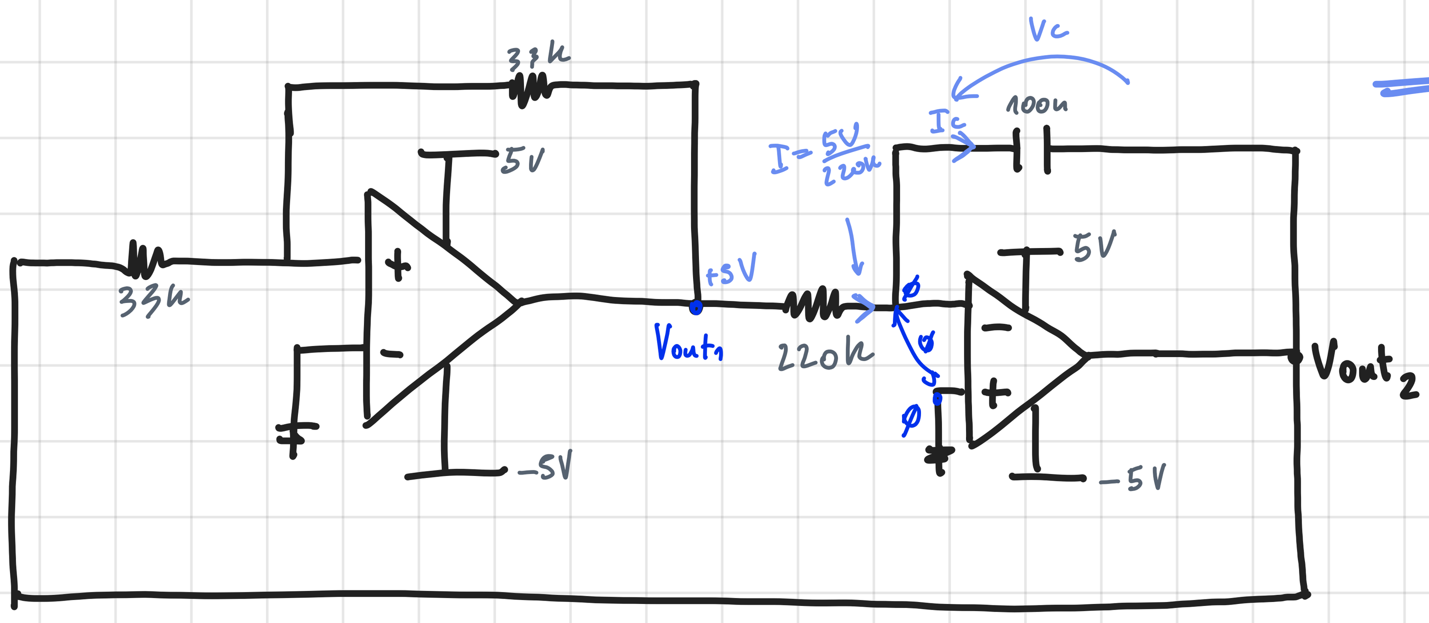
b) Write the equation of output frequency vs. R and compute the value for R=220kΩ

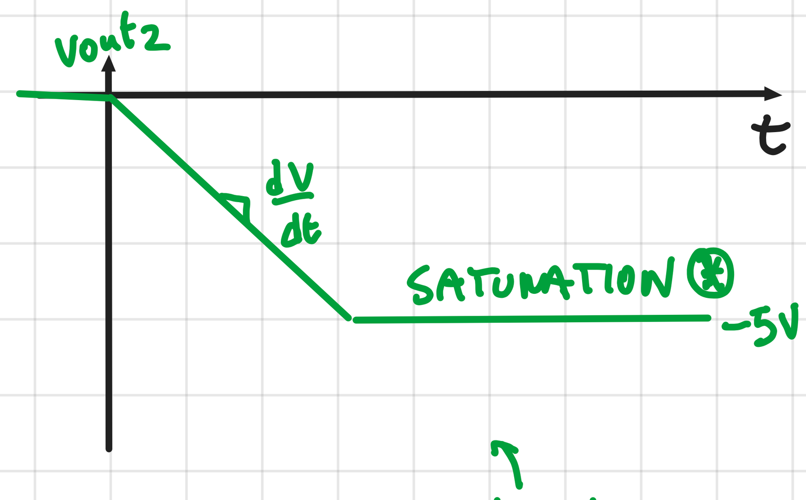
a) Instead of the circuit in the figure we start our analysis drawing the integrator and trigger configurations in a different way:



Now, we know that the Schmitt trigger can have only two possible outputs : +5V, -5V

- For $V_{out_1} = +5V$





$$\Longrightarrow I = \frac{5V}{220k\Omega} = I_c = \frac{C\, dV_c}{dt}$$

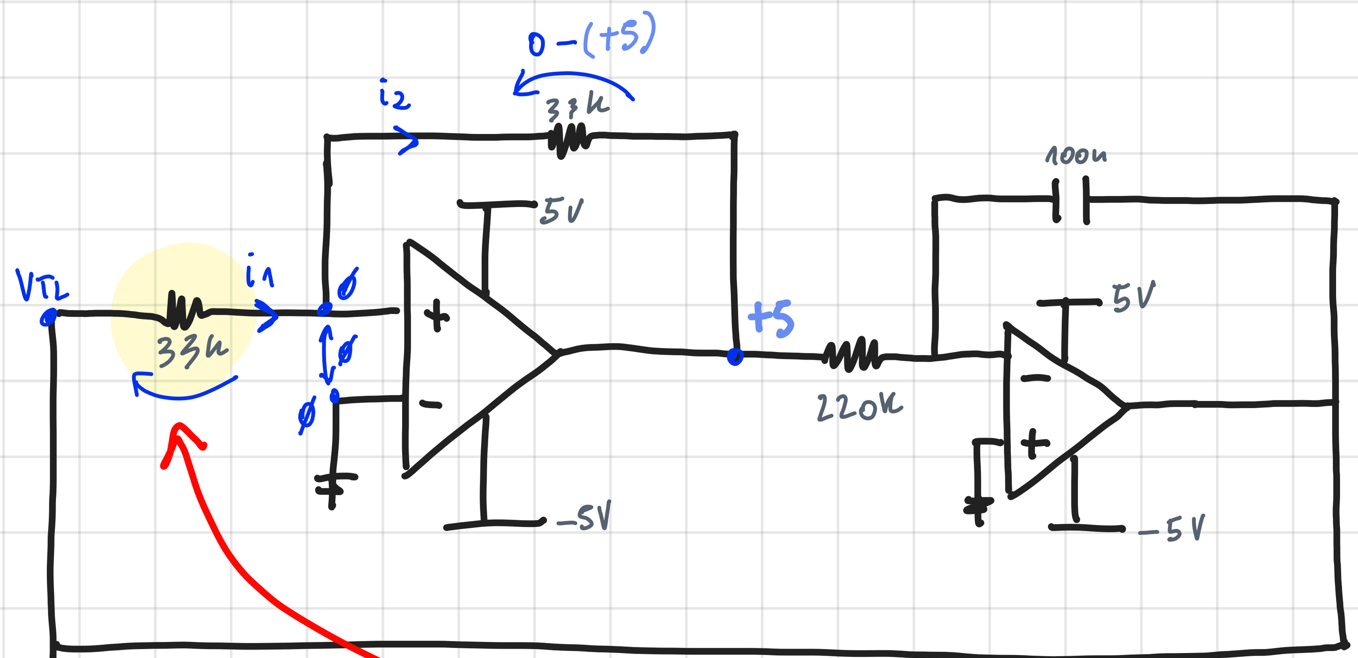
$$\hookrightarrow \frac{dV_c}{dt} = \frac{I}{C} = \frac{5V}{220k\Omega \cdot 100n} = 227 \frac{V}{s}$$

$$V_{out_2} = -V_c = -\frac{1}{C}\int_0^t I(t)\,dt = -\frac{1}{220k\Omega\, 100nF}\int_0^t \overset{5V}{\overset{\shortparallel}{V_{out_1}}}\, dt = -227\frac{V}{s}\cdot t\,[s]$$

(*) We actually don't know if V_{out2} will saturate to -5V before the trigger commutes (from +5V ⟶ -5V)

↑ low threshold

↪ Let's compute the threshold value for which the trigger commutes. We analyze when $V_{in1} = V_{out2} = V_{TL}$ is such that $i_1 = i_2$

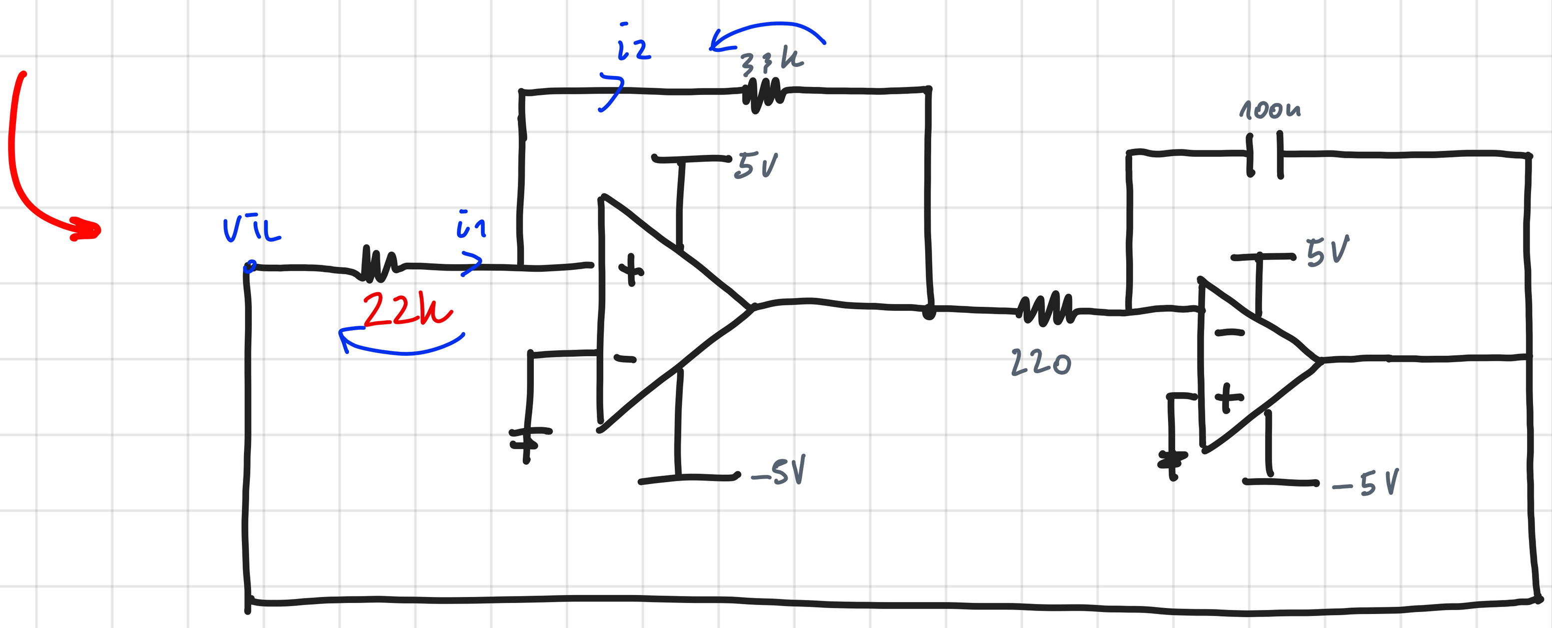


$$\longrightarrow i_1 = \frac{V_{TL}}{33k\Omega} = i_2 = \frac{-5V}{33k\Omega}$$

$\hookrightarrow$ $V_{TL} = -5V$ ⟵ threshold on the SATURATION

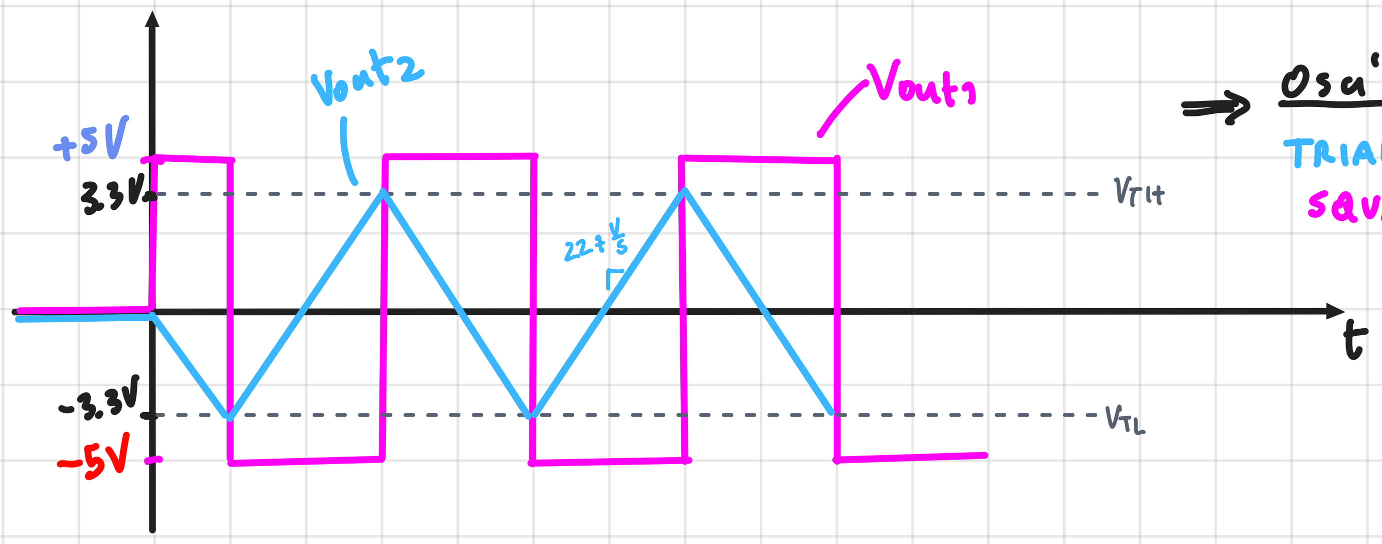
it's better to consider a different value for this resistor

↪ e.g. 22kΩ



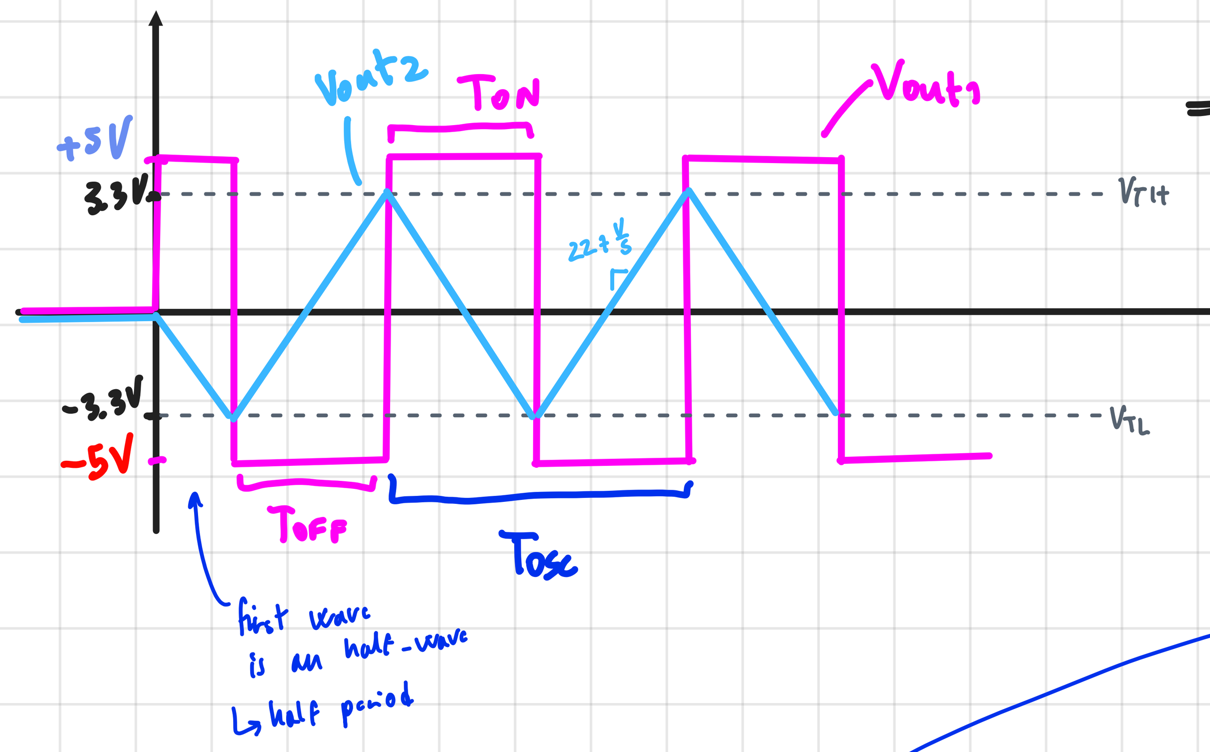
$$\longrightarrow i_1 = \frac{V_{TL}}{22k\Omega} = i_2 = \frac{-5V}{33k\Omega} \longrightarrow V_{TL} = -5\cdot\frac{22}{33} = -3.3V$$

(Since the V_{out_1} is simmetric ±5V ⟹ $V_{TH} = 3.3V$)



⟹ Oscillator: TRIANGULAR WAVE, SQUARE WAVE

Oscillator analysis



$\Rightarrow$ Oscillator ← simply - stable

TRIANGULAR WAVE

SQUARE WAVE

$\Longrightarrow$ $T_{osc} = T_{ON} + T_{OFF} = 58\ ms$ ⟶ $f_{osc} = \frac{1}{58\ ms} = 17\ Hz$

$T_{OFF} = T_{ON} = \dfrac{2 \cdot 3.3\,V}{227\ \frac{V}{s}} = 29\ ms$

$\dfrac{5\,V}{\underbrace{220\,k\Omega}_{R} \cdot 100\,nF}$

b) $T_{osc} = \dfrac{2 \cdot 2 \cdot 3.3\,V}{\dfrac{5\,V}{R \cdot 100\,nF}} = 264\ \dfrac{ns}{\Omega}\ R$

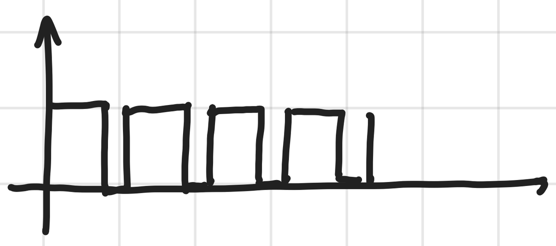
↳ $f_{osc} \cong 3{,}8\ \dfrac{M\Omega}{s} \cdot \dfrac{1}{R}$ $\quad \left(f_{osc}(220\,k\Omega) \simeq 17\,Hz\right)$

Obs. Oscillators

We can have different trends with this oscillator configurations.

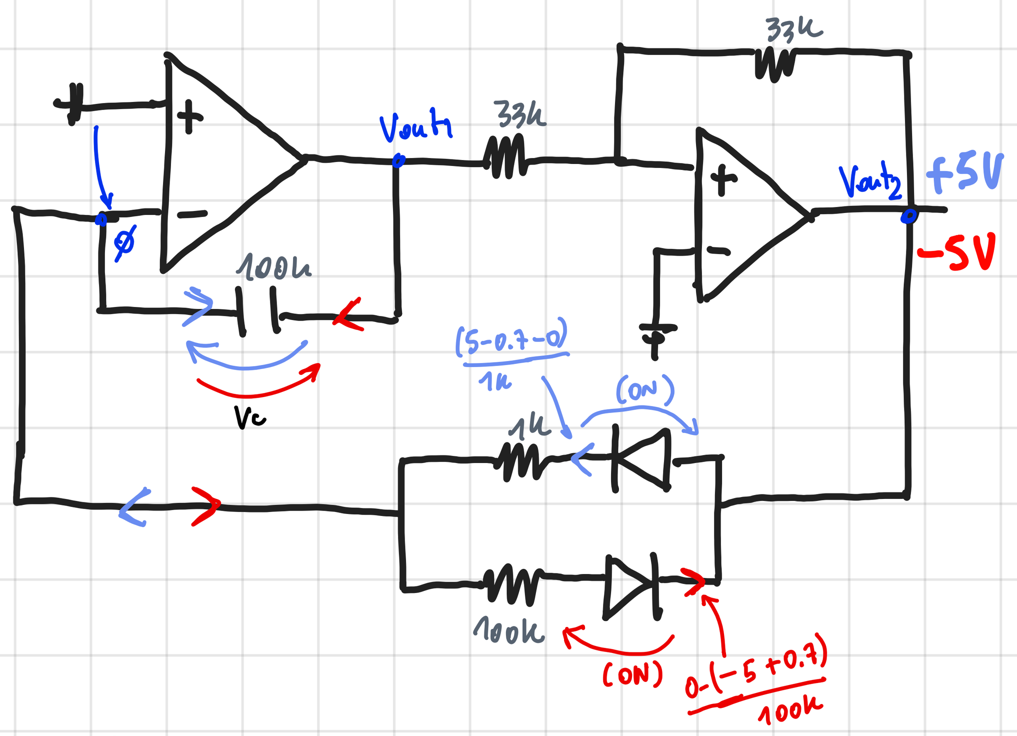
e.g. • saw tooth

• different T_{ON}, T_{OFF}



⟶ Duty cycle change : $\text{Duty Cycle} = \dfrac{T_{ON}}{T_{ON}+T_{OFF}}$

ex.



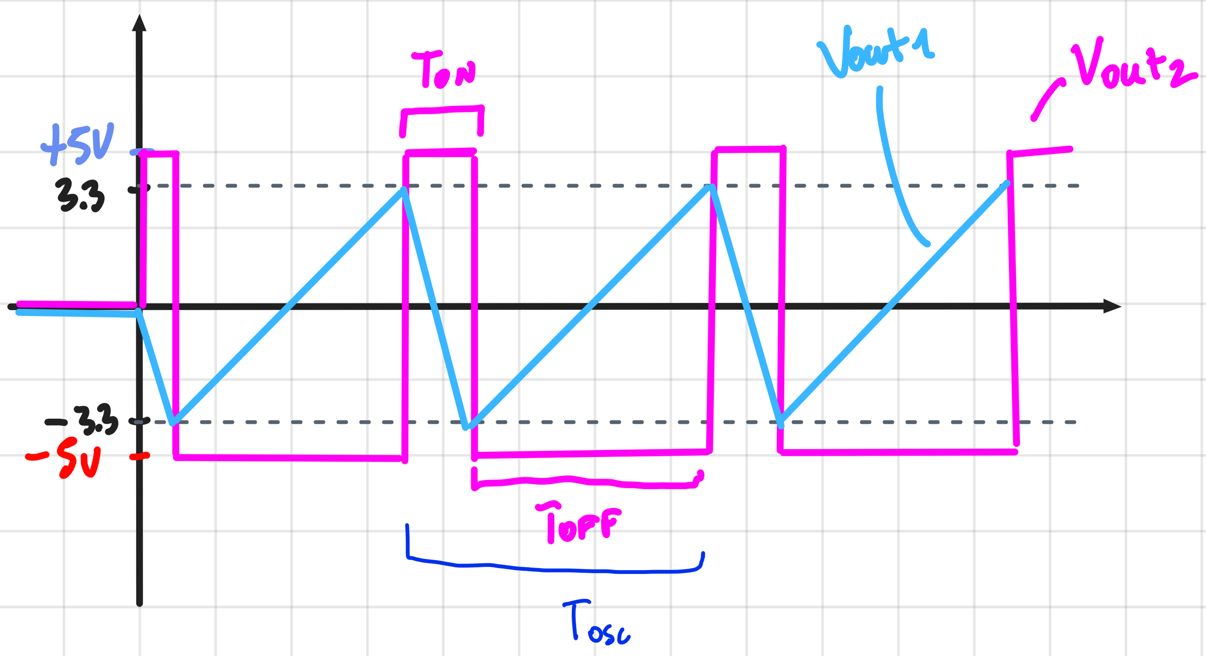
(Diode voltage 0.6 V - 0.7 V)

$\Rightarrow$ • $V_{out_1} = -V_c$ ⟶ $\dfrac{dV_{out_1}}{dt} = -\dfrac{I}{C} = -\dfrac{5-0.7-0}{1k \cdot 100n} = -43\ k\ \dfrac{V}{s}$ ← much faster slope ⟶ different $T_{ON} \neq T_{OFF}$

• $V_{out_1} = V_c$ ⟶ $\dfrac{dV_{out_1}}{dt} = \dfrac{I}{C} = \dfrac{0-(-5+0.7)}{100k \cdot 100n} = 430\ \dfrac{V}{s}$

SQUARE WAVE with ≠ Duty Cycle

∼ SAW TOOTH WAVE



$T_{ON} = \dfrac{2 \cdot 3.3\,V}{43\ \frac{kV}{s}} = 154\ \mu s$

$\wedge\wedge$

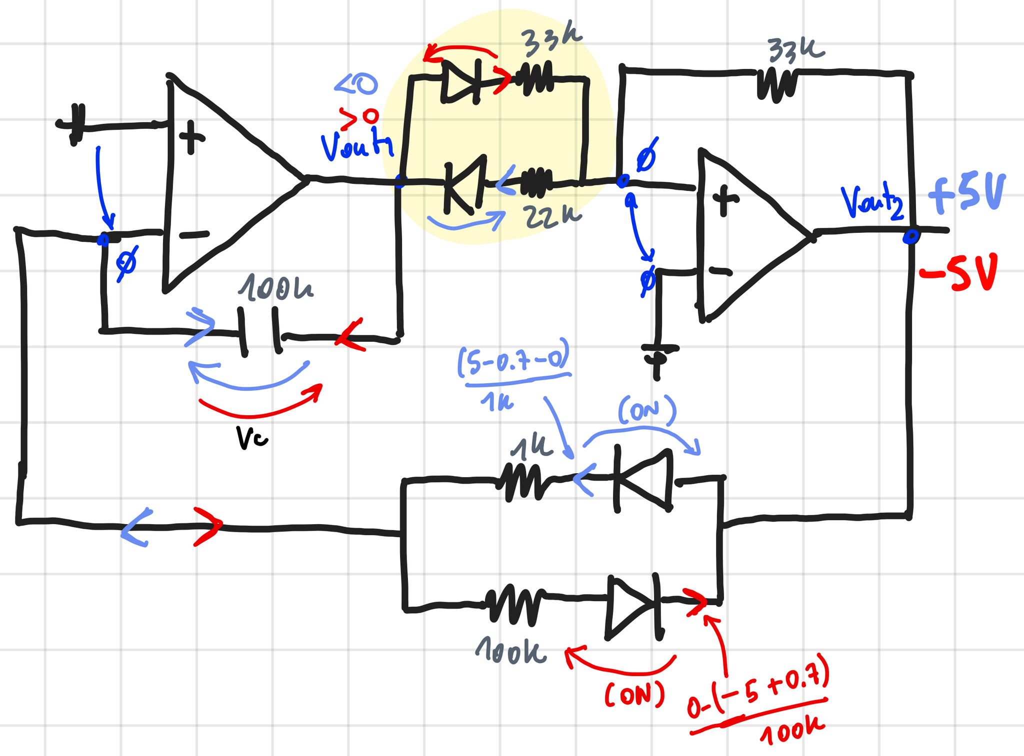
$T_{OFF} = \dfrac{2 \cdot 3.3\,V}{430\ \frac{V}{s}} = 15\ ms$

$T = T_{ON} + T_{OFF} \cong T_{OFF} = 15\,ms$

↳ $\text{Duty Cycle} = \dfrac{T_{ON}}{T} = 0{,}01\ \%$

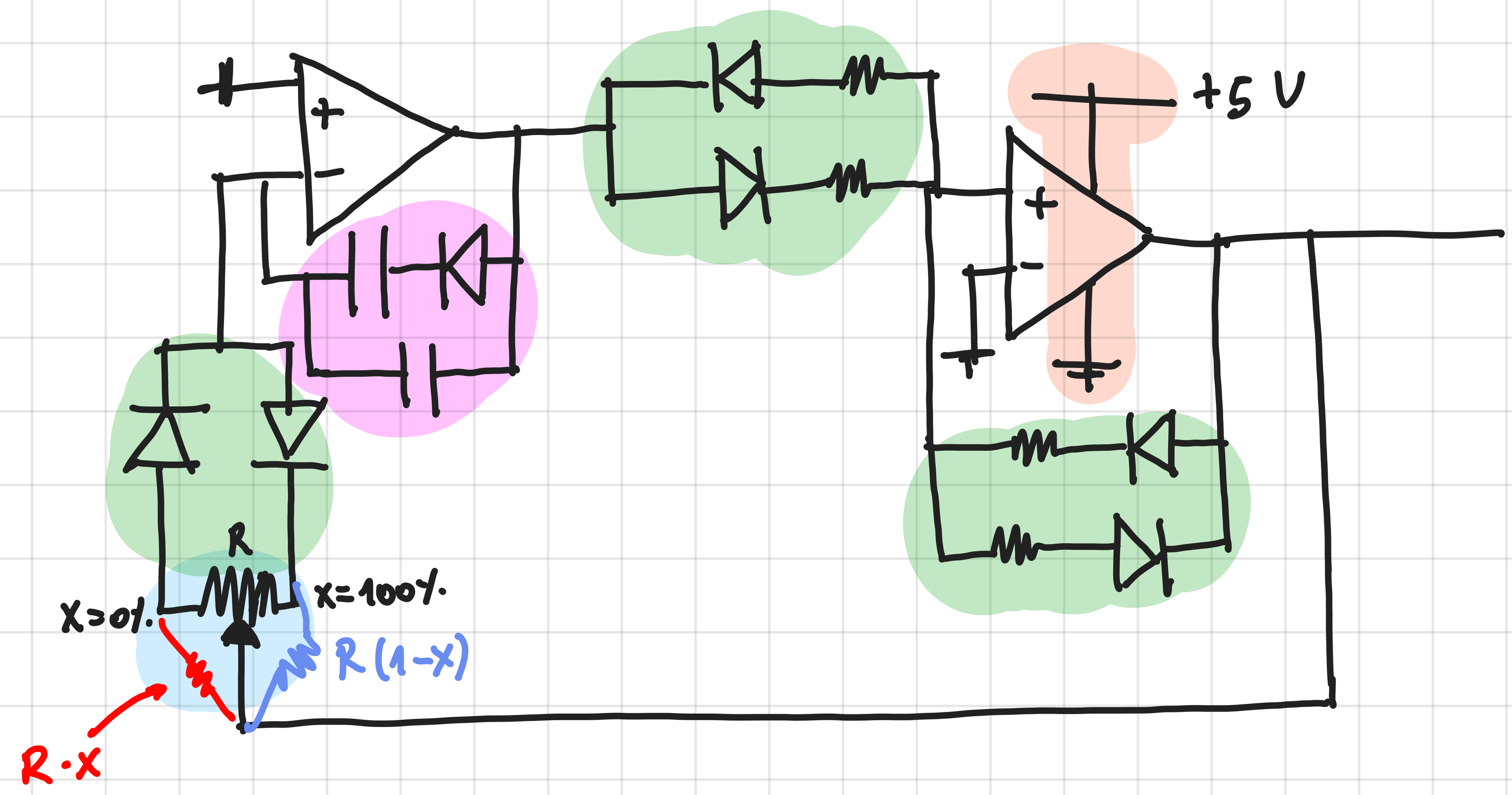
ex. Now suppose we want to change V_{TH} and V_{TL} to make it for ex. non-symm.

We saw in the ex. that V_{TH} and V_{TL} depend on the resistors of the Schmitt trigger, so to have different V_{TH}, V_{TL} for symm. output $\pm 5V$ we can implement also here the diodes that allow us to pass to specific and different resistors, based on the direction of the current, that depends on the output.



⟶ . . . ⟶ Different thresholds ⟵ Otherwise we can use non symm. P.S.

ex. Playing with the different elements of a circuit can allow us to have a lot of design variability

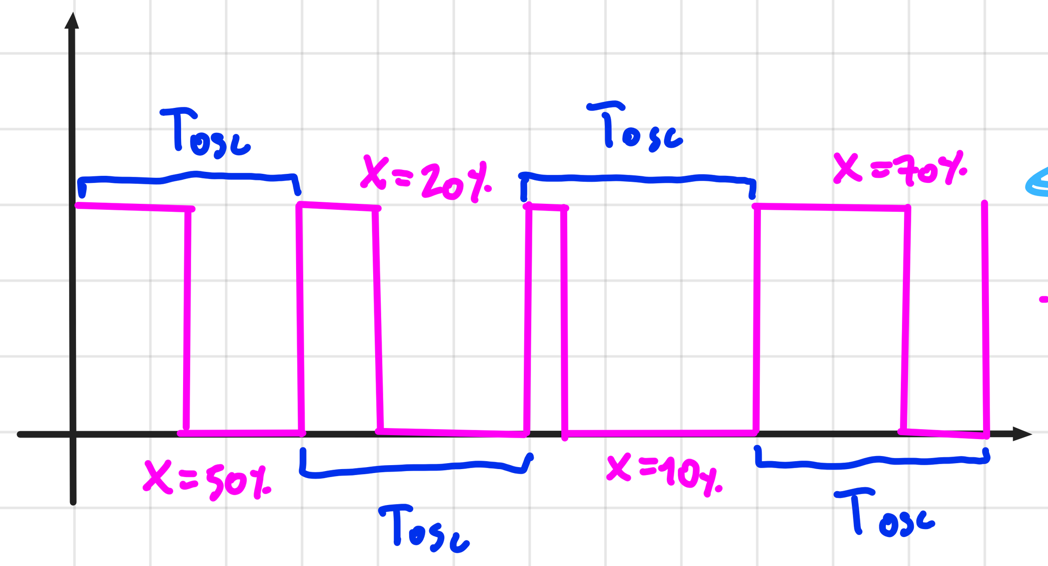


→ to allow the choice btw different resistors

→ Choice btw sum of C (parallel of C) or just one C ⇒ diff. slopes

→ potentiometer to have diff. resistors

→ non symm. P.S.

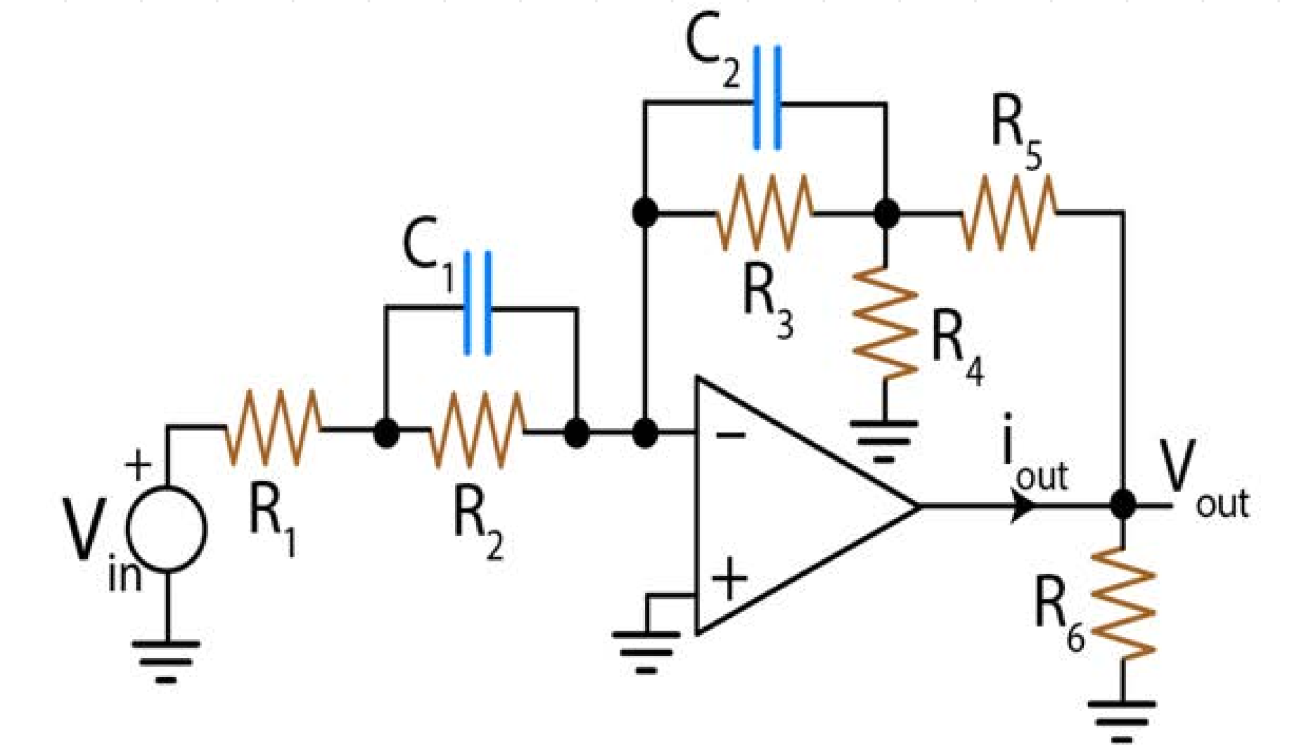


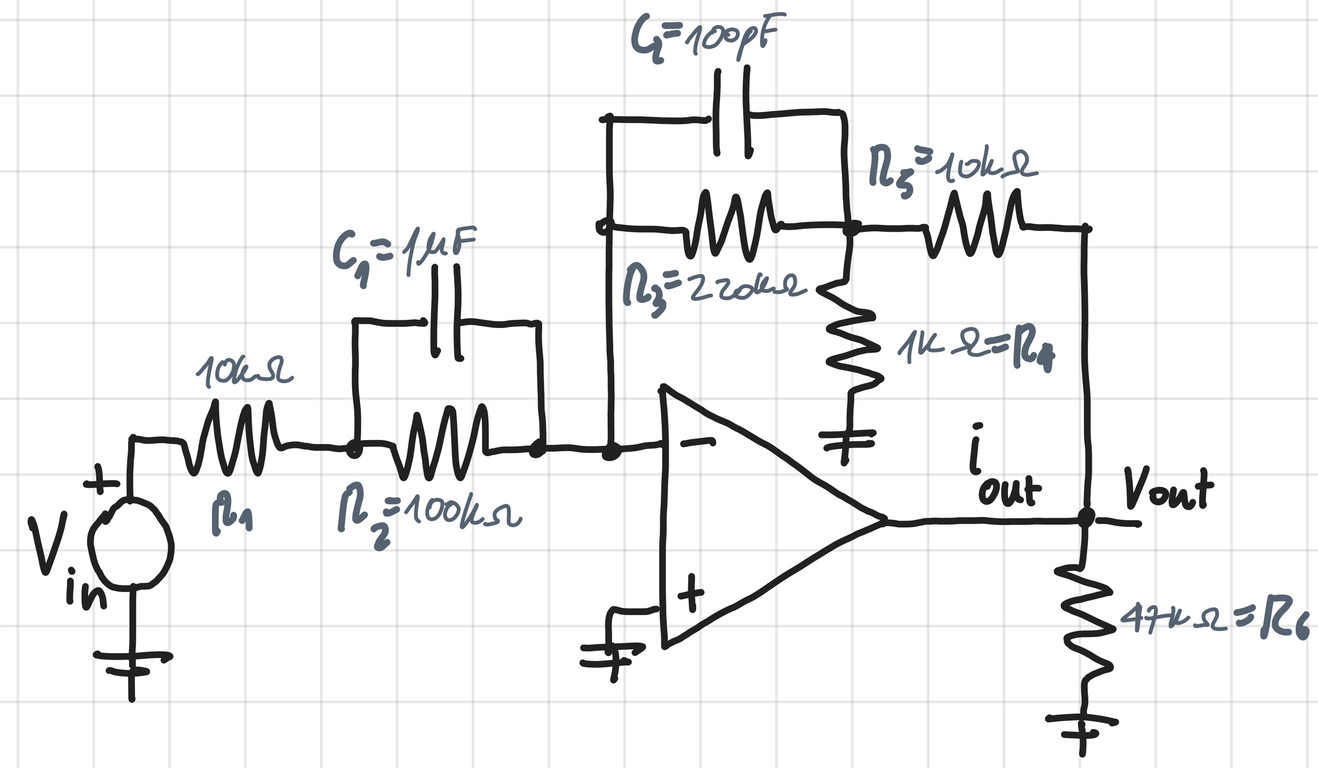
We can change the duty cycle but the f_{osc} will remain const. (period stays const.)

Because $T_{osc} \propto R_{ON} + R_{OFF} = R$

the sum is always the same

①



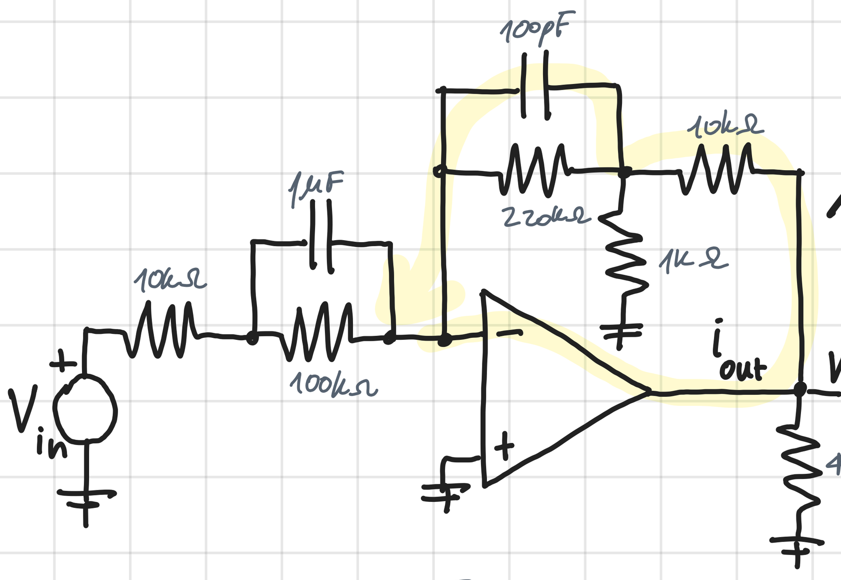


R_1=10kΩ, R_2=100kΩ, R_3=220kΩ, R_4=1kΩ, R_5=10kΩ, R_6=47kΩ, C_1=1μF, C_2=100pF.

a) Plot the ideal $|v_{out}(f)/v_{in}(f)|$ gain.

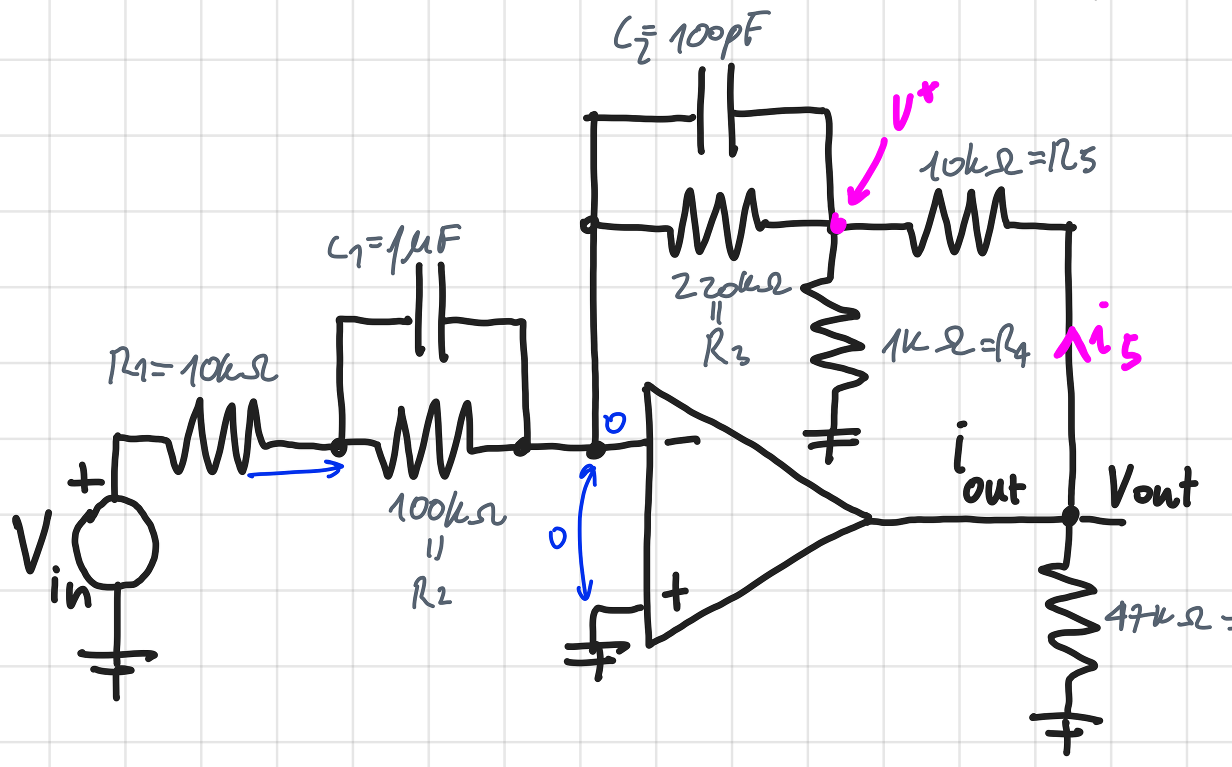
b) Compute i_{out} when V_{in}=-100mV.

↳ Negative or positive feedback



direction of the loop → negative feedback
↓
virtual ground

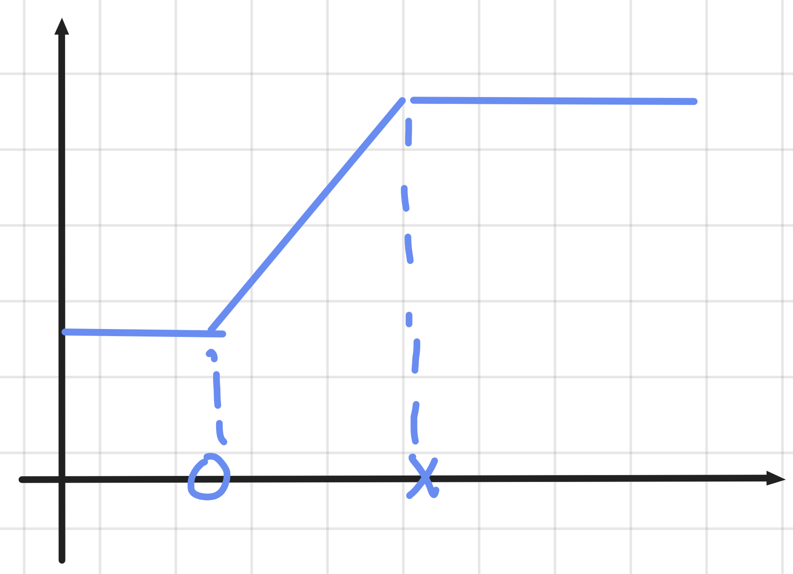
a)



feedback

① $G(0) = -\dfrac{R_F}{R_1+R_2}$

② $G(\infty) = -\dfrac{R_F}{R_1}$



↳ $i_{in}(f) = \dfrac{V_{in}}{R_1 + Z_1} =$ ① DC [0 Hz] $\dfrac{V_{in}}{R_1+R_2}$; ② AC [∞ Hz] $\dfrac{V_{in}}{R_1}$

↳ $V^*(0) = -\dfrac{V_{in}}{R_1+R_2} \cdot R_3$

$i_5(0) = \dfrac{V^*}{R_3} + \dfrac{V^*}{R_4}$

$\Rightarrow V_{out}(0) = V^* + R_5 \cdot i_5 = V^* + R_5 V^* \left(\dfrac{1}{R_3} + \dfrac{1}{R_4}\right) = -\dfrac{V_{in}}{R_1+R_2} \cdot R_3 \left[1 + R_5\left(\dfrac{1}{R_3} + \dfrac{1}{R_4}\right)\right]$

$R_3 \| R_4$ causes an increase in the gain

↳ ① $G(0) = \dfrac{V_{out}}{V_{in}}(0) = -\dfrac{R_3}{R_1+R_2}\left[1 + \dfrac{R_5}{R_3\|R_4}\right] = -\dfrac{220k}{110k}\left[1 + \dfrac{10k}{1k}\right] = -22$

↳ ② $G(\infty) = \dfrac{V_{out}}{V_{in}}(\infty) \to -\dfrac{R_5}{R_1} = -1$

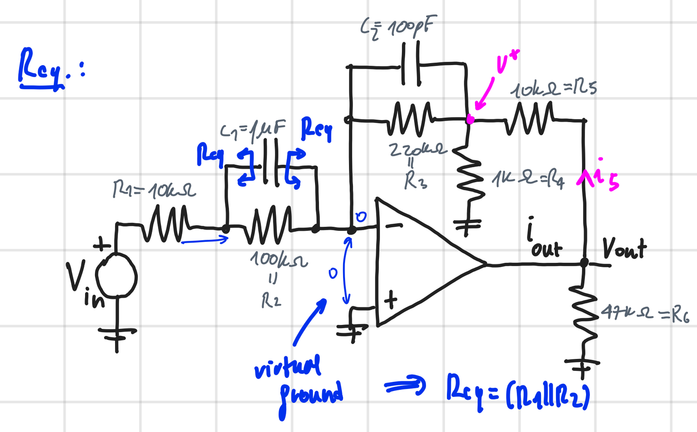
• Poles and zeros:

for C_1

• $pole_1 = \dfrac{1}{2\pi C_1 (R_2 \| R_1)} = \dfrac{1}{2\pi 1\mu (10k \| 100k)} = 18 Hz$

• $zero_1 = \dfrac{1}{2\pi C_1 R_2} = 1.6 Hz$

Req.:

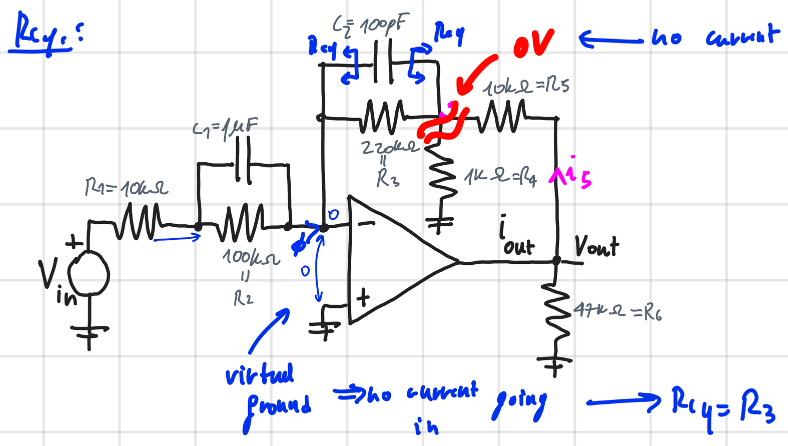


for C_2

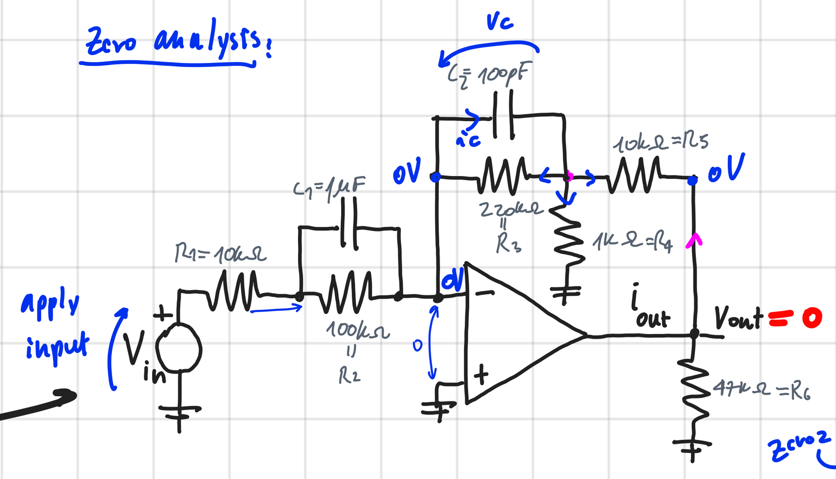
• $pole_2 = \dfrac{1}{2\pi C_2 R_3} = 7.2 kHz$

• $zero_2 = \dfrac{1}{2\pi C_2 (R_3 \| R_4 \| R_5)} = 1.8 MHz$

Req.:



Zero analysis:

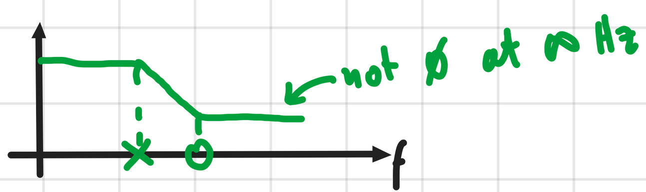


$\to i_C = \dfrac{V_C}{\frac{1}{sC_2}} = -\dfrac{V_C}{R_3} - \dfrac{V_C}{R_4} - \dfrac{V_C}{R_5} = -\dfrac{V_C (R_4R_5 + R_3R_5 + R_3R_4)}{R_3 R_4 R_5}$

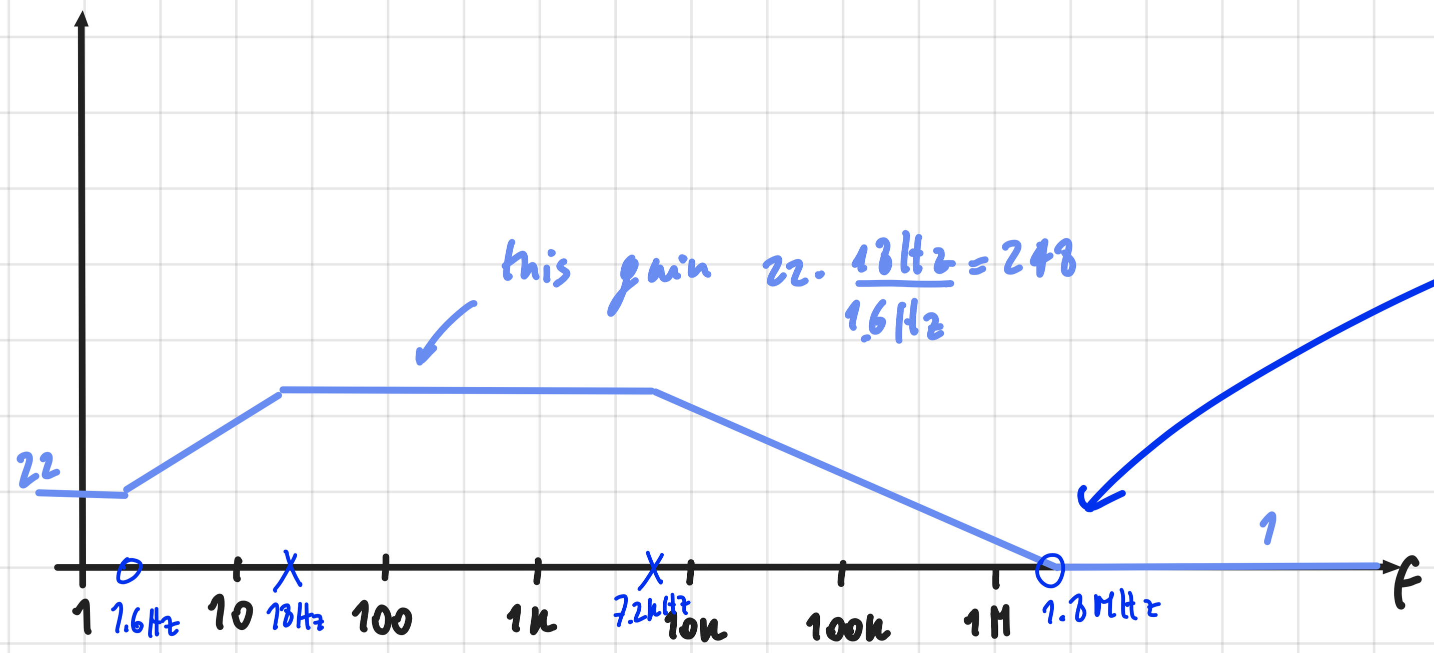
this eq. holds for:

zero → $s = \dfrac{\frac{1}{R_3} + \frac{1}{R_4} + \frac{1}{R_5}}{C_2} = \dfrac{1}{C_2 (R_3\|R_4\|R_5)}$

↳ the value at ∞ is not 0 → we have a zero too



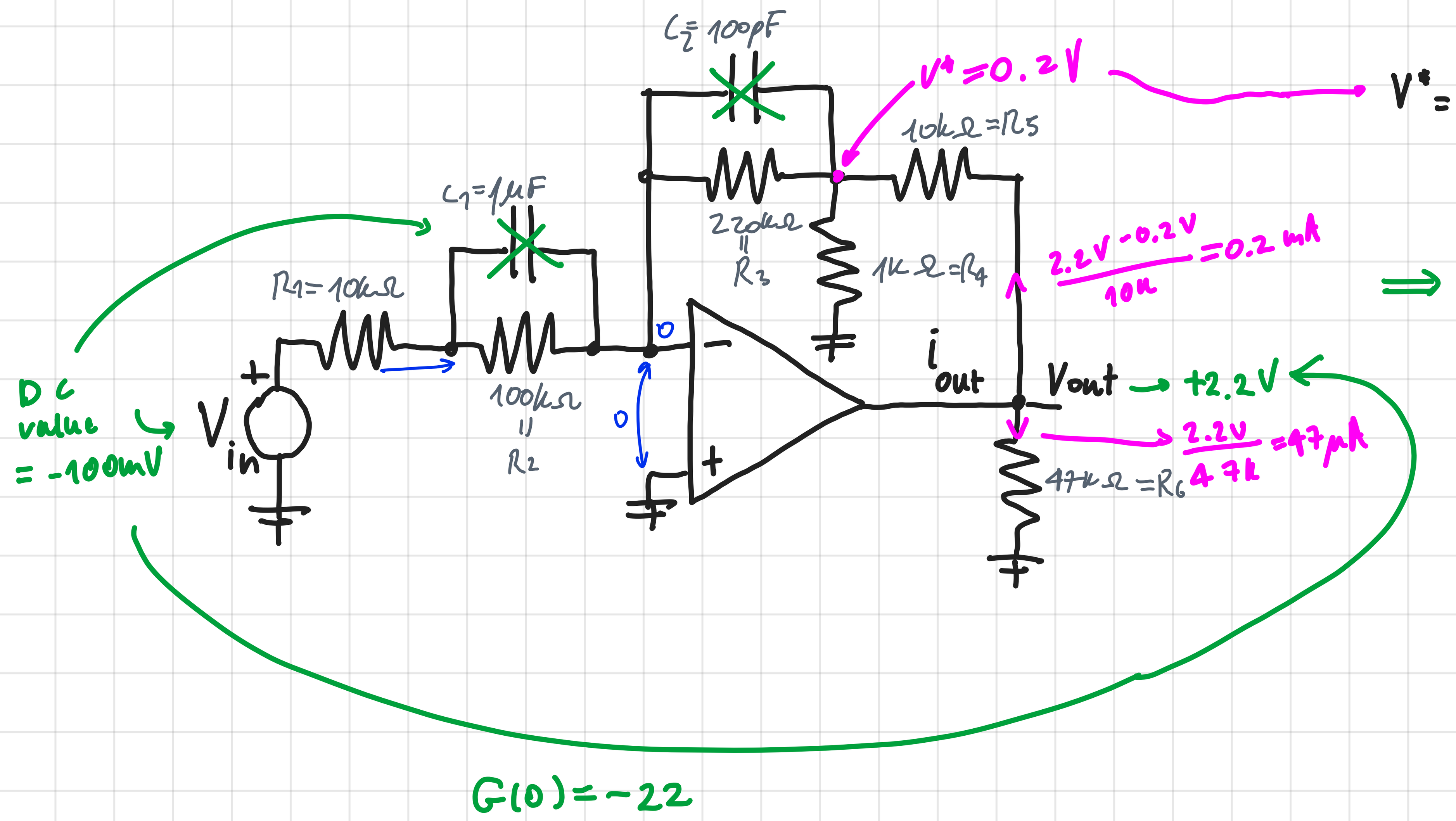
Bode diagram:



We could have also compute the zero like:

$\hookrightarrow zero_2 = \frac{248 \cdot 7.2\text{kHz}}{1} = 1.8\text{ MHz}$ ✓

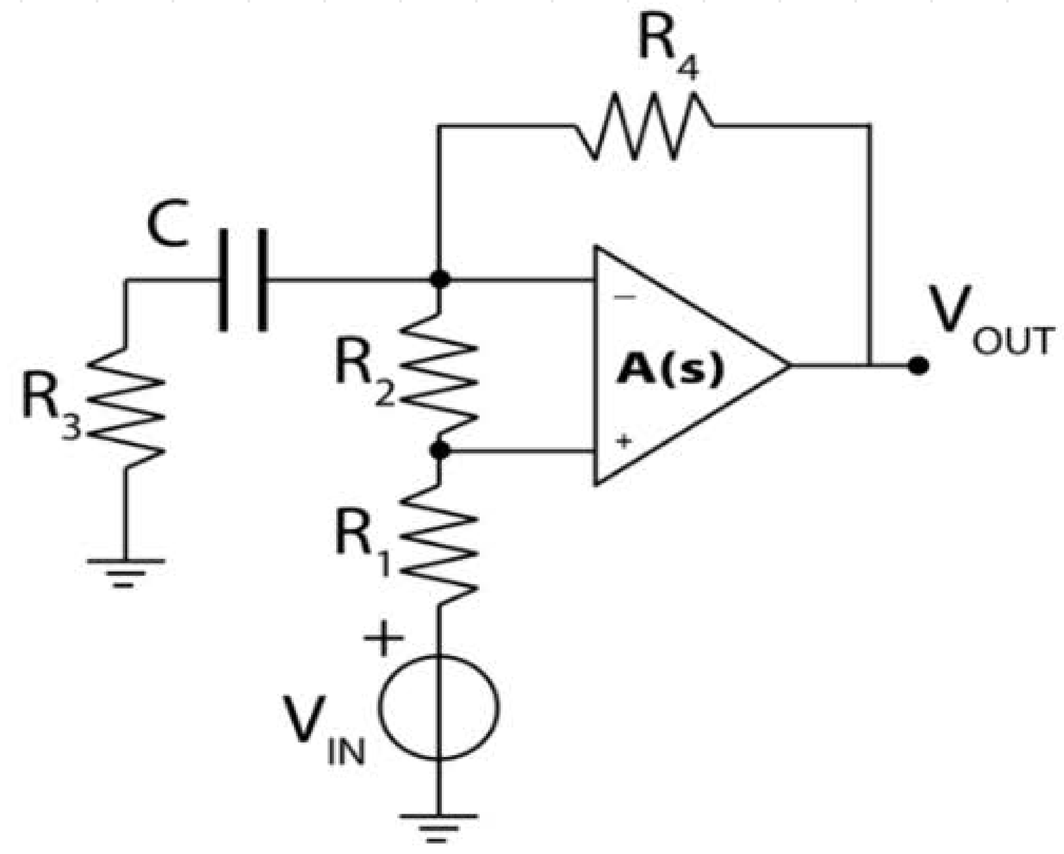
b)

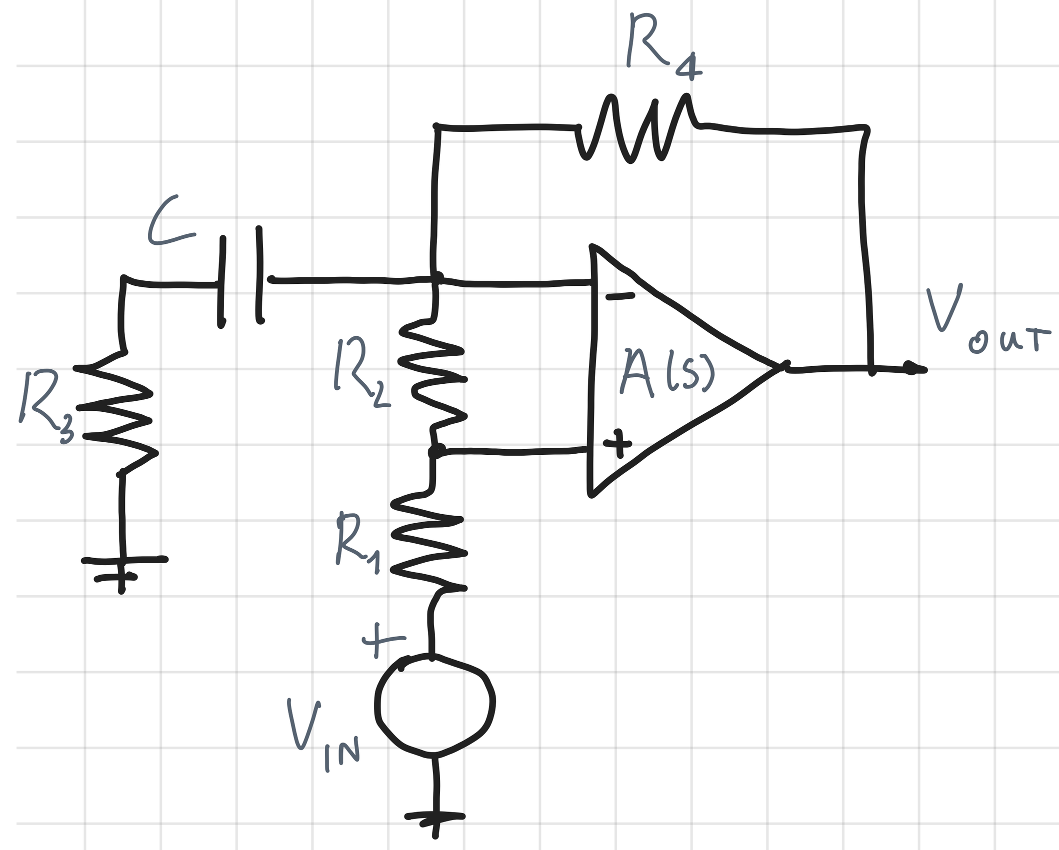


$V^+ = +100mV \cdot \frac{220k}{110k} = 0.2V$

$\Longrightarrow i_{out} = i_5 + i_6 = 0.2mA + 47\mu A = 247\mu A$

②





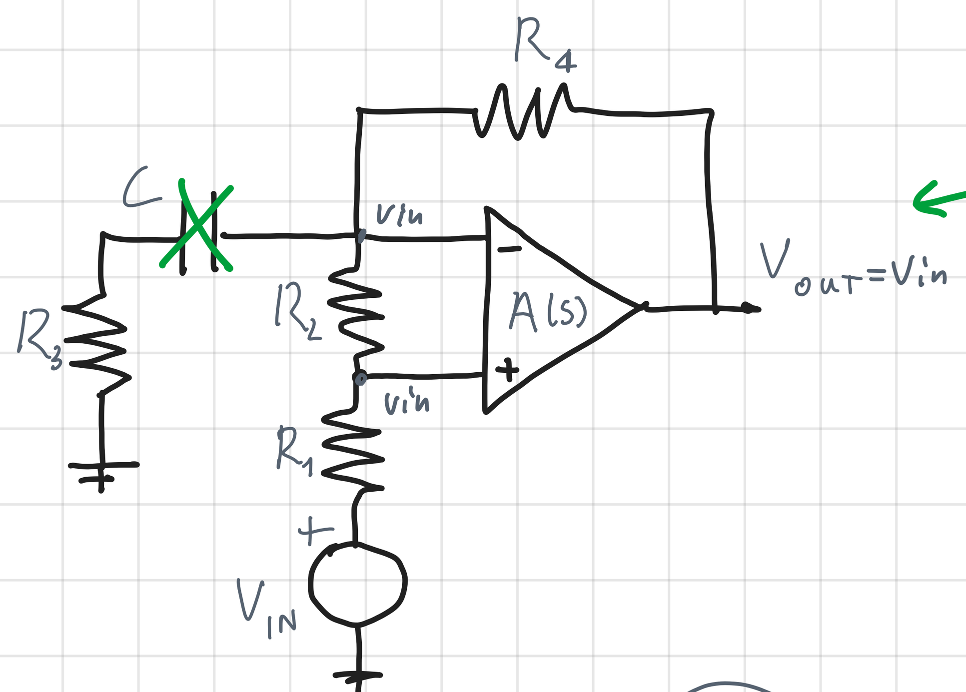
A_0=100dB, GBWP=100MHz.

R_1=22kΩ, R_2=1kΩ, R_3=1kΩ, R_4=47kΩ, C=1nF.

a) Plot the Bode diagram of the **ideal** and **real** $v_{OUT}(f)/v_{IN}(f)$.

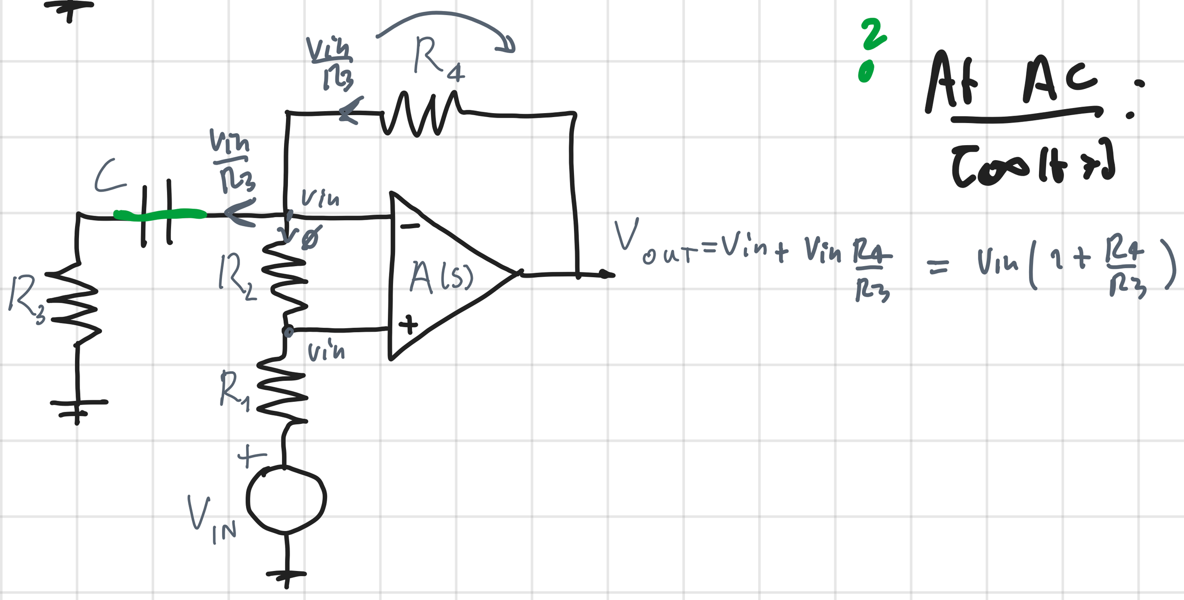
b) Compute the range of GBWP values that guarantees stability with a P.M. better than 90°.

a)



1. At DC [0 Hz]: $G(0) = \frac{V_{out}}{V_{in}}(0) = +1$

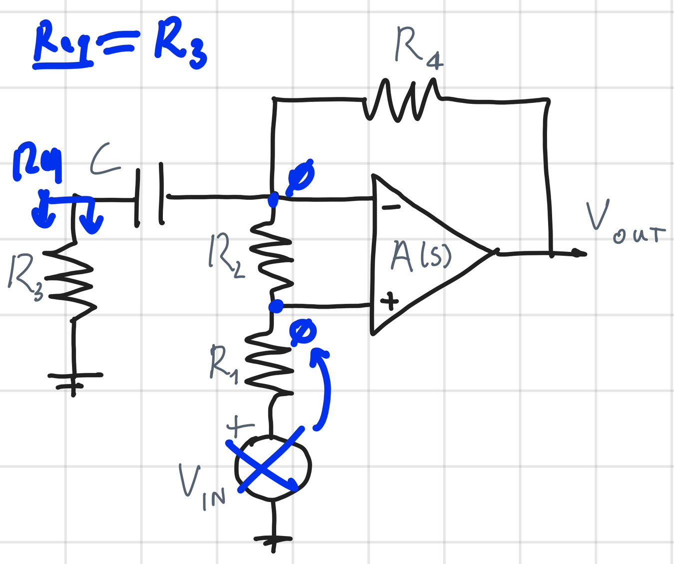
So there's a pole



2. At AC [∞ Hz]: $G(\infty) = \frac{V_{out}}{V_{in}}(\infty) = \left(1 + \frac{R_4}{R_3}\right) = +48$

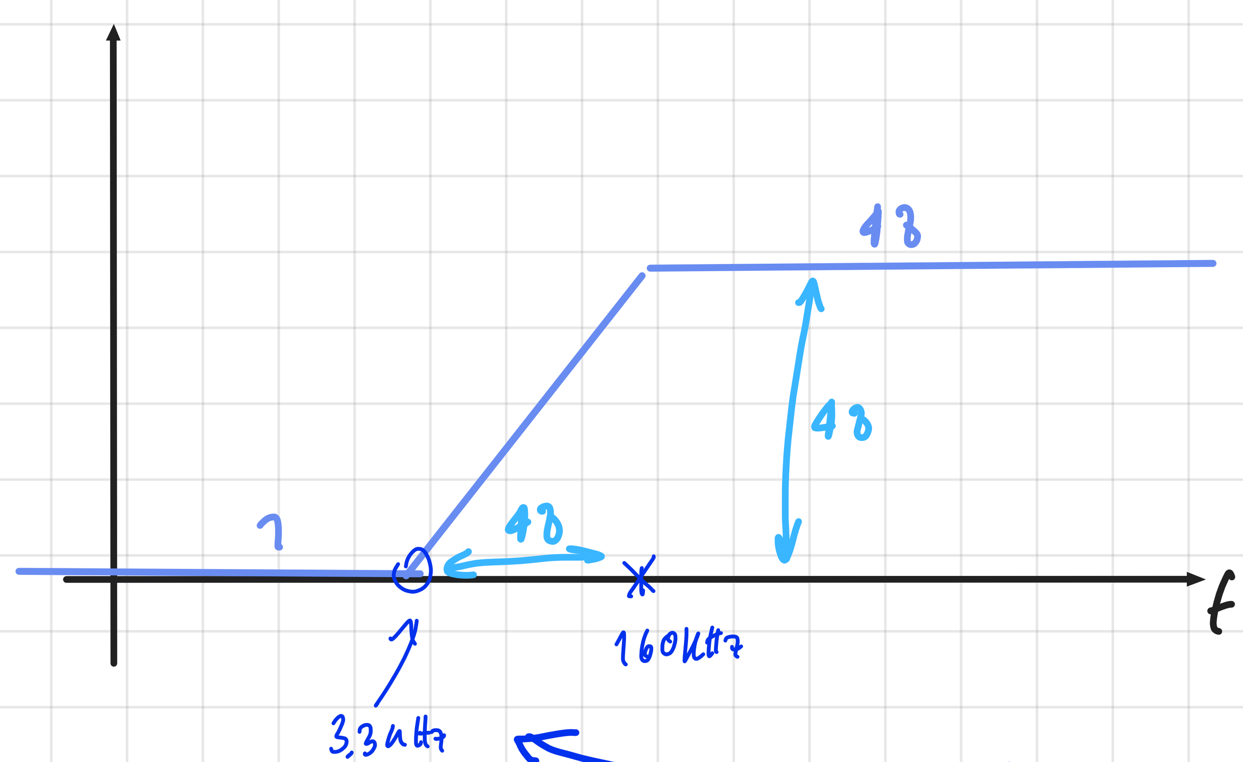
• Pole and zero:

$R_{eq} = R_3$



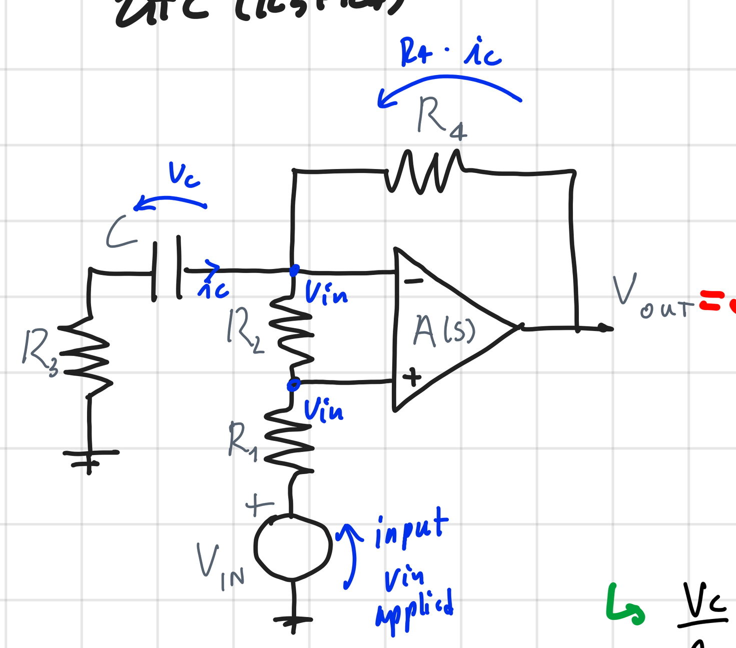
• $pole = \frac{1}{2\pi C R_3} = \frac{1M}{2\pi} = 160\ KHz$

Bode diagram:



We computed the zero graphically but also from circuit analysis

• $zero = \frac{1}{2\pi C(R_3+R_4)} = 3.3\ kHz$



Can Vout be 0?

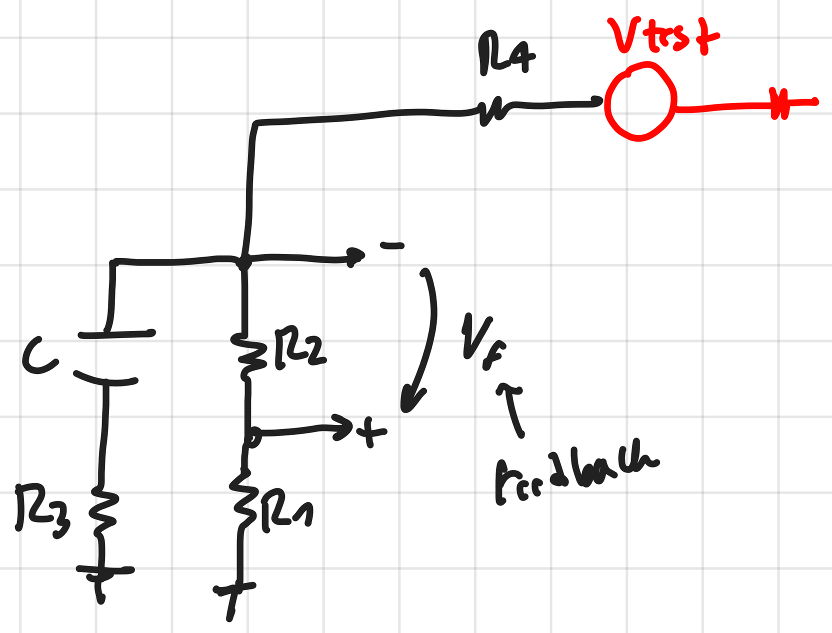
$i_c = \frac{1}{sC}$

↳ $\frac{V_c}{\frac{1}{sC}}(R_3+R_4) + V_c = 0$

↳ $sC(R_3+R_4) + 1 = 0$

↳ $s_{zero} = \frac{1}{C(R_3+R_4)}$

b) Gloop analysis:



• DC → C open

$$\beta(0) = \frac{V_f}{V_{test}}(0) = -\frac{R_2}{R_2+R_1+R_4} = -\frac{1k}{22k+47k} = -\frac{1}{69}$$

↳ $\frac{1}{\beta}(0) = -69$

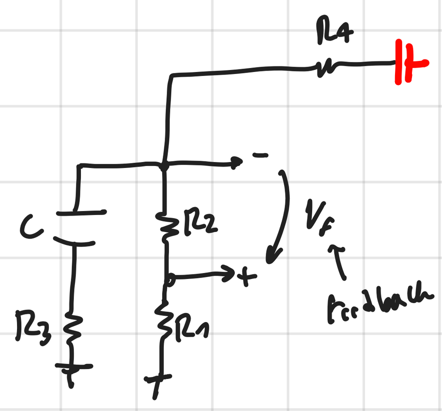
• AC → C close

$$\beta(\infty) = \frac{V_f}{V_{test}}(\infty) = -\frac{R_3 \| (R_1+R_2)}{[R_3 \| (R_1+R_2)]+R_4} \cdot \frac{R_2}{R_1+R_2} = -\frac{1k \| 23k}{1k\|23k+47k} \cdot \frac{1}{23} = -870 \cdot 10^{-6}$$

↳ $\frac{1}{\beta}(\infty) = -1151$

• Pole and zero

↳ Vtest grounded

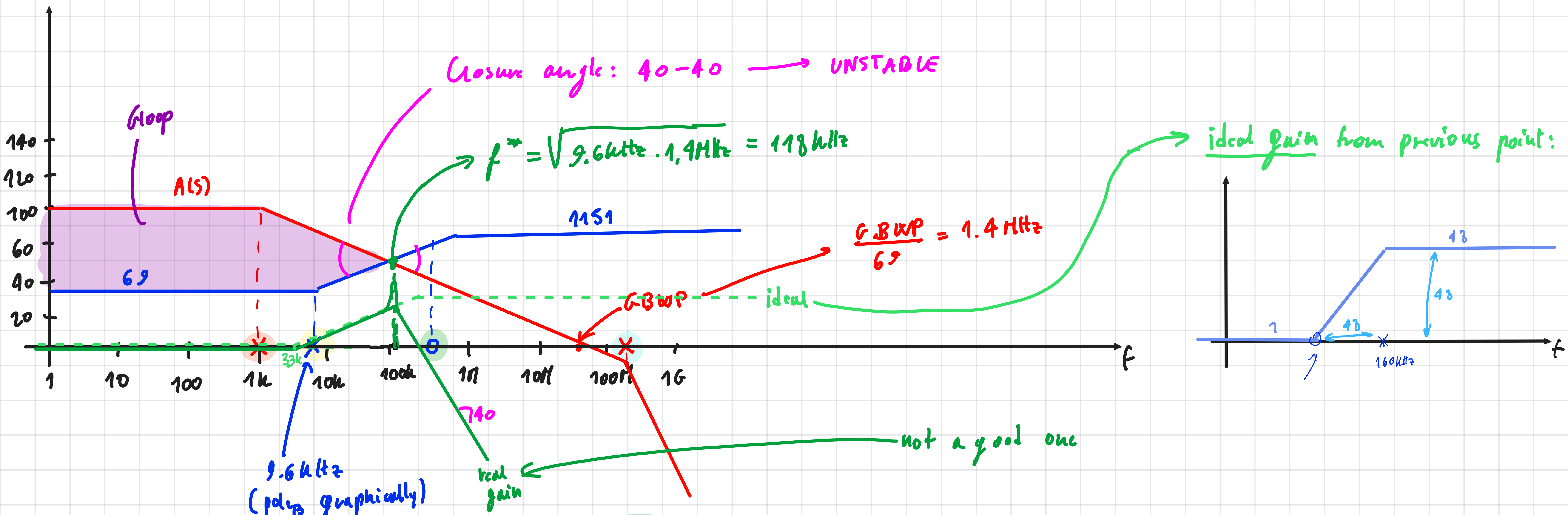


• $pole_\beta = \frac{1}{2\pi C[R_3+R_4 \| (R_1+R_2)]} = \dots$

• $zero_\beta = \frac{1}{2\pi C R_3} = 160\,kHz$

much easier too compute zero (then pole graphically)

Bode diagram:

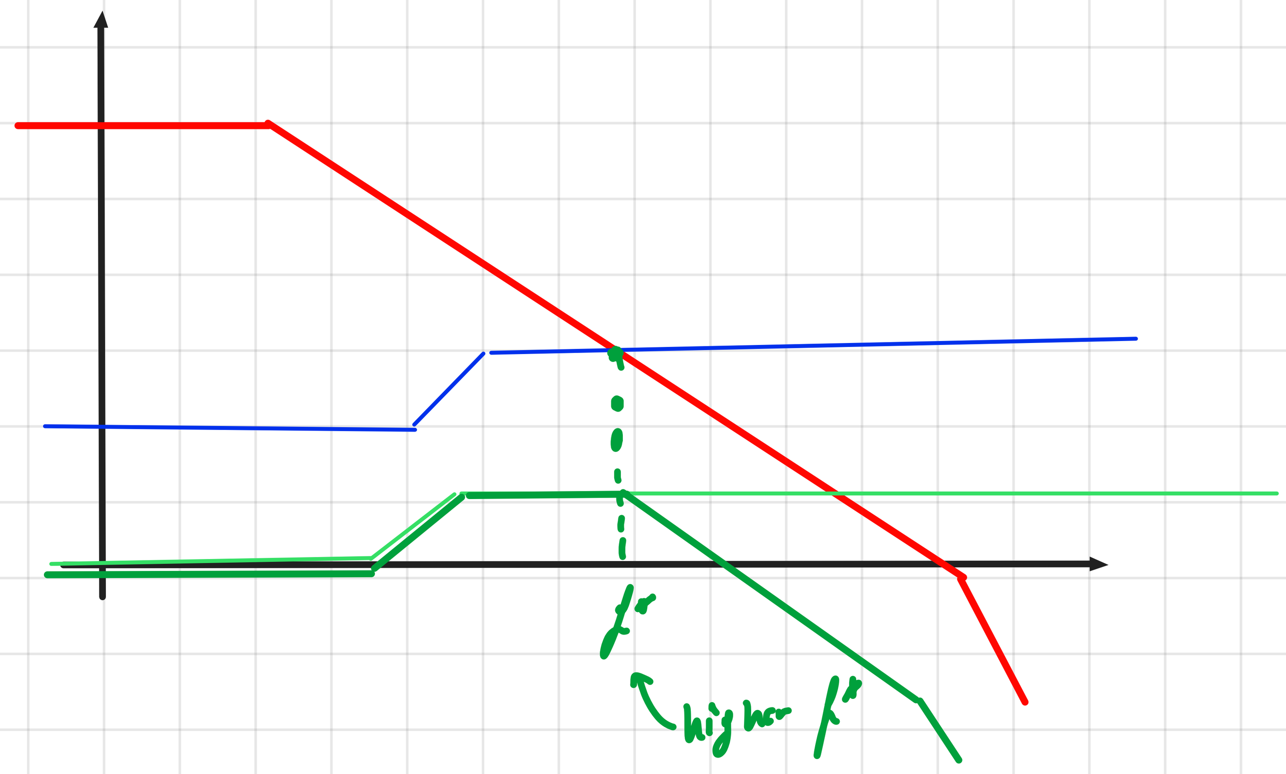


• Phase margin: $PM = 180° - 90° - 90° + \arctan\frac{f^*}{160k} - \phi = 0 + 36° = 36°$

ϕ: negligible

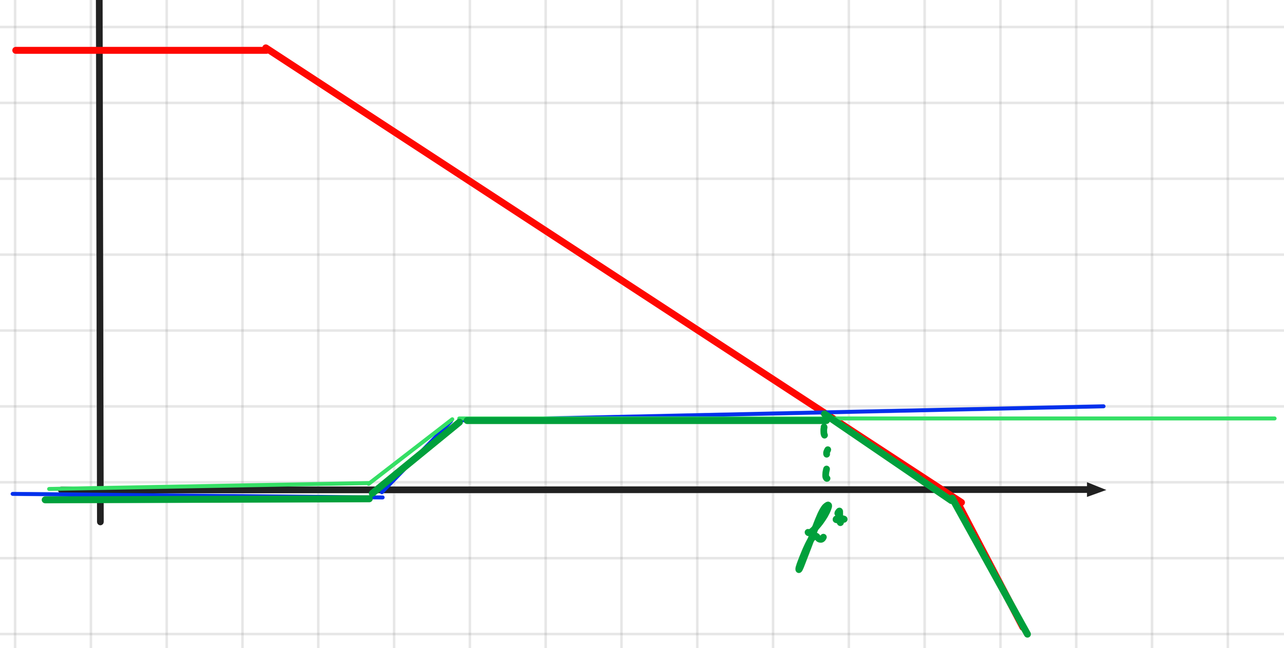
try to increase PM (but it's too late)

↳ A possible solution could be to buy another Op Amp → different A(s)

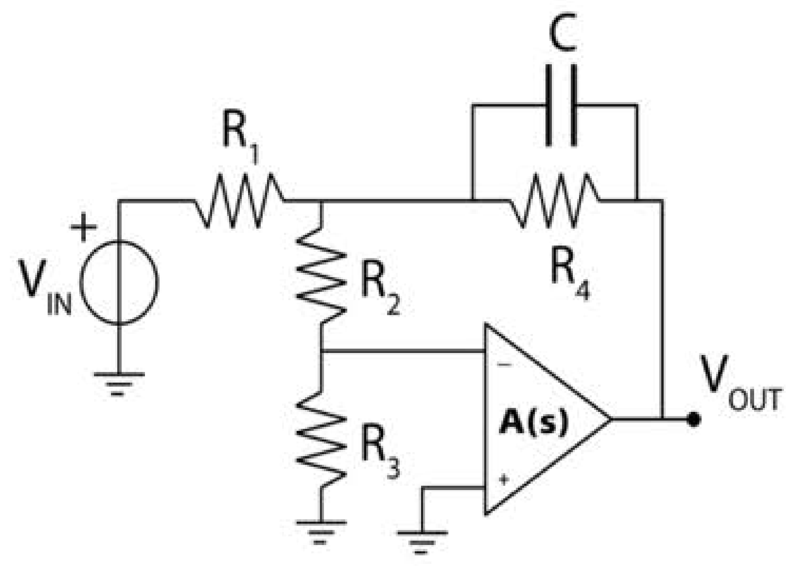


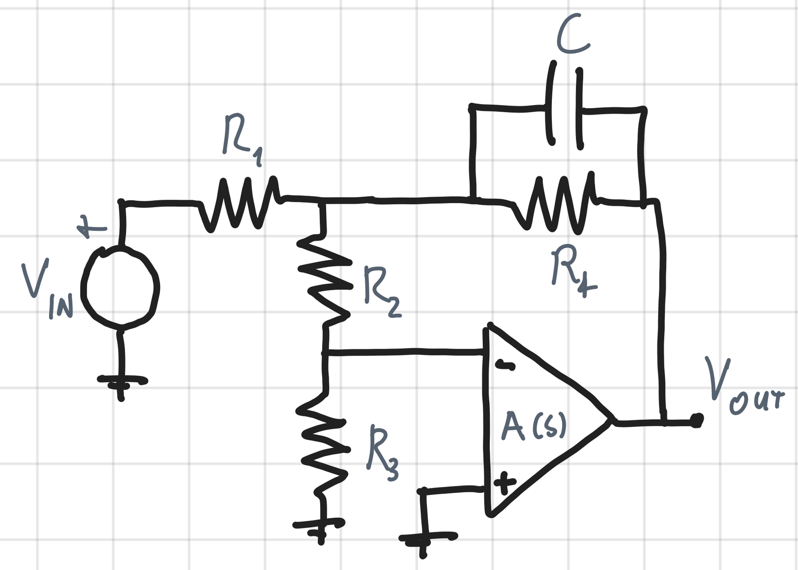
BUT NOT THAT feasible

↳ Or we can change $\frac{1}{\beta}$ → reduce the value by removing some resistors in order to match the ideal gain



③





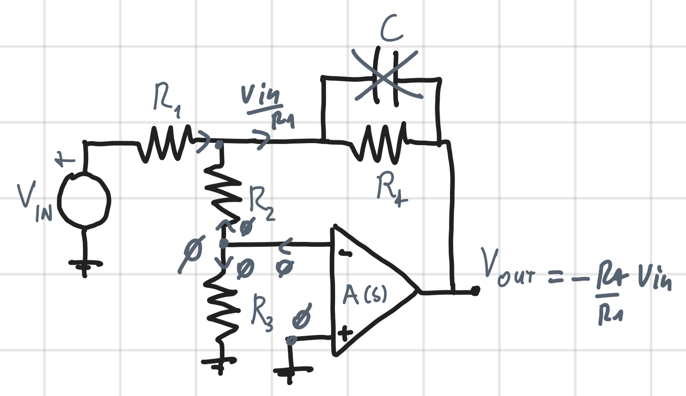
Compensated OpAmp: A_0=120dB, GBWP=10MHz, I_B=10nA, V_{OS}=5mV. R_1=47kΩ, R_2=33kΩ, R_3=22kΩ, R_4=680kΩ, C=330pF.

a) Plot the **real** $v_{out}(f)/v_{in}(f)$ gain and comment stability.

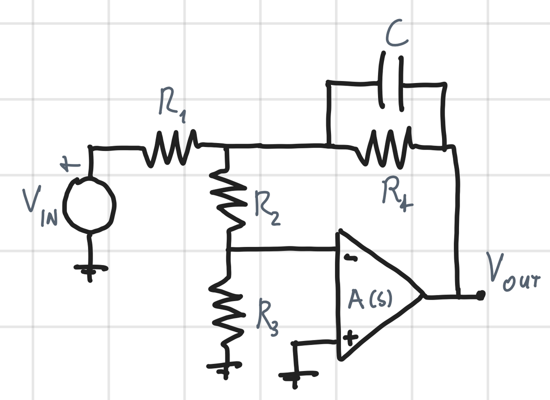
b) Compute the output static errors due to the OpAmp.

c) Let the OpAmp be a Norton Amplifier instead, with A_i=5, compute the $v_{out}(f)/v_{in}(f)$ gain.

a)

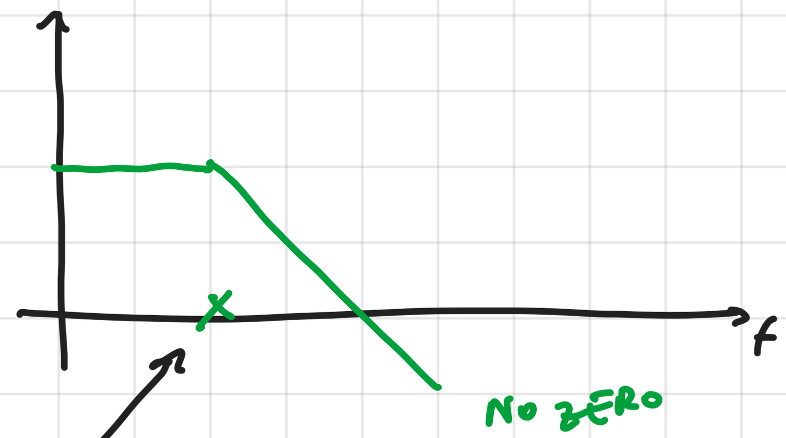


1. **DC** $\quad G(0) = -\frac{R_F}{R_1} = -\frac{R_4}{R_1} = -14.5$



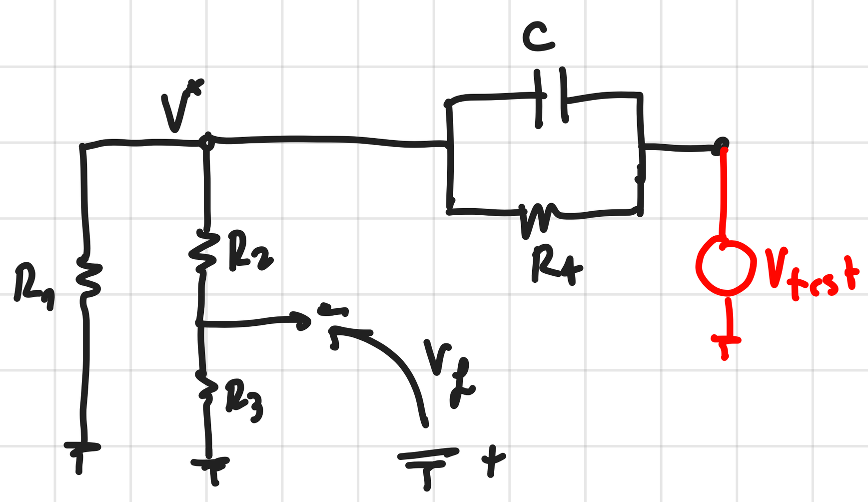
2. **AC** $\quad G(\infty) = \emptyset$

no zero



↳ Pole: $\quad \text{pole} = \frac{1}{2\pi C R_4} = 710\,\text{Hz}$

β computation:



• DC → C open

$$\beta(0) = -\frac{R_1 \parallel (R_2+R_3)}{R_1 \parallel (R_2+R_3) + R_4} \cdot \frac{R_3}{R_3+R_2} = -0.014 \rightarrow \frac{1}{\beta}(0) = -71$$

• AC → C close

$$\beta(\infty) = -\frac{R_3}{R_3+R_2} = -0.4 \rightarrow \frac{1}{\beta}(\infty) = 2.5$$

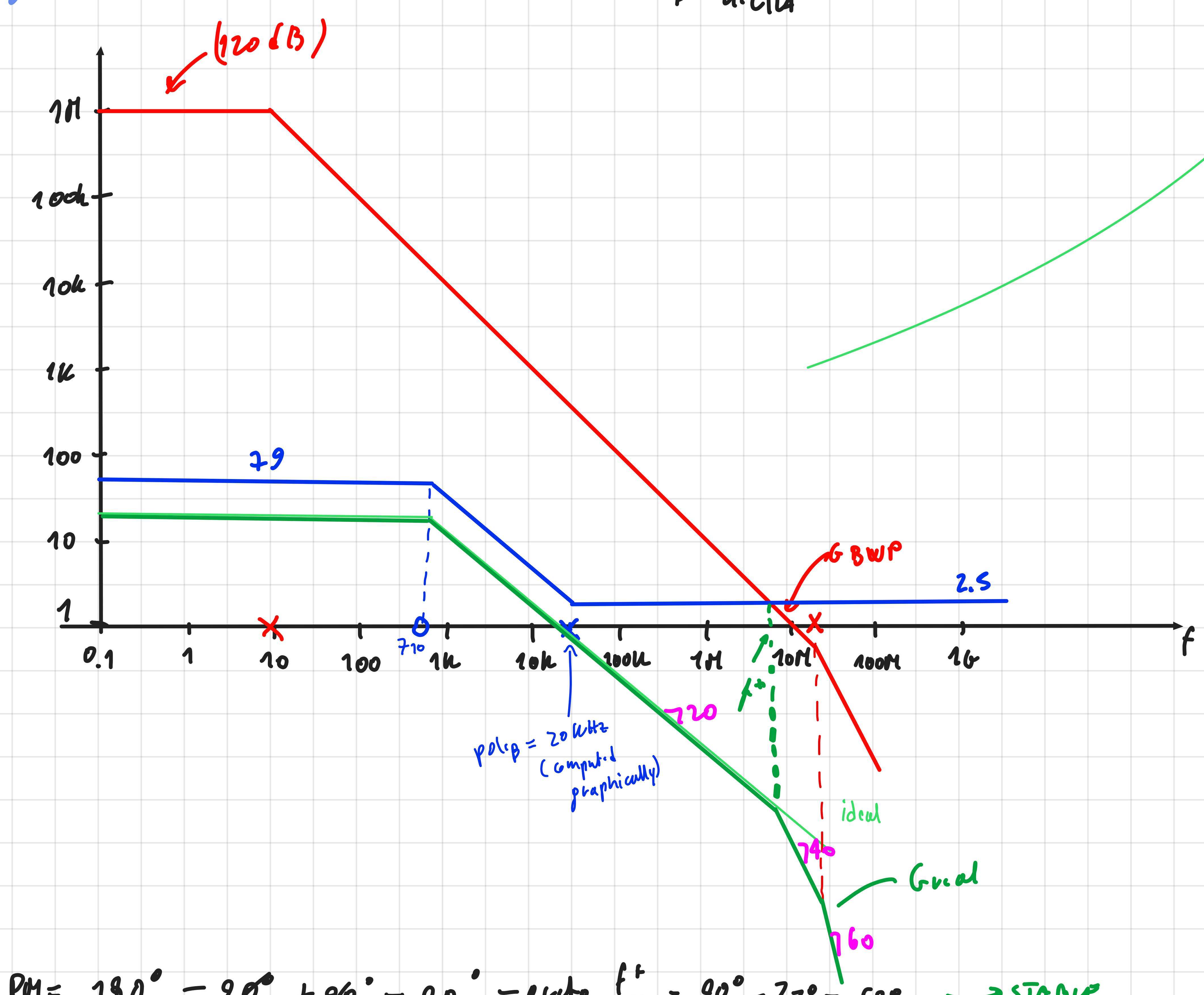
• Pole and zero: (No Vtest)

• $\text{pole}_\beta = \frac{1}{2\pi C \{R_4 \parallel [R_1 \parallel (R_2+R_3)]\}} = \dots$

• $\text{zero}_\beta = \frac{1}{2\pi C R_4} = 710\,\text{Hz}$ ← easier

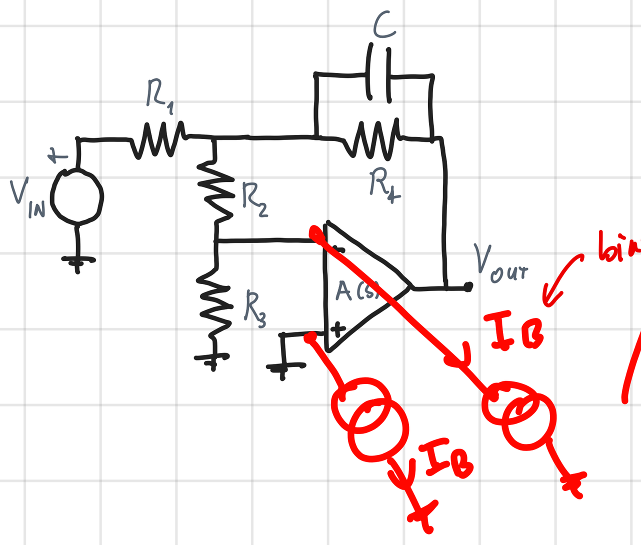
ideal gain

Bode diagram:



$$PM = 180° - 90° + 90° - 90° - \text{arctg}\frac{f^*}{f_2} = 90° - 22° = 68°$$ → STABLE

b) (From the part we skipped at lesson)



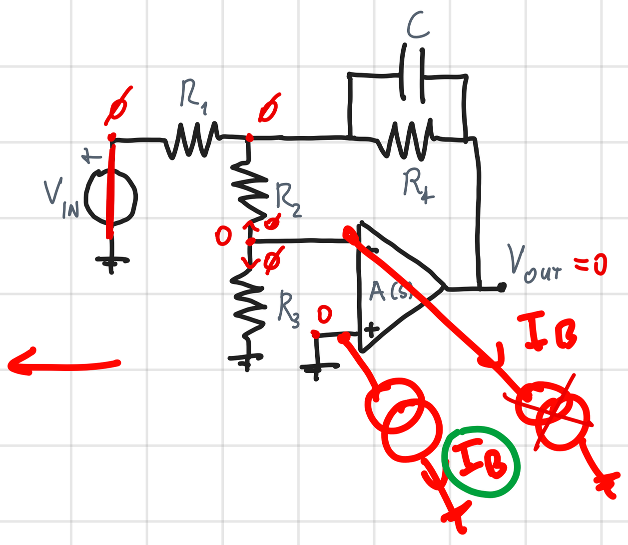
Although these current generator the input impedance are still ∞

↳ but there will be a leakage in the Op Amp

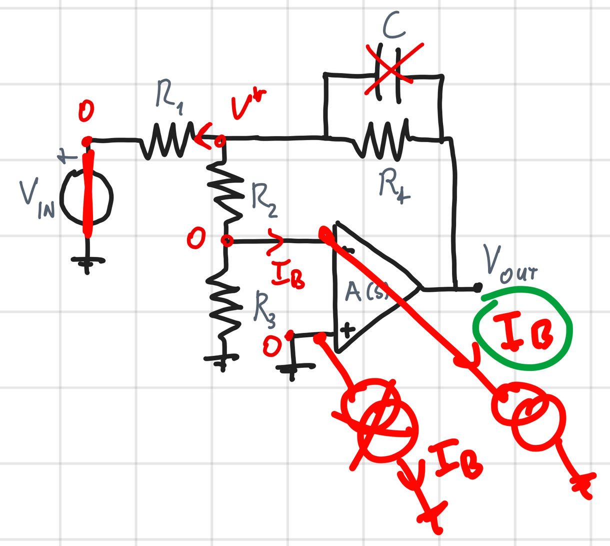
bias current → cause errors

↳ • Effect of I_B^+:

NO EFFECT



• Effect of I_B^-:



$\to V^+ = I_B^- R_2$

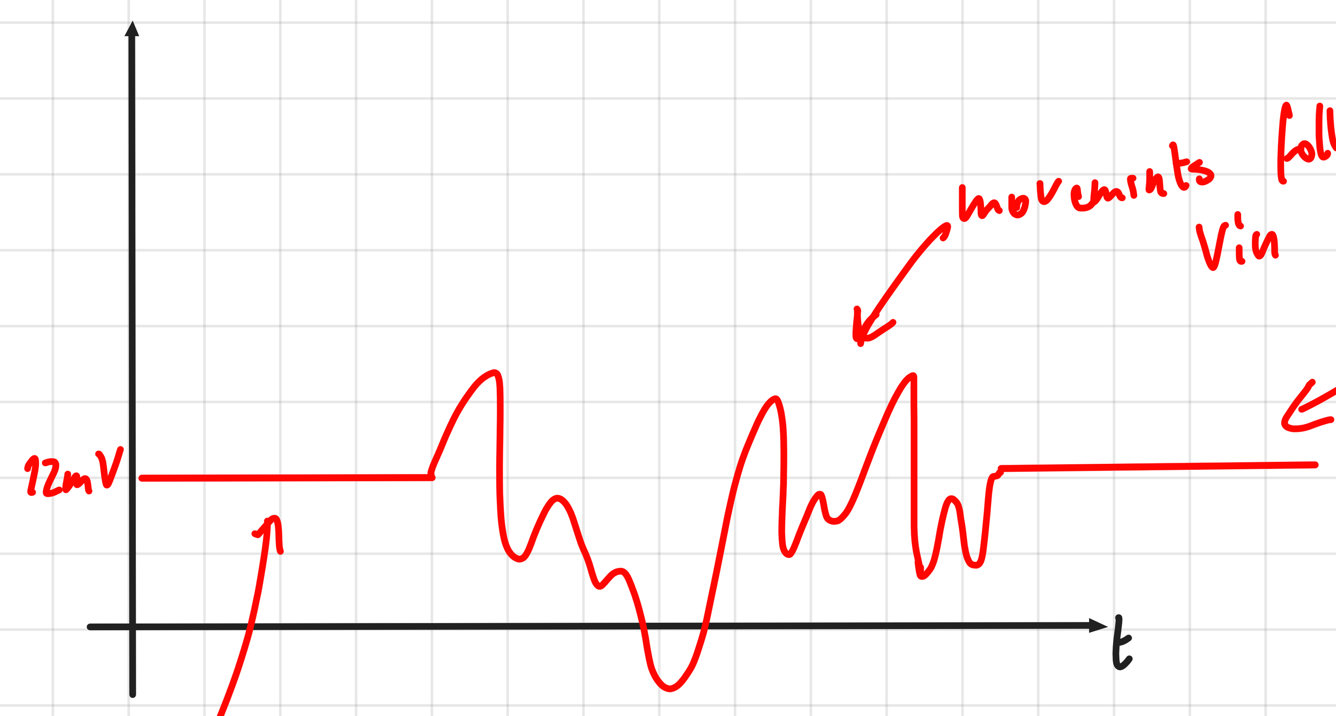
$I_1 = \frac{V^+}{R_1} = I_B^- \cdot \frac{R_2}{R_1}$

$I_2 = I_B^-$

$I_4 = I_1 + I_2 = I_B^- \left(1 + \frac{R_2}{R_1}\right)$

$V_{out} = R_4 \cdot I_B^- \left(1 + \frac{R_2}{R_1}\right) + I_B^- \cdot R_2 = 12\,mV$ (*)

↳ So if we look at the output of the OpAmp in time domain:

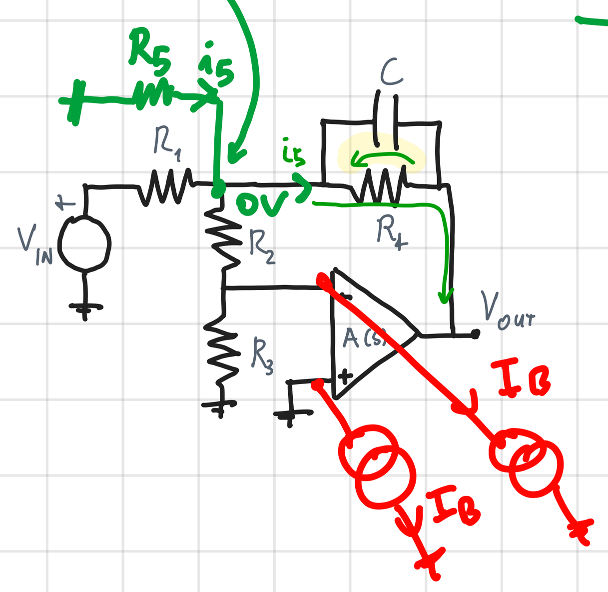


movements following Vin

but will have this OFFSET due to bias current

the output is not 0 when Vin is 0 but is at 12mV (*)

to remove it we could inject some current in this node



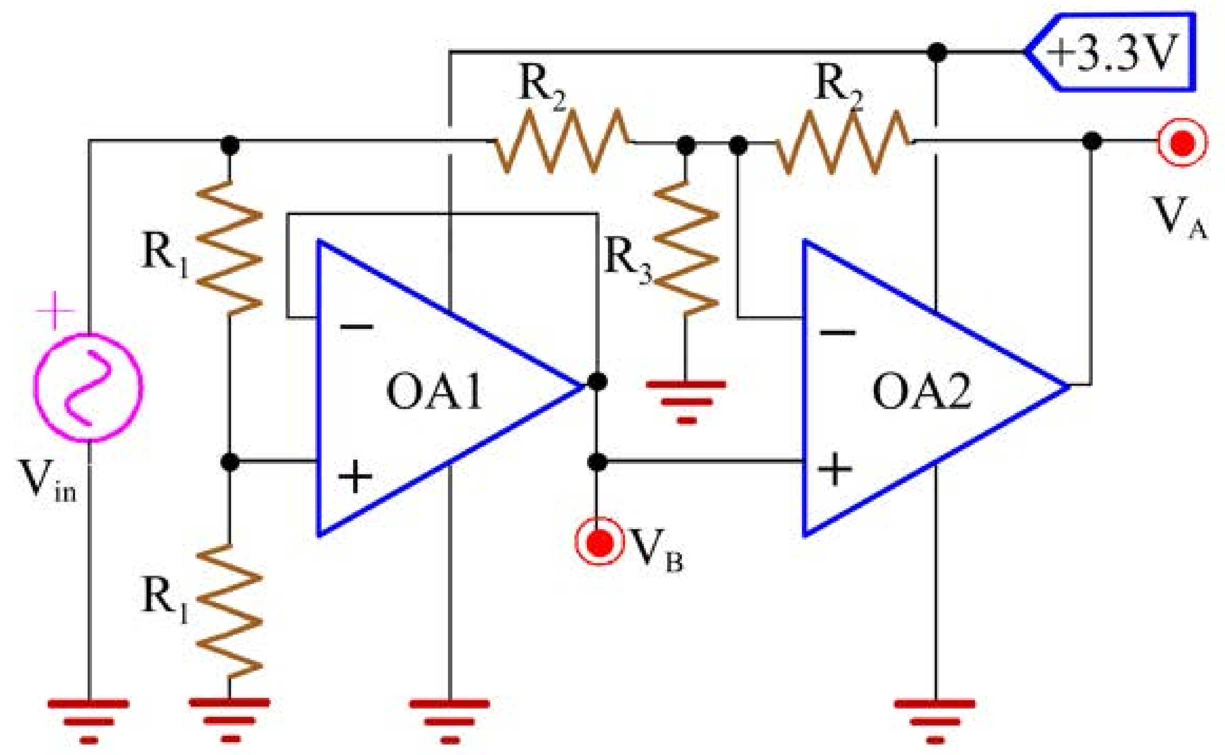
→ in such a way that i_S, when that node is ground (Vin=0), will flow on R4

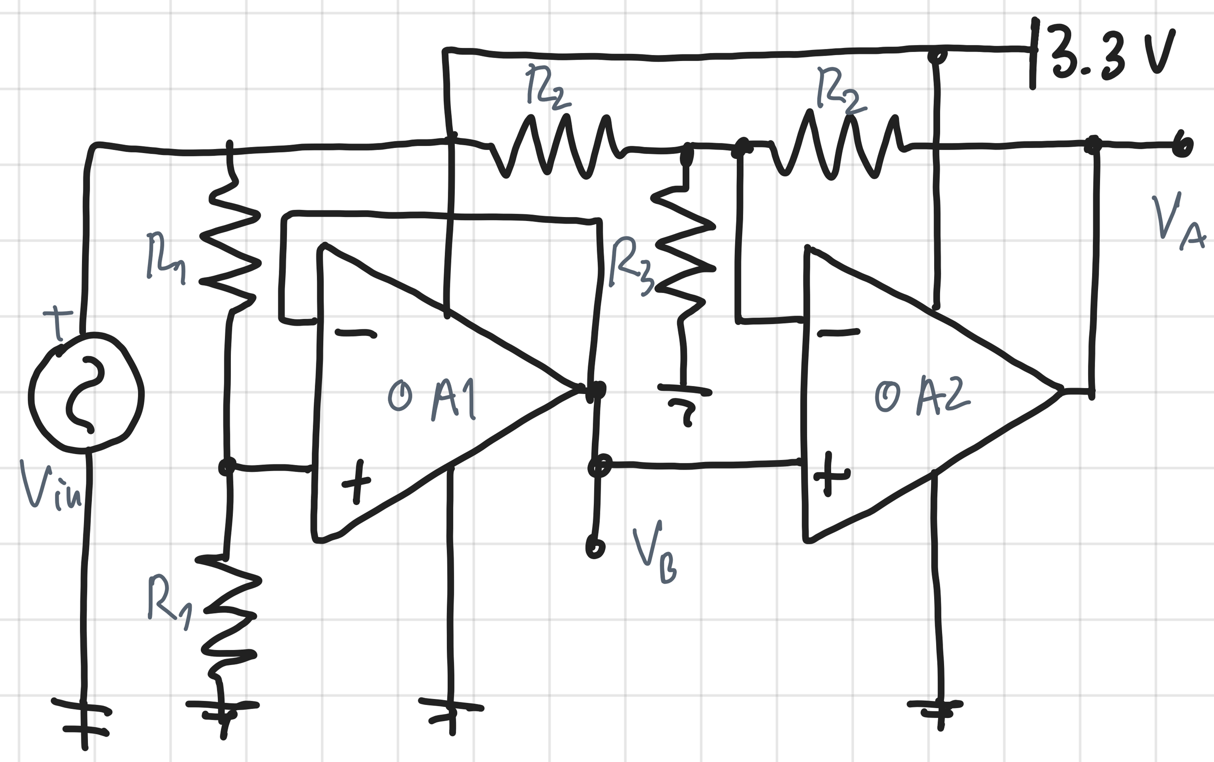
↳ giving a neg. contribution to Vout that will counter balance that offset of 12mV given by the bias

⇓

so that Vout=0 for Vin=0

4



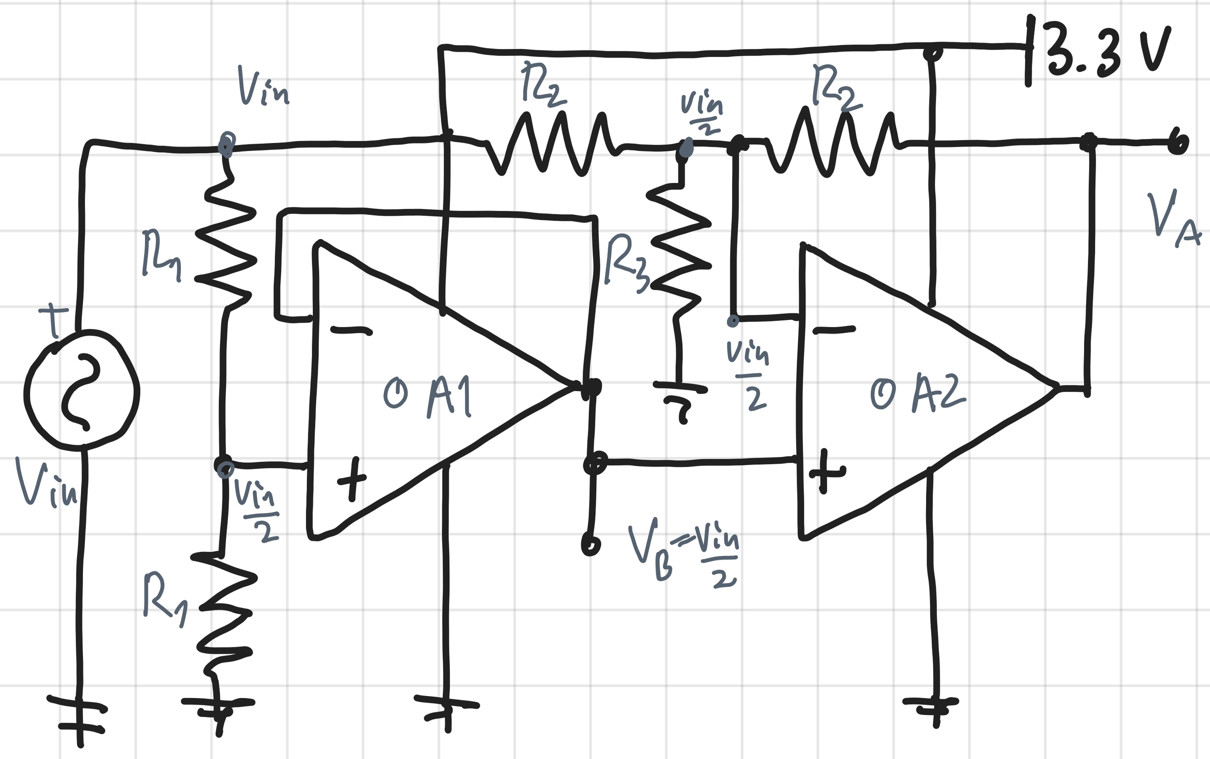


OpAmp with A_0=100dB and GBWP=100MHz. R_1=47kΩ, R_2=220kΩ, R_3=110kΩ.

a) Compute the **real** $v_A(f)/v_{in}(f)$ and $v_B(f)/v_{in}(f)$ gains and the input impedance.

b) Compute the output static error on V_A, due to I_B=10nA and V_{OS}=5mV of both OpAmps.

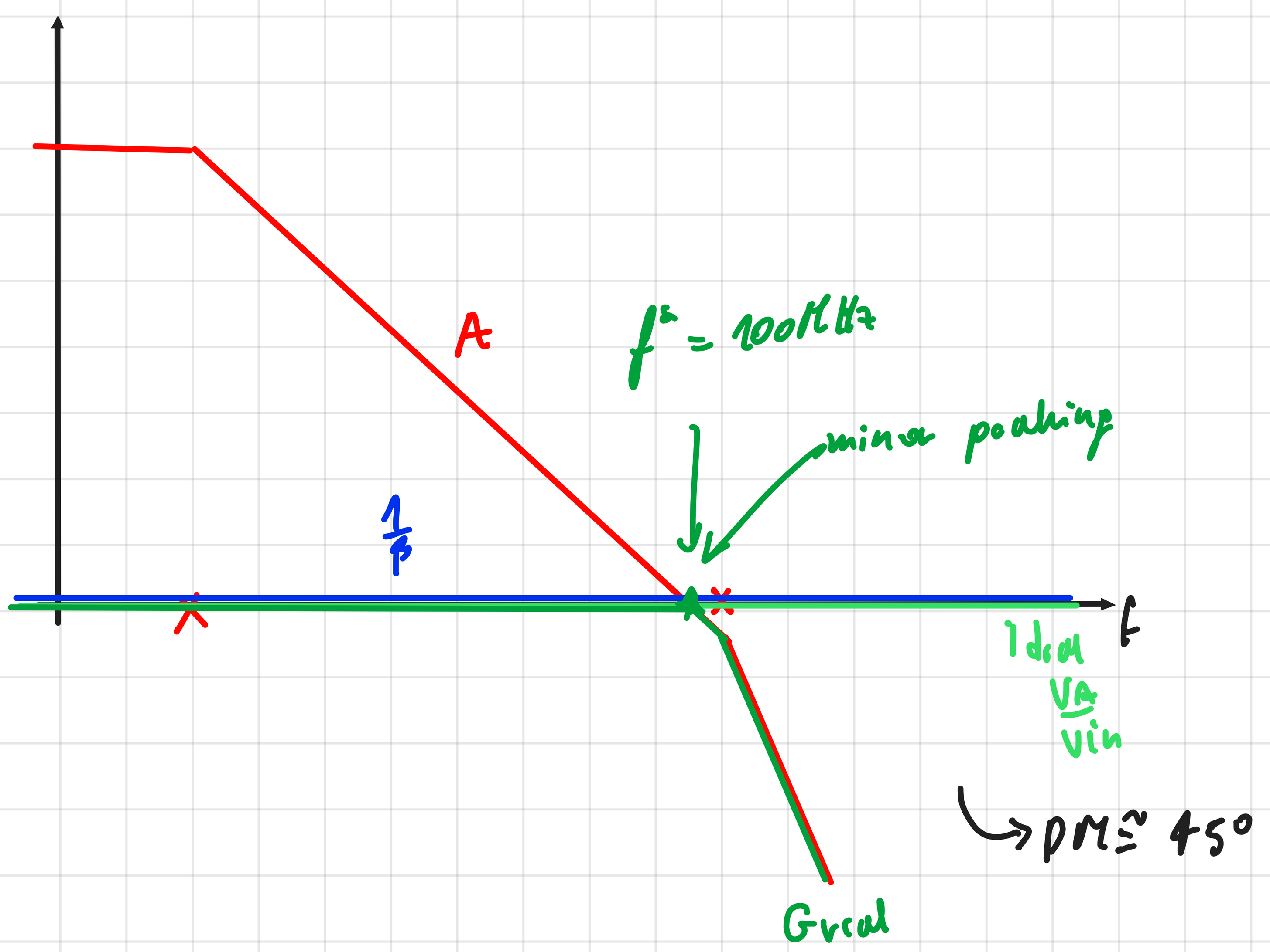
a)



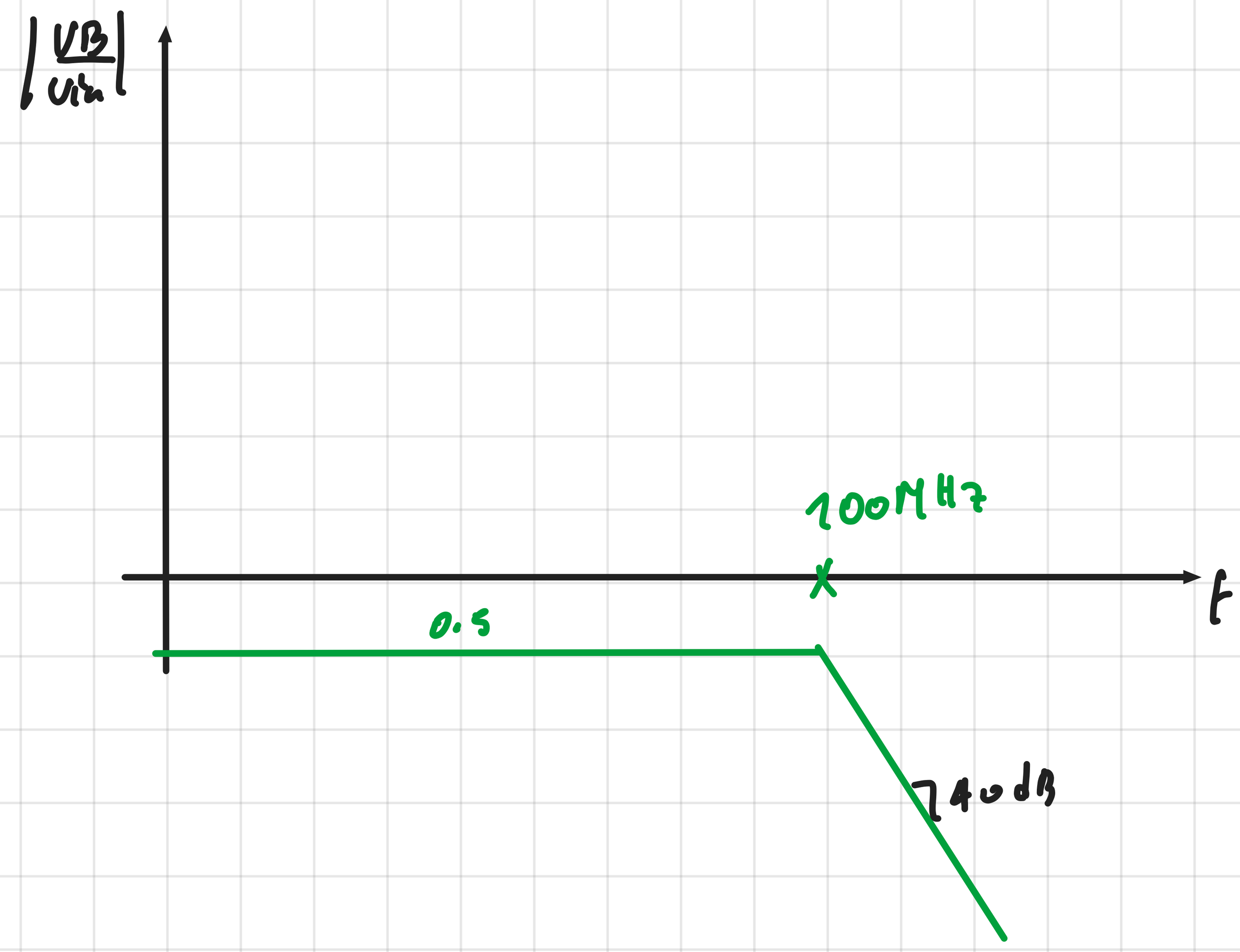
$$V_A = \left(\frac{\frac{V_{in}}{2}}{R_3} + \frac{\frac{V_{in}}{2} - V_{in}}{R_2}\right) R_2 + \frac{V_{in}}{2} = \frac{V_{in}}{2}\left[\left(\frac{R_2}{2R_3} - \frac{R_2}{R_2}\right) + 1\right]$$

$$\hookrightarrow Gain_{V_A} = \frac{V_A}{V_{in}} = \frac{1}{2}\left(\cancel{1} + \frac{R_2}{R_3} - \cancel{1}\right) = \frac{1}{2}\frac{R_2}{R_3} = 1 \quad \text{(BUFFER ACTION)}$$

Bode diagram:

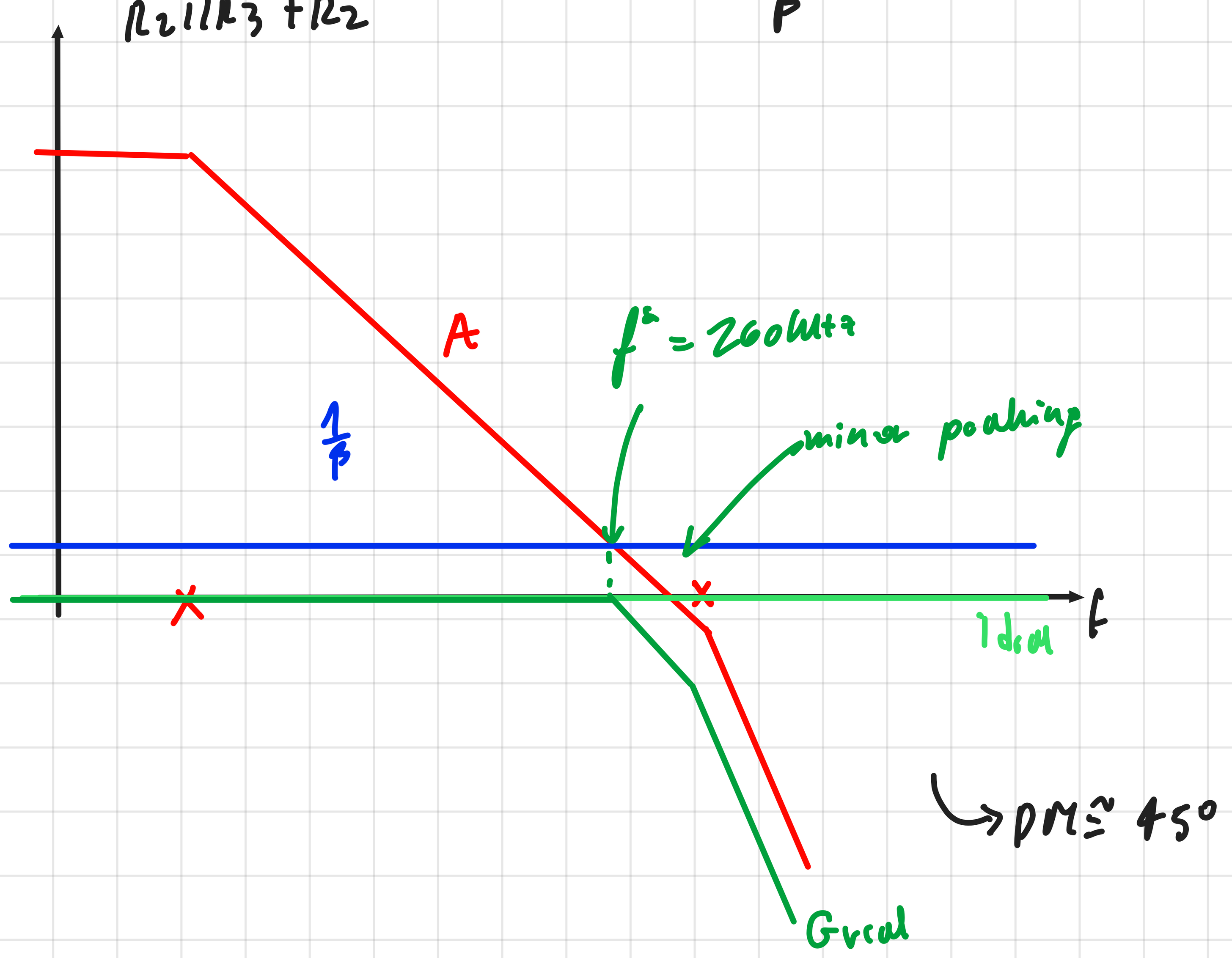


$$Gain_{V_B} = \frac{V_B}{V_{in}} = \frac{1}{2} = 0.5$$

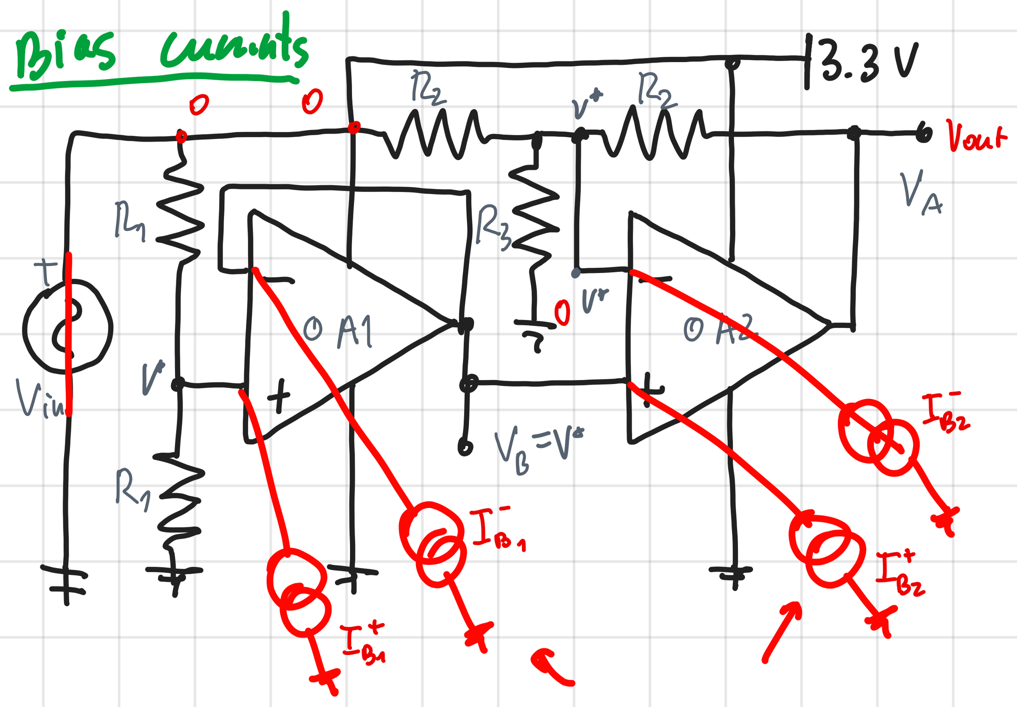


β computation:

$$\beta = \frac{R_2 \| R_3}{R_2 \| R_3 + R_2} = 0.26 \longrightarrow \frac{1}{\beta} = 3.9$$



b) • Bias currents



• $I_{B_1}^+$ $\longrightarrow$ $V^+ = I_{B_1}^+ (R_1 \| R_1) \cdot \left(\frac{(R_2 \| R_3) + R_2}{R_2 \| R_3}\right)\left(1 + \frac{R_2}{R_2 \| R_3}\right) = 0.9\,mV$

• $I_{B_1}^-$ $\longrightarrow$ $I_{B_1}^-$ (no effect)

• $I_{B_2}^+$ $\longrightarrow$ $I_{B_2}^+$ (no effect)

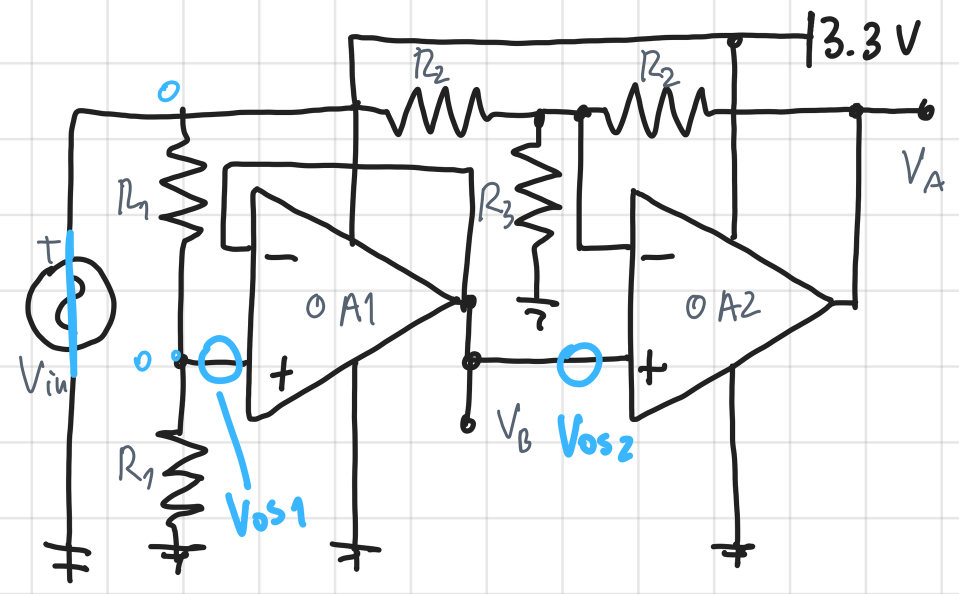
• $I_{B_2}^-$ $\longrightarrow$ $I_{B_2}^- \cdot 220k = 2.2\,\mu V$

$\longrightarrow V_{out_\varepsilon} \cong 0.9\,mV$

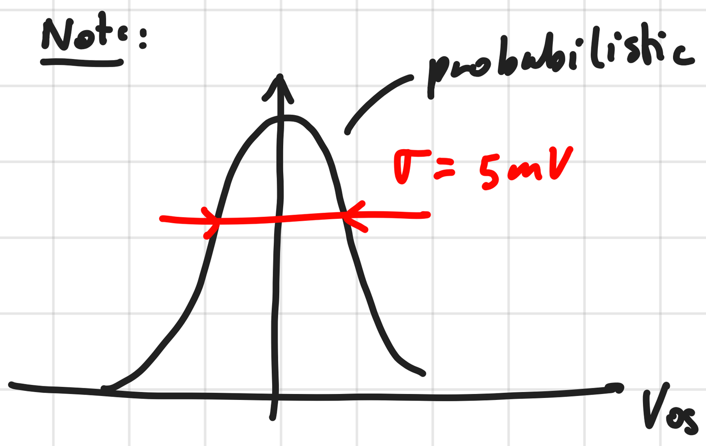
error

• Offset $\longrightarrow$ due to mismatch of components (e.g. diff. btw transistors that make the Op Amp $\longrightarrow$ see slides skipped for ref.)

We simply model this mismatch like a voltage offset



Note:



we don't know if it's pos. or neg.

• V_{os1} $\quad V_{out_\varepsilon}^{I} = V_{os1}\left(1 + \frac{220k}{220k \| 110k}\right) = V_{os1} \cdot 3.9 = \pm 18\,mV$ ← first contribution

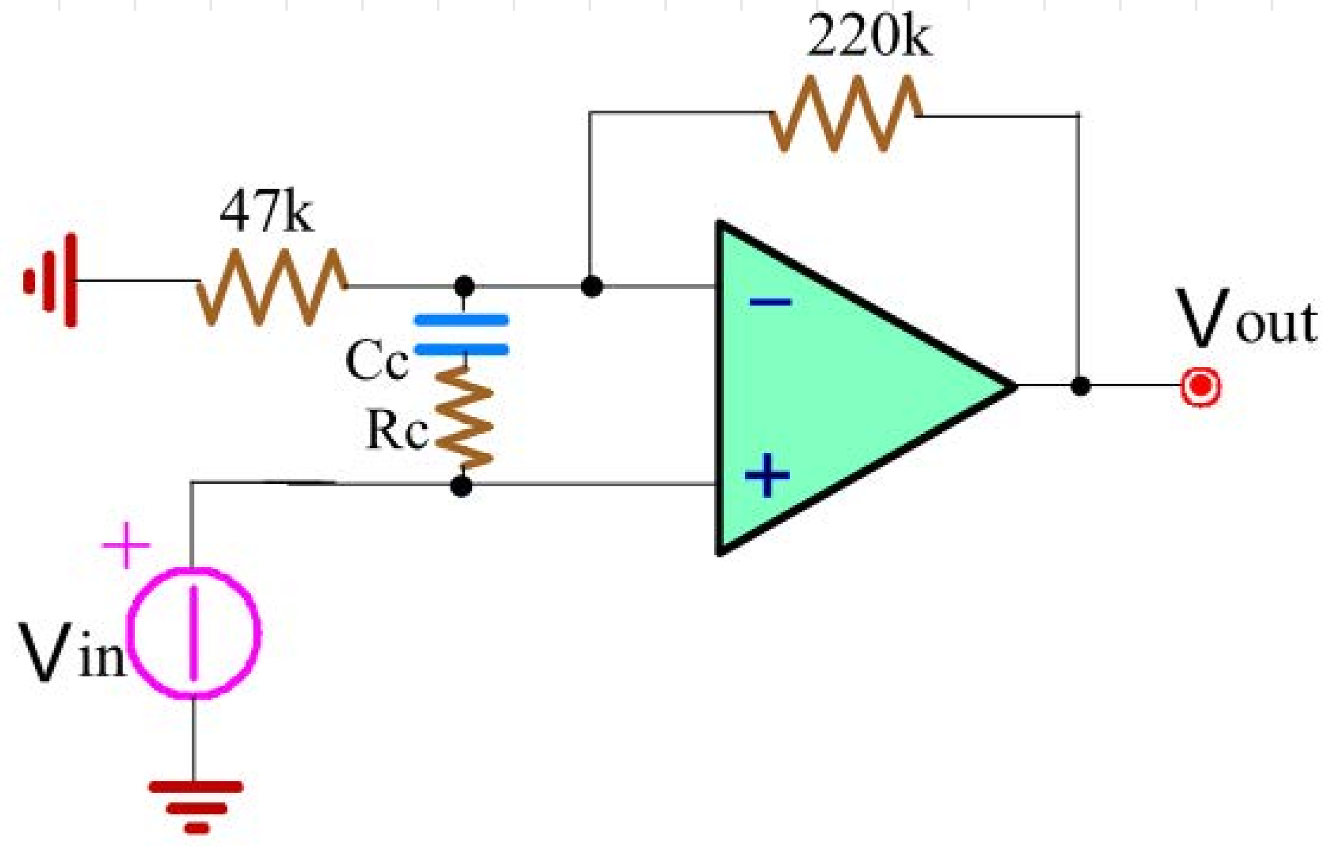
• V_{os2} $\quad V_{out_\varepsilon}^{II} = V_{os2}\left(1 + \frac{220k}{220k \| 110k}\right) = \cdots = \pm 18\,mV$ ← second contrib.

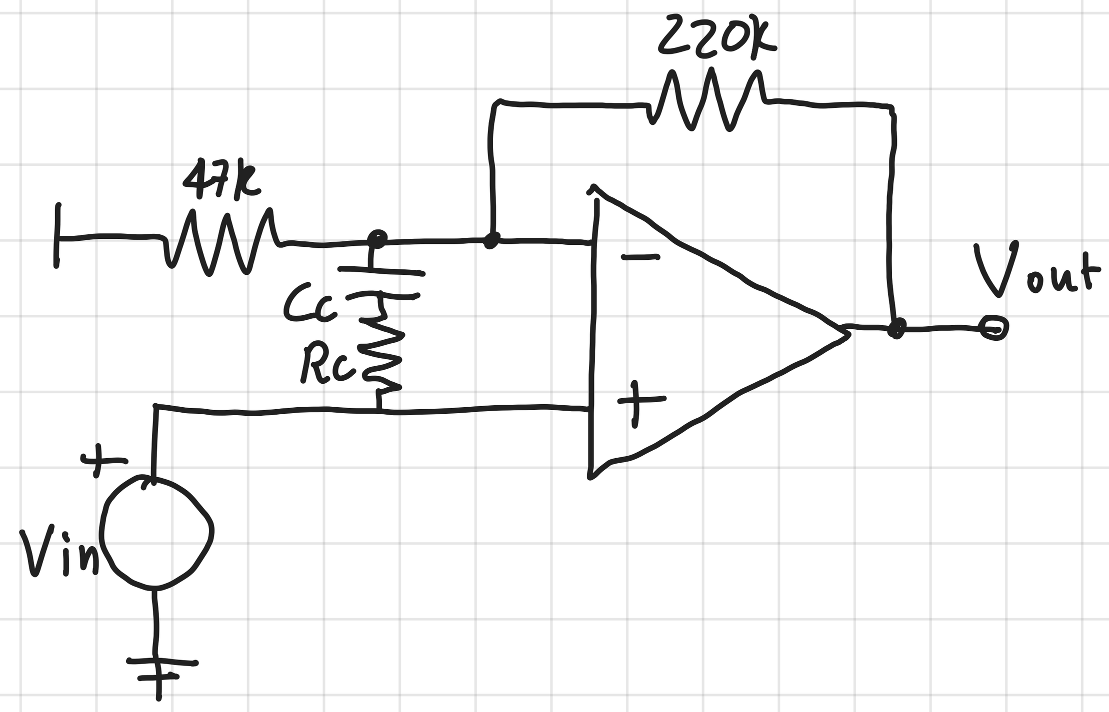
$\longrightarrow V_{out} = \pm 18\,mV \pm 18\,mV = \pm 36\,mV$

we have to consider the whole span

only by chance they will cancel out

5



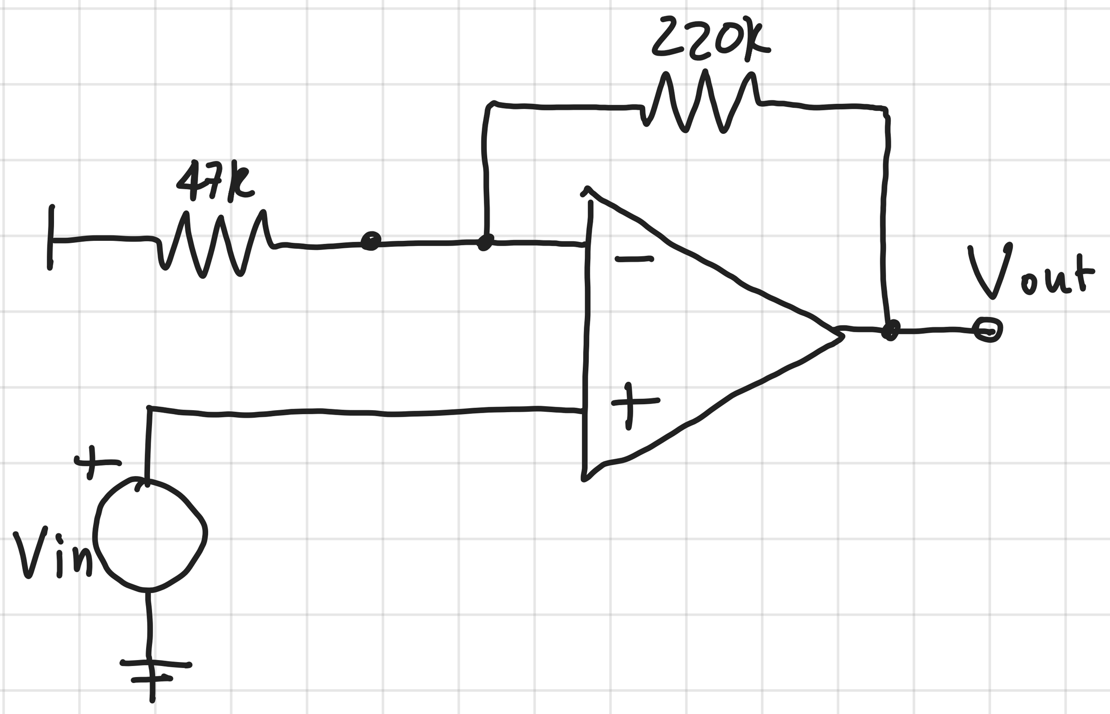


Uncompensated OpAmps with A_0=120dB, f_0=5kHz and f_1=50MHz, I_B=1nA and V_{OS}=3mV.

a) **Without** C_C and R_C, compute stability and PM.

b) Properly size C_C and R_C to attain PM=90°.

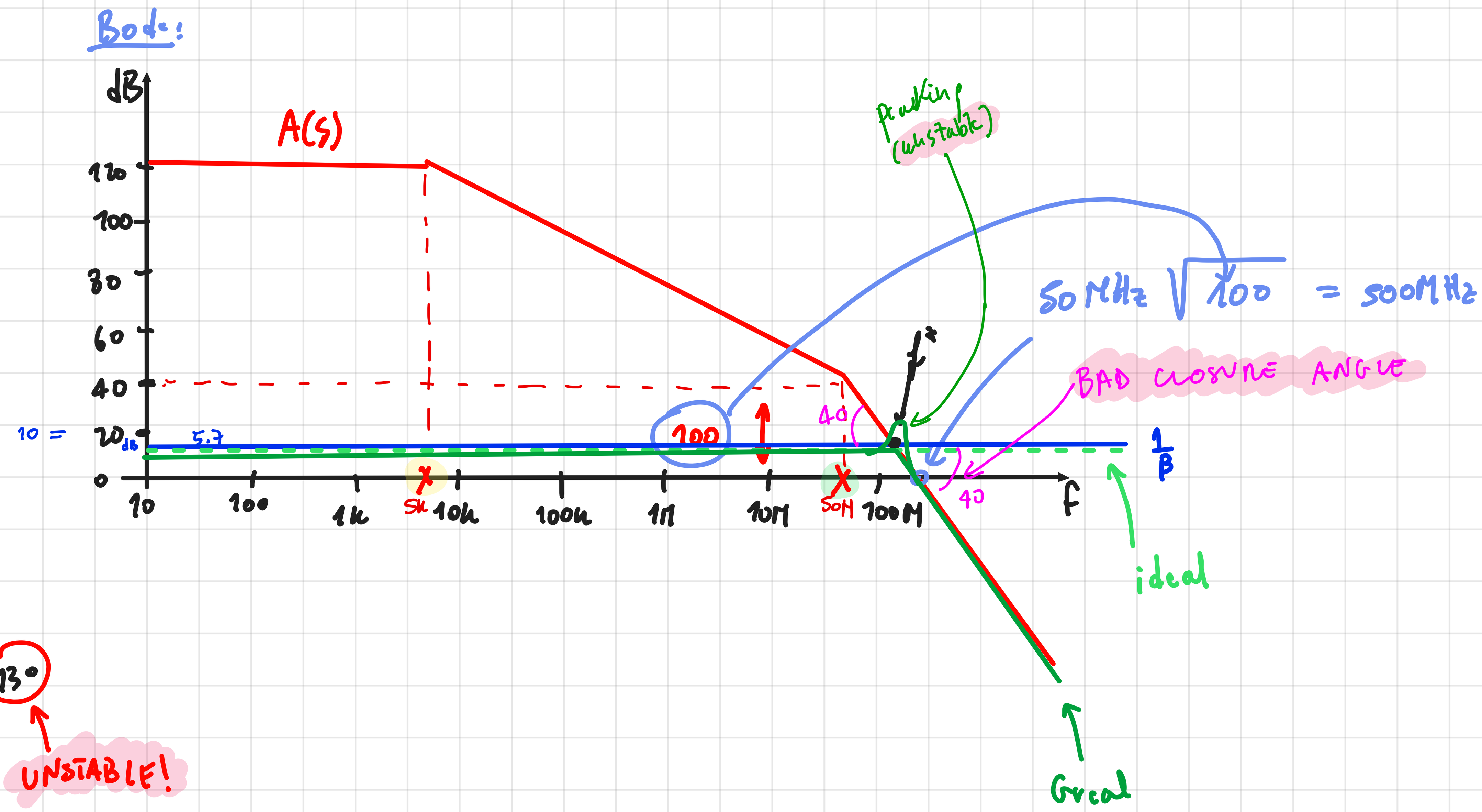
a)



→ Non-inverting

$\hookrightarrow G_{ideal} = 1 + \frac{R_2}{R_1} = 1 + \frac{220k}{47k} = 5.7$

Bode:



$\hookrightarrow f^* = 50MHz \cdot \sqrt{\frac{100}{5.7}} = 209\ MHz$

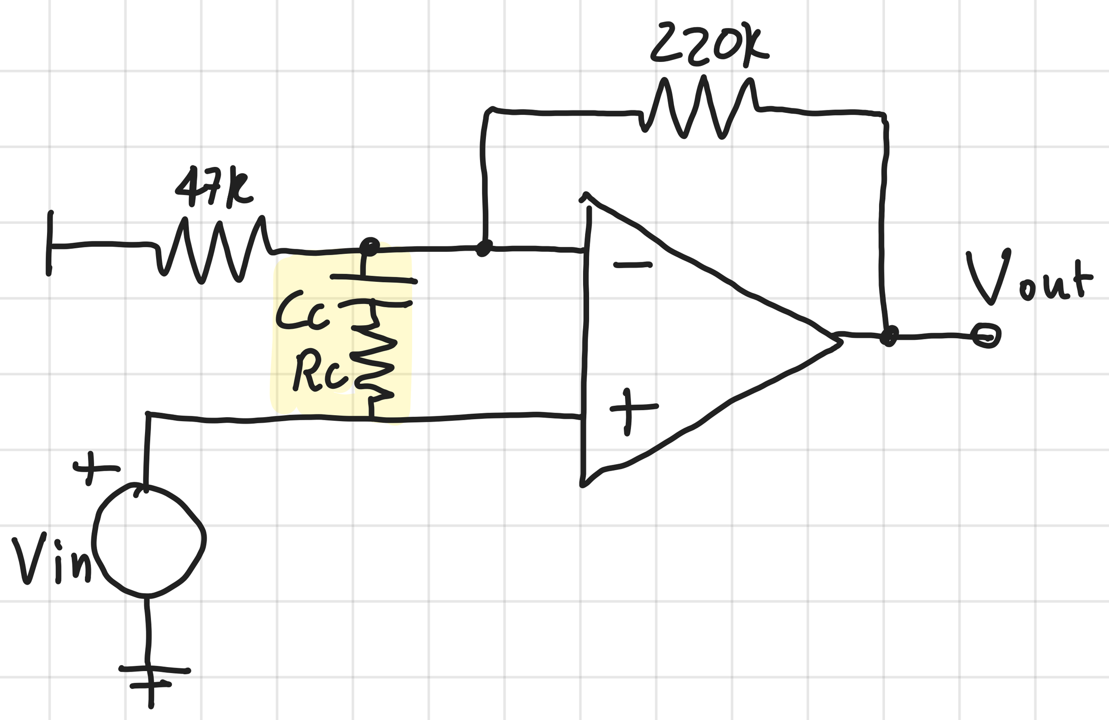
Phase margin:

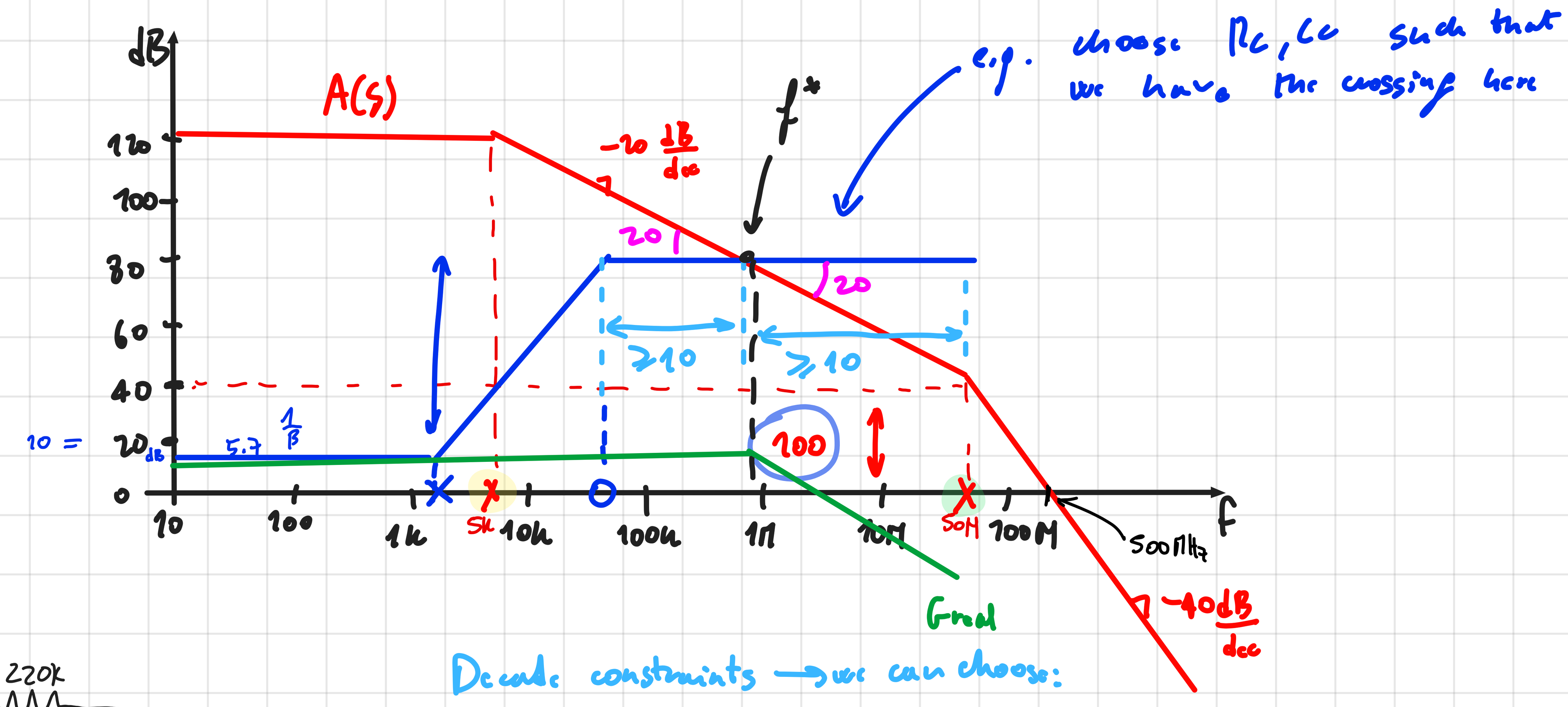
$PM = 180° - 90° - \arg \frac{f^*}{50MHz} = 90° - \arctan\left(\frac{209\ MHz}{50\ MHz}\right) = 90° - 77° = 13°$

UNSTABLE!

b)

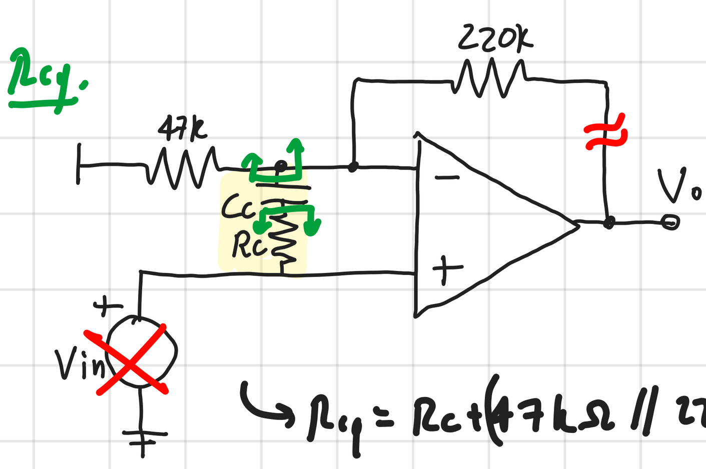
Consider now:





$\hookrightarrow zero_\beta = \frac{1}{2\pi R_C C_C}$

$\hookrightarrow pole_\beta = \frac{1}{2\pi C_C (R_C + (47k // 220k))}$



$\hookrightarrow R_{eq} = R_C + (47k\Omega // 220k)$

Decade constraints → we can choose:

$\hookrightarrow f^* = \frac{50MHz}{10} = 5\ MHz$

e.g. $\frac{1}{\beta}(\infty) = 10 \cdot A_{min} = 1k \simeq 1 + \frac{220k}{R_C}$

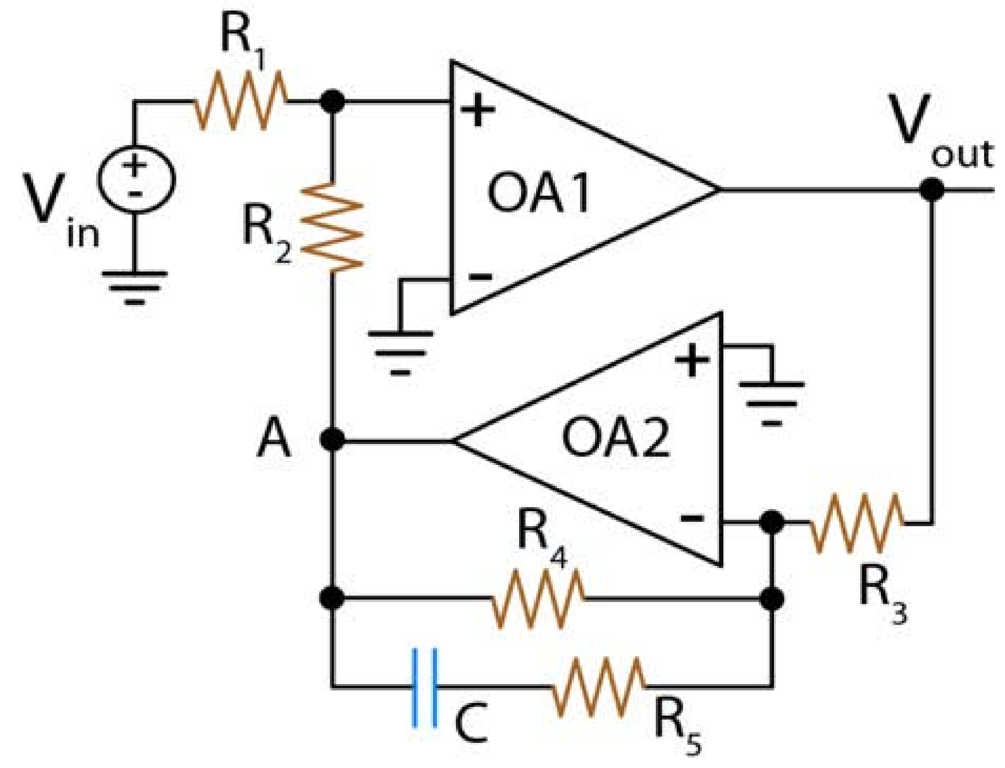
$\hookrightarrow R_C = \frac{220k}{999} \simeq 220\ \Omega$

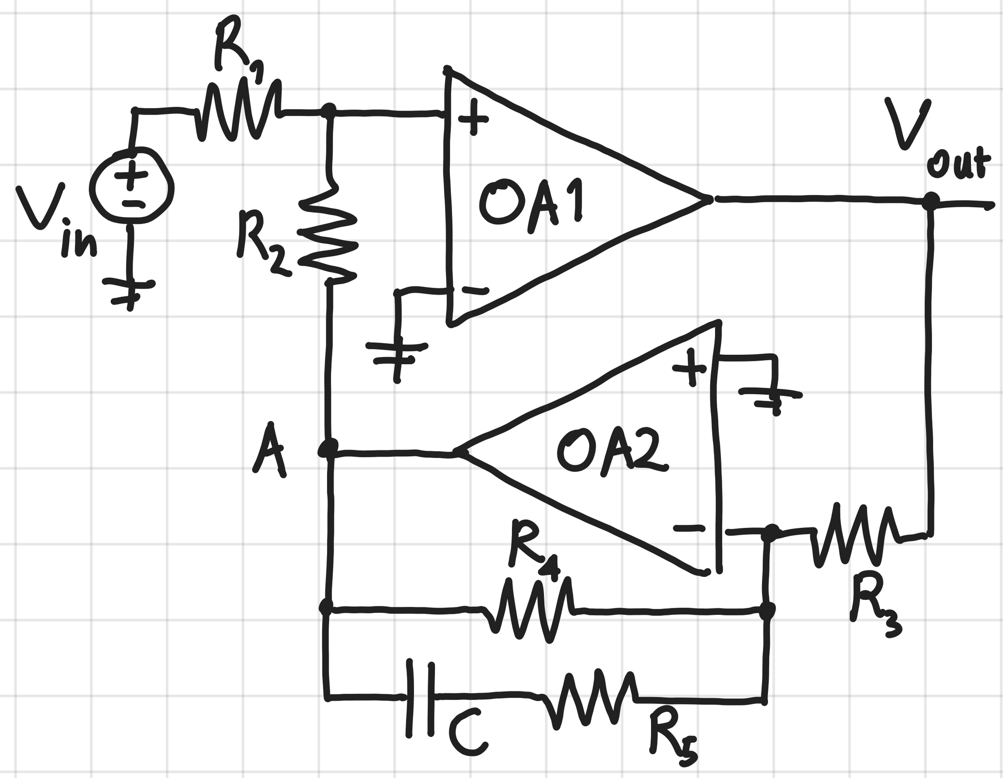
we want the zero$_\beta$ to be at least one decade before f^* → $zero_\beta = \frac{1}{2\pi C_C R_C} = \frac{f^*}{10} = 500kHz$

$\hookrightarrow C_C = \frac{1}{2\pi \cdot 500kHz \cdot 220\Omega} \cong 1.4\ nF$

R_C

(6)





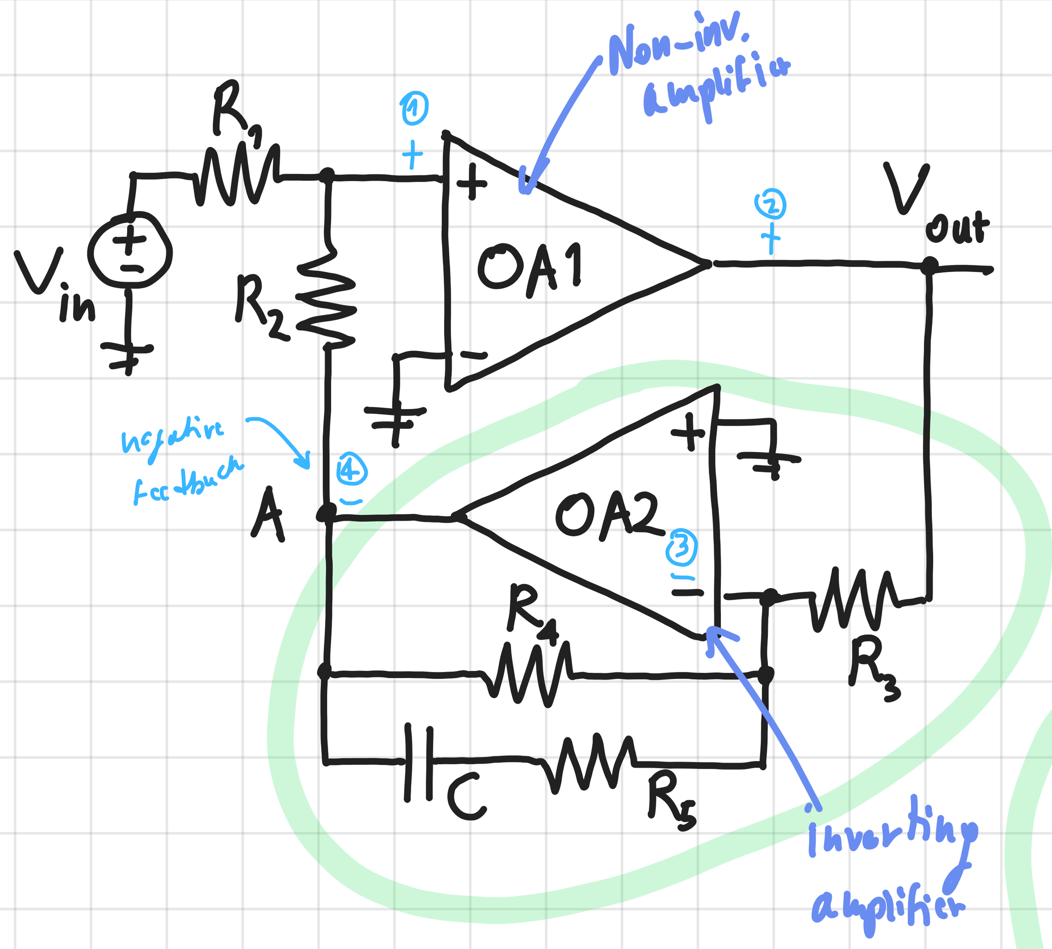
OpAmp with A_0=120dB and GBWP=20MHz, with I_B=10nA and V_{OS}=5mV.
R_1=1kΩ, R_2=50kΩ, R_3=2kΩ, R_4=50kΩ, R_5=1kΩ, C=10nF.

a) Plot the Bode diagram of the $v_{out}(f)/v_{in}(f)$ **real** gain, when OA2 is still **ideal**.

b) Discuss circuit stability when also OA2 is **real**.

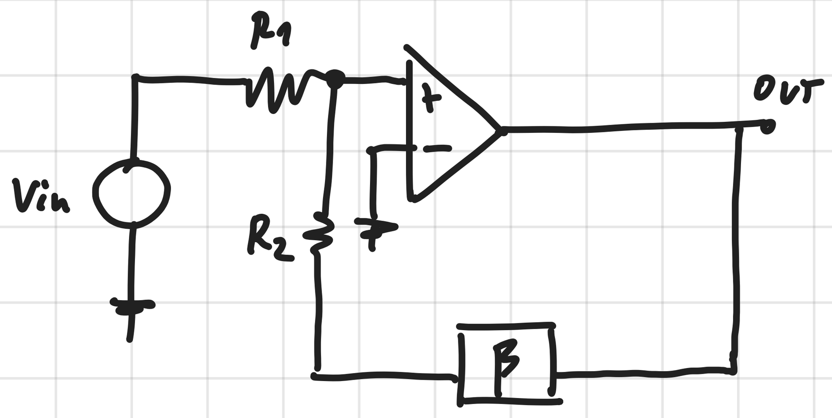
c) Compute the output error due to bias currents and offset voltages of both OpAmps.

a)



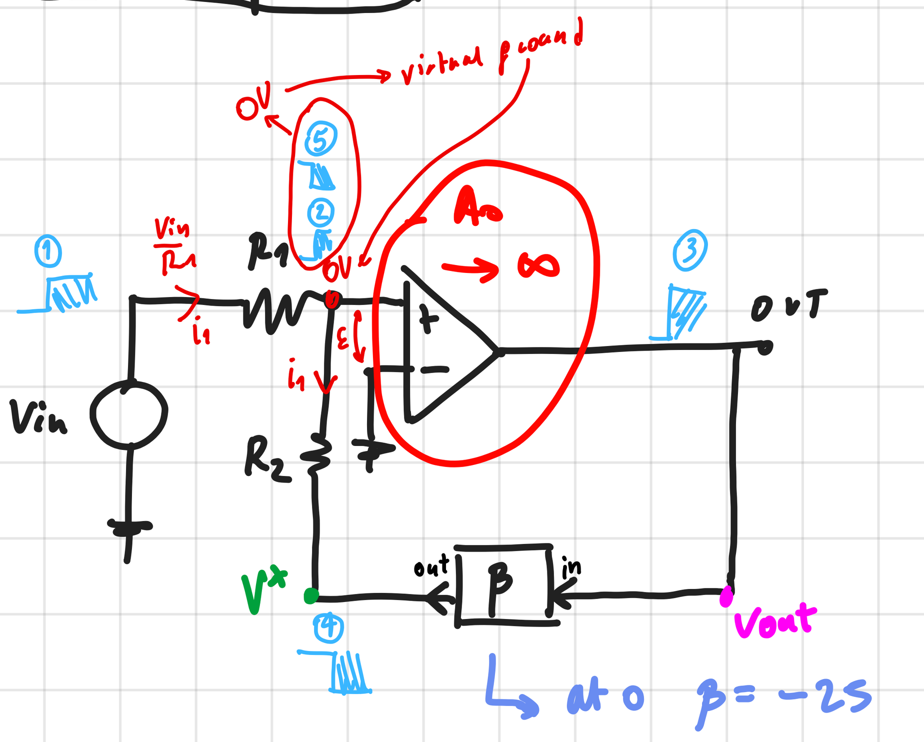
→ Negative feedback

$\equiv$



$$\begin{cases} G(0) = -\dfrac{R_4}{R_3} = -25 \\ G(\infty) = -\dfrac{R_4 \| R_5}{R_3} = -0.48 \end{cases}$$

↳ Gain Computation:



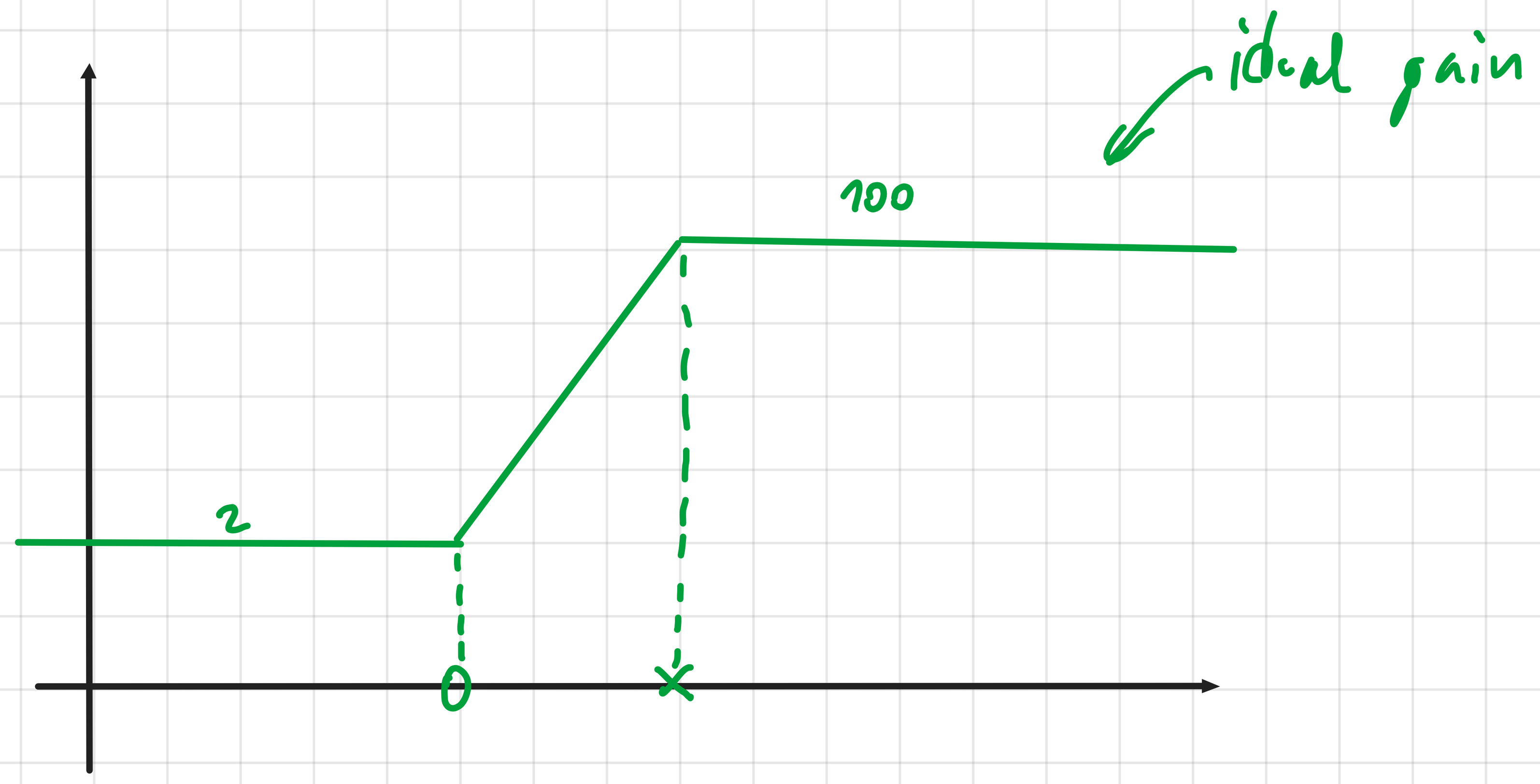
↳ at 0 $\beta = -25$
at ∞ $\beta = -0.48$

$$\rightarrow V^+ = -\frac{V_{in}}{R_1} \cdot R_2 = -\frac{V_{in}}{1k} \cdot 50k = -V_{in} \cdot 50$$

$$\rightarrow V^+ = -\beta V_{out} \rightarrow \begin{cases} V_{out}(0) = -\dfrac{V^+}{25}(0) \\ V_{out}(\infty) = -\dfrac{V^+}{0.48}(\infty) \end{cases}$$

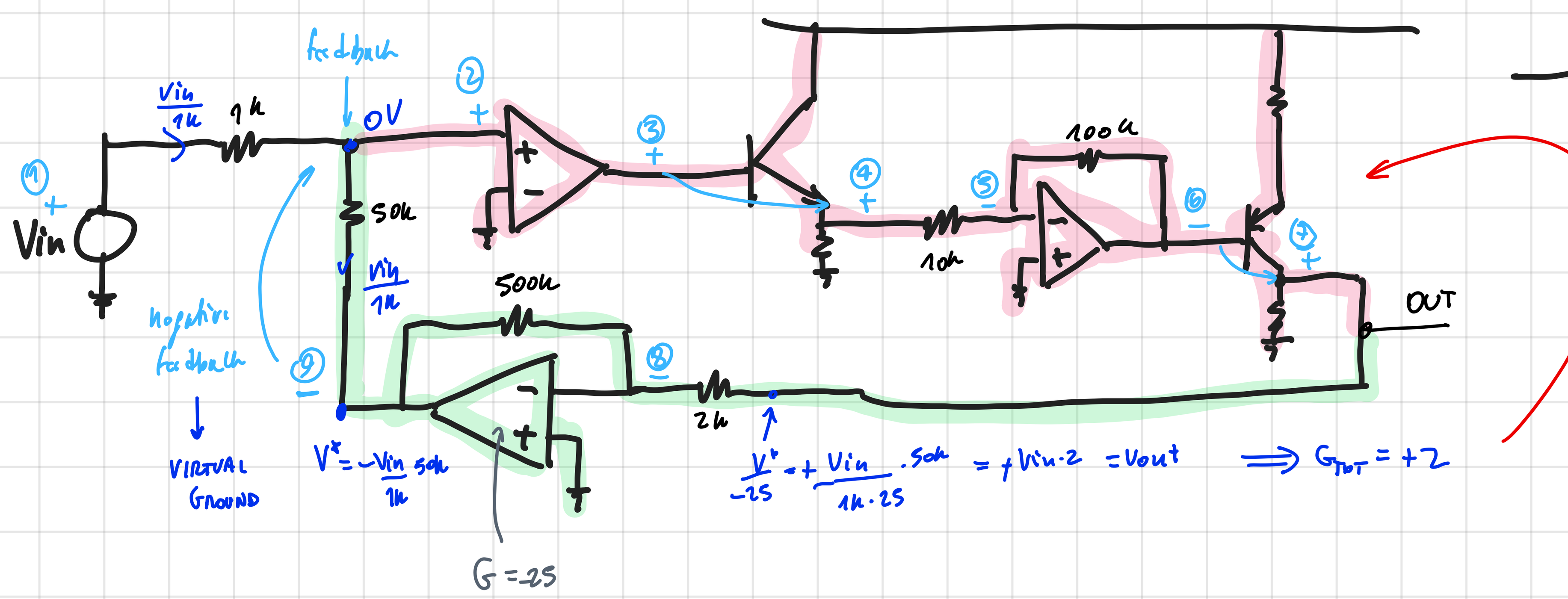
$$G_{DC} = \frac{V_{out}}{V_{in}}(0) = \frac{-50}{-25} = +2$$

$$G_{AC} = \frac{V_{out}}{V_{in}}(\infty) = \frac{-50}{-0.48} \simeq +100$$



ex.

Consider a different circuit to understand how to analyze the negative feedback



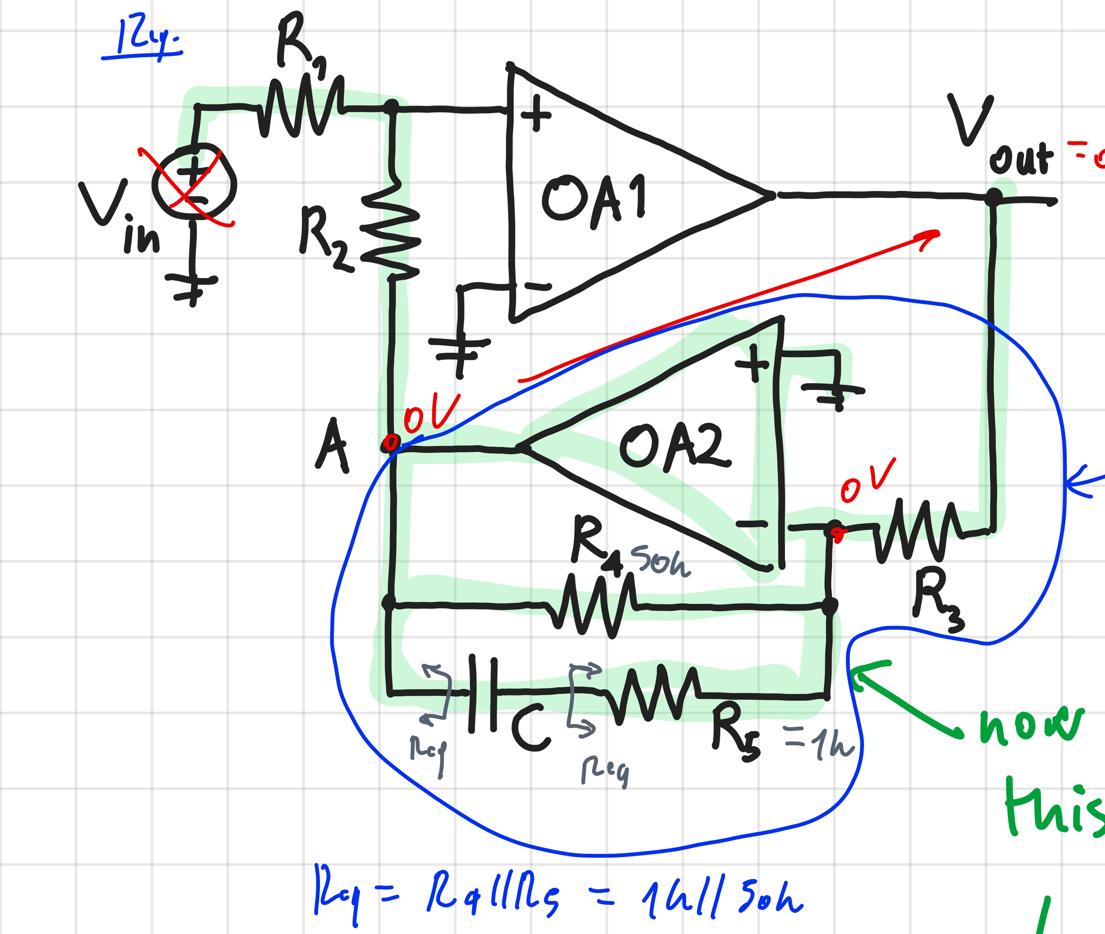
we don't care about this direction thanks to the feedback we can arrive to Vout without passing through that network

this is A(s)

↓

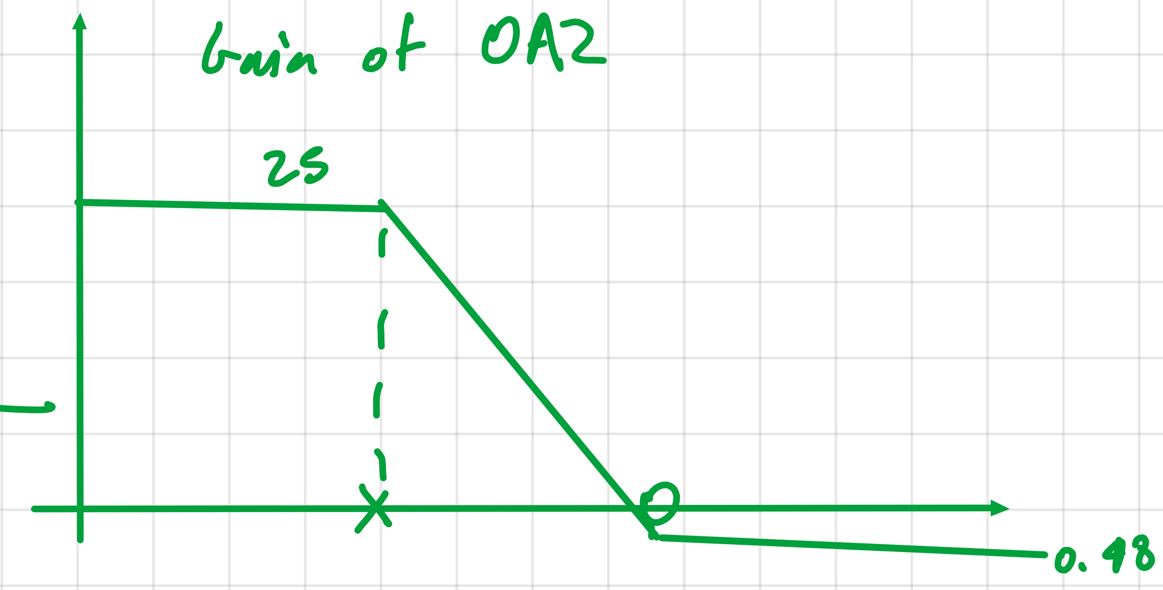
What matters is the β network from the output → input

b) Going back to our circuit



$\rightarrow$ pole $= \frac{1}{2\pi C(50k+1k)} = 312\,Hz$

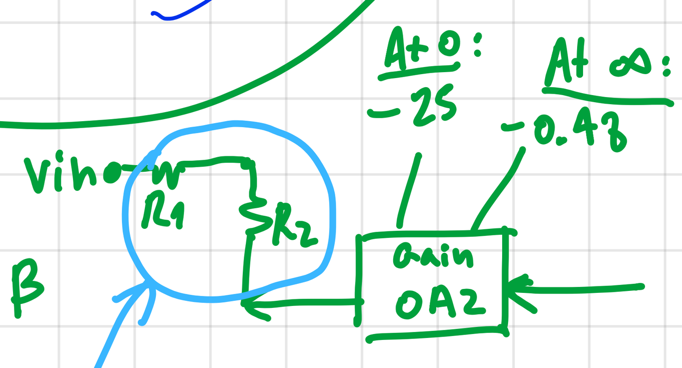
$\rightarrow$ zero $= 312 \cdot \frac{25}{0.48} = 16\,kHz$



now we consider this as β

↳ before we saw that this has this characteristic

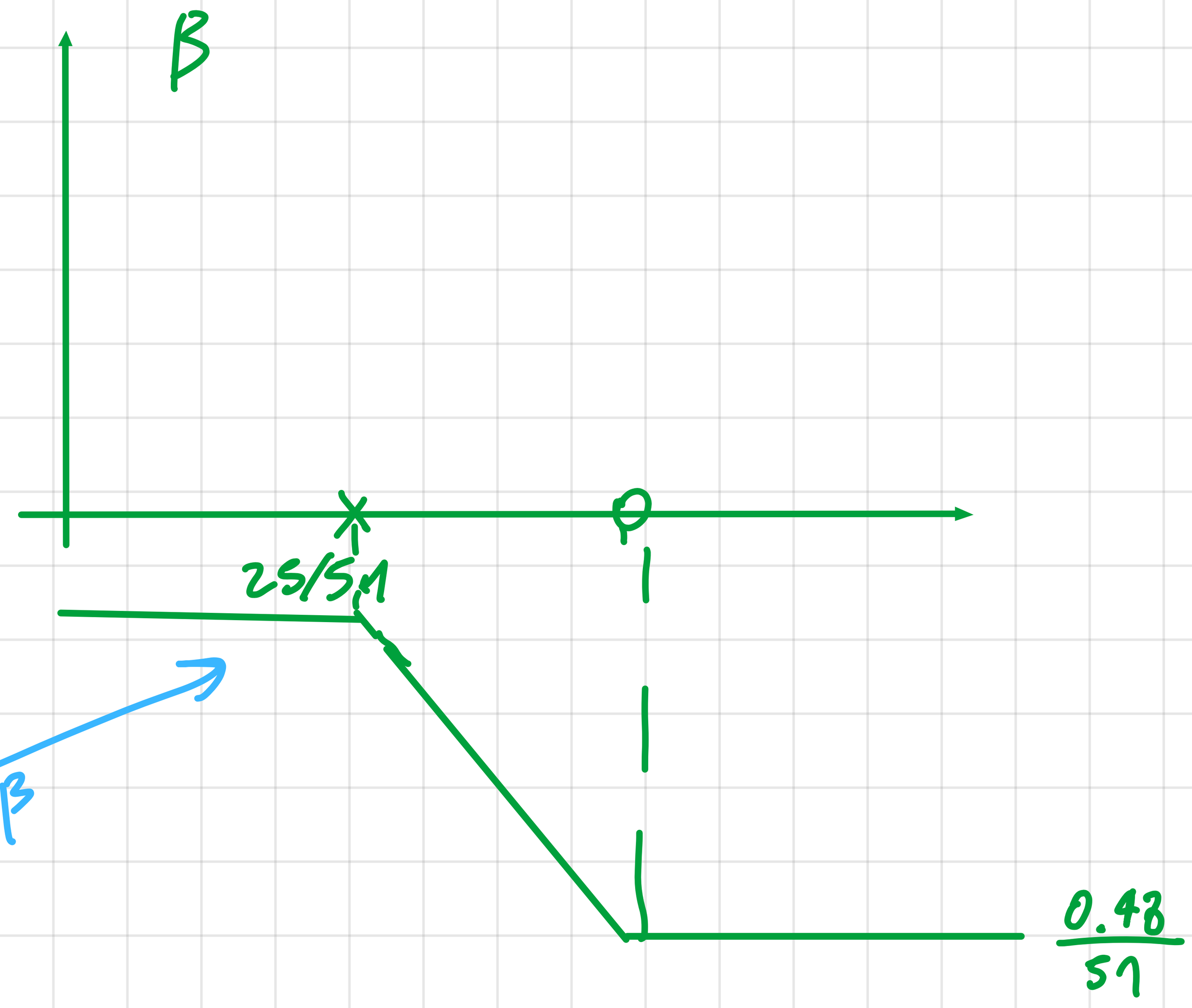
↳ so the new β



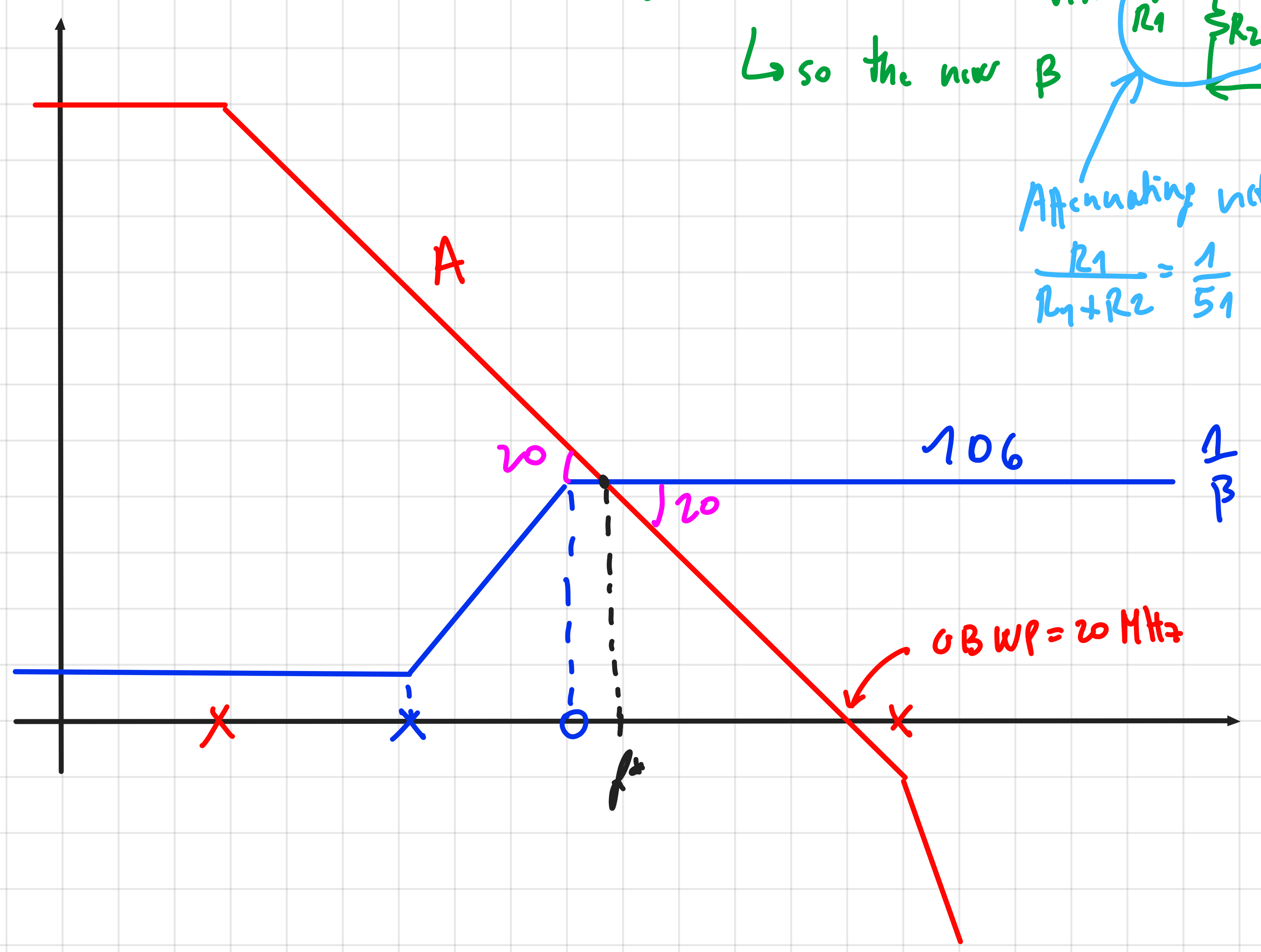
Attenuating network

$\frac{R_1}{R_1+R_2} = \frac{1}{51}$

so β



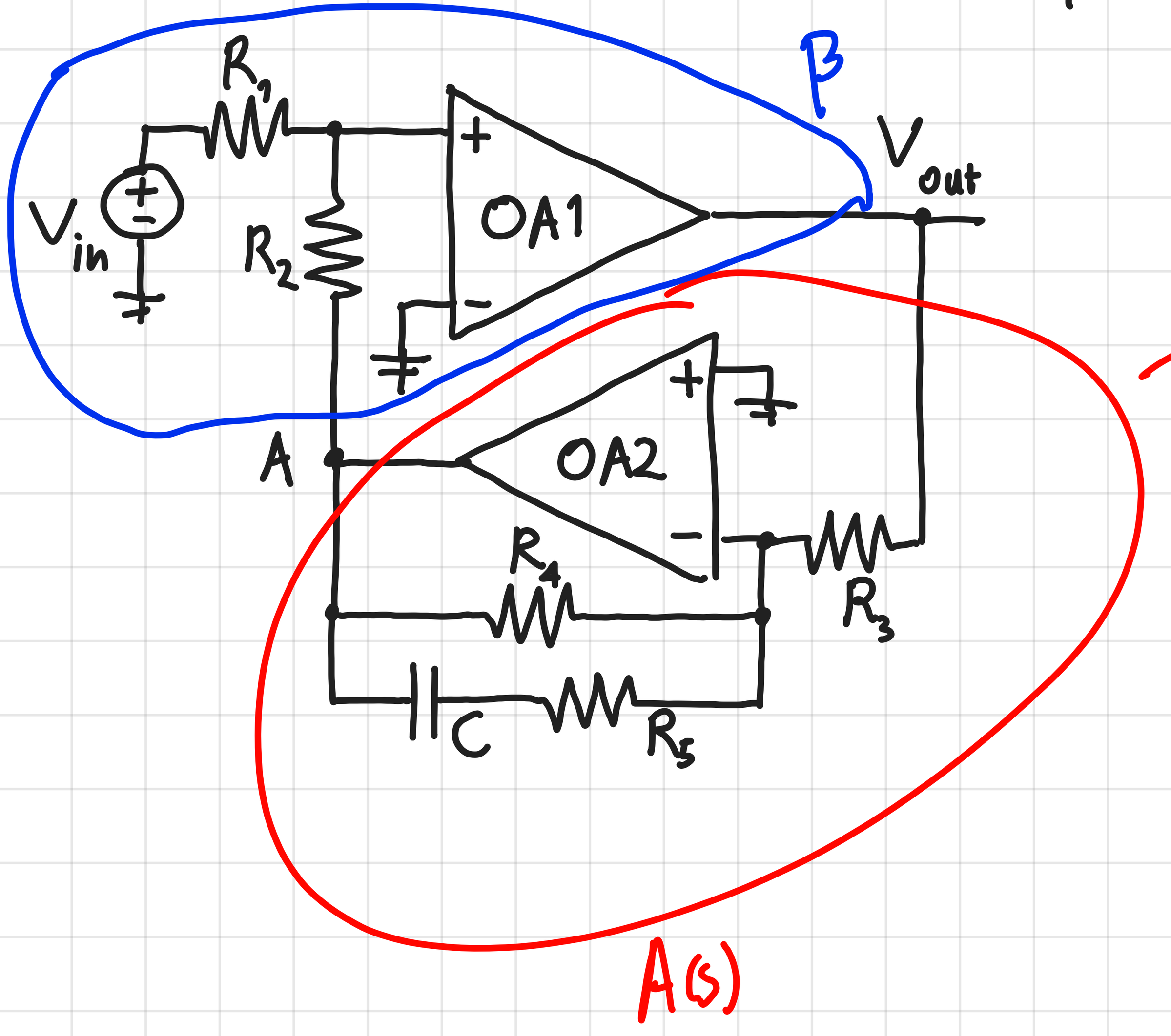
Bode

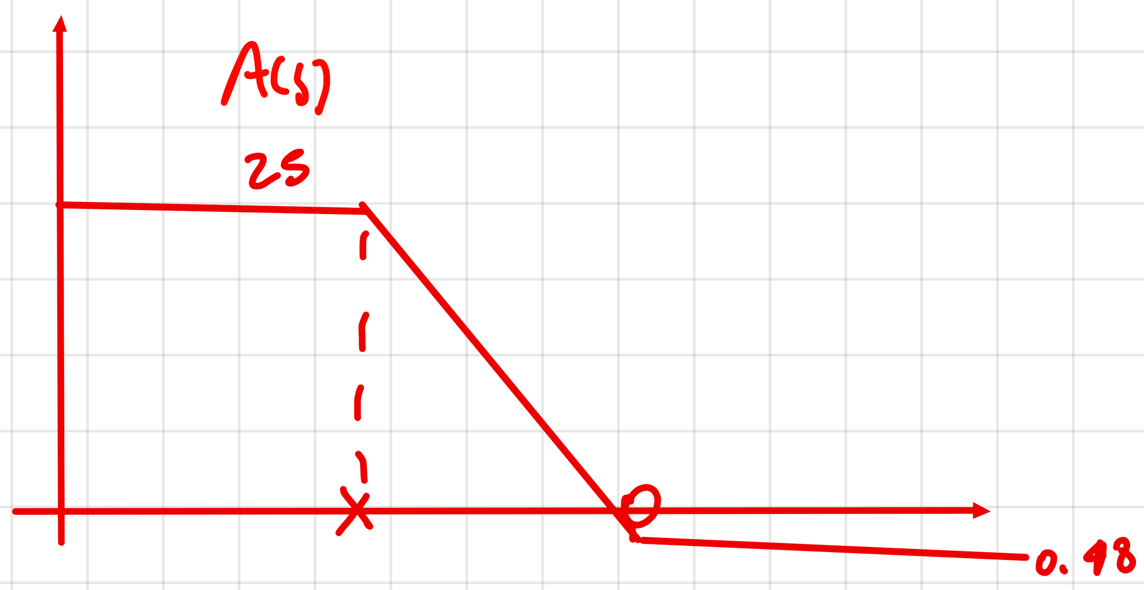


$\rightarrow f^* = \frac{GBWP}{106} = 189\,kHz$

Note:

↳ Suppose now we choose different β and A(s)

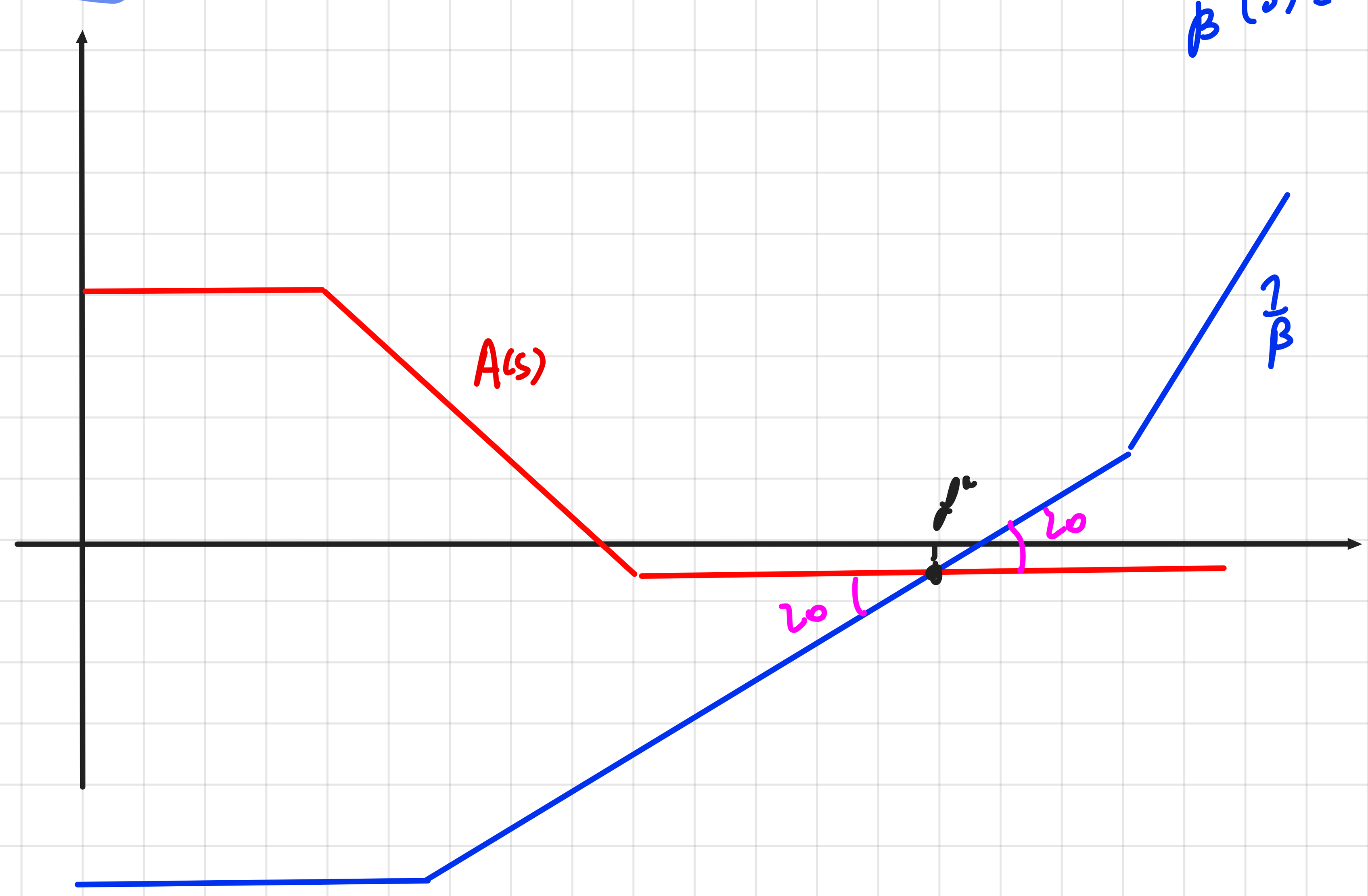




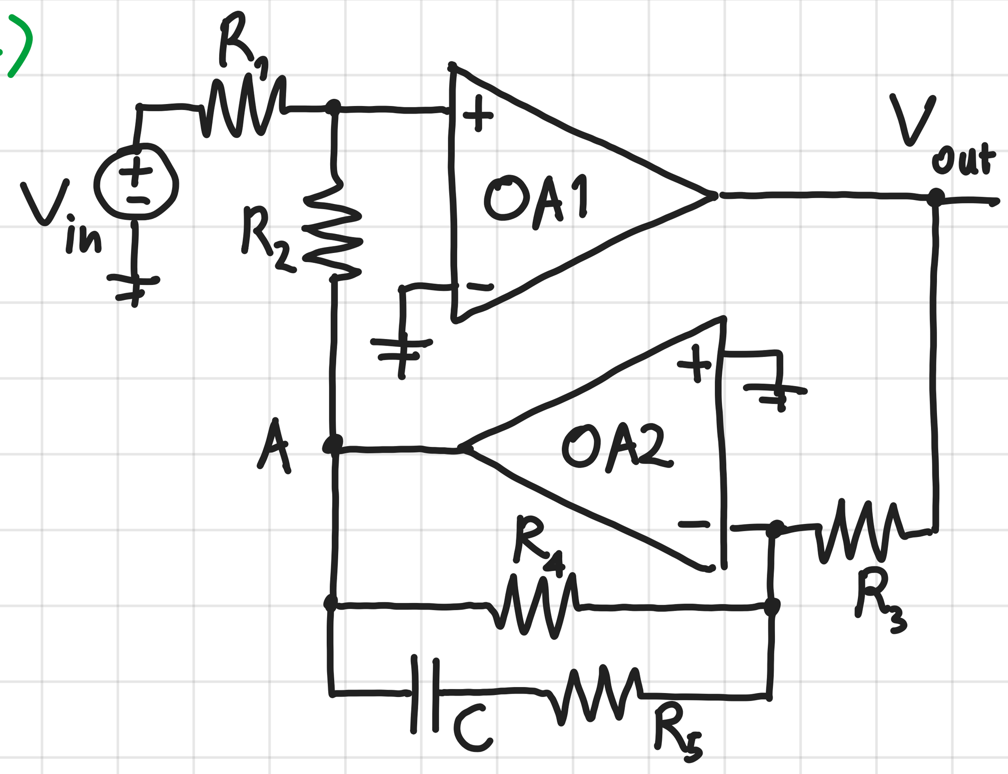
$\beta(s) = \frac{R_1}{R_1+R_2} \cdot A(s) =$ DC: $\frac{1}{51} \cdot 1000000 = 19 \cdot 10^3$; AC: $\frac{1}{51}$

↳ $\frac{1}{\beta}(s) =$ DC: $51 \cdot 10^{-6}$; AC: 51

Bode

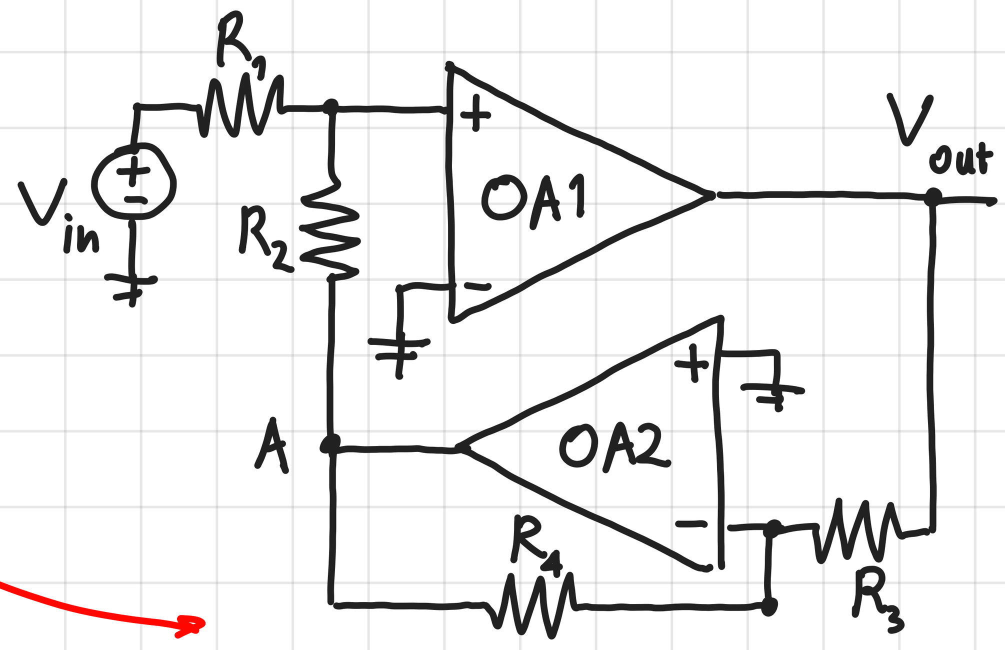


$\rightarrow$ if we compute it f^* will be the same computed before c)

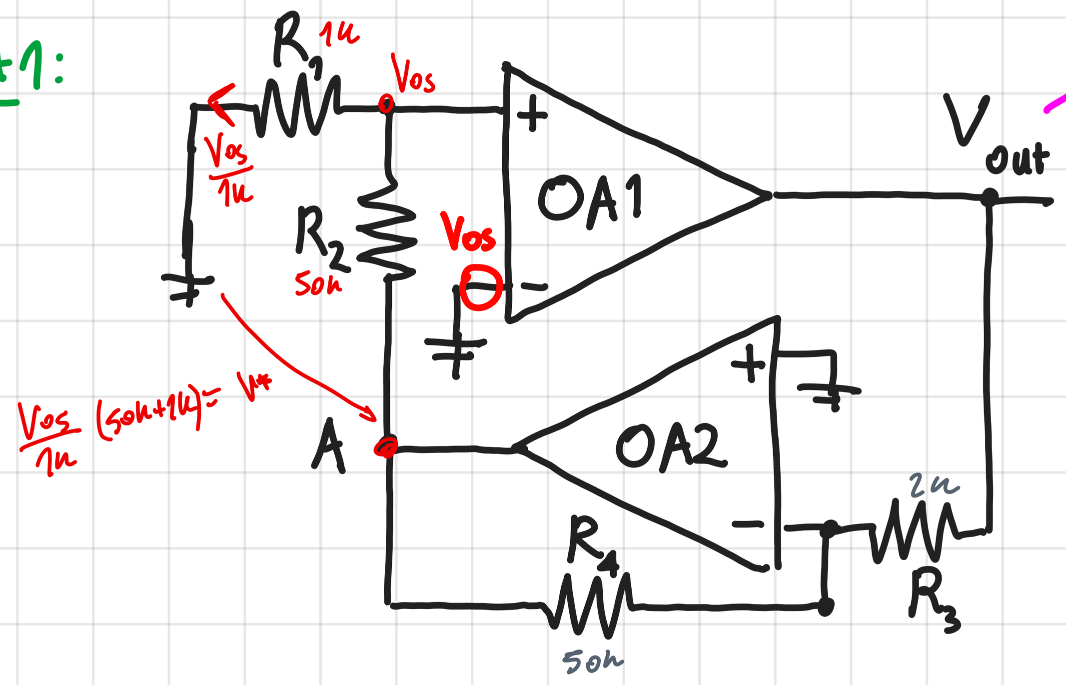


consider it at DC

c open



- Offset 1:

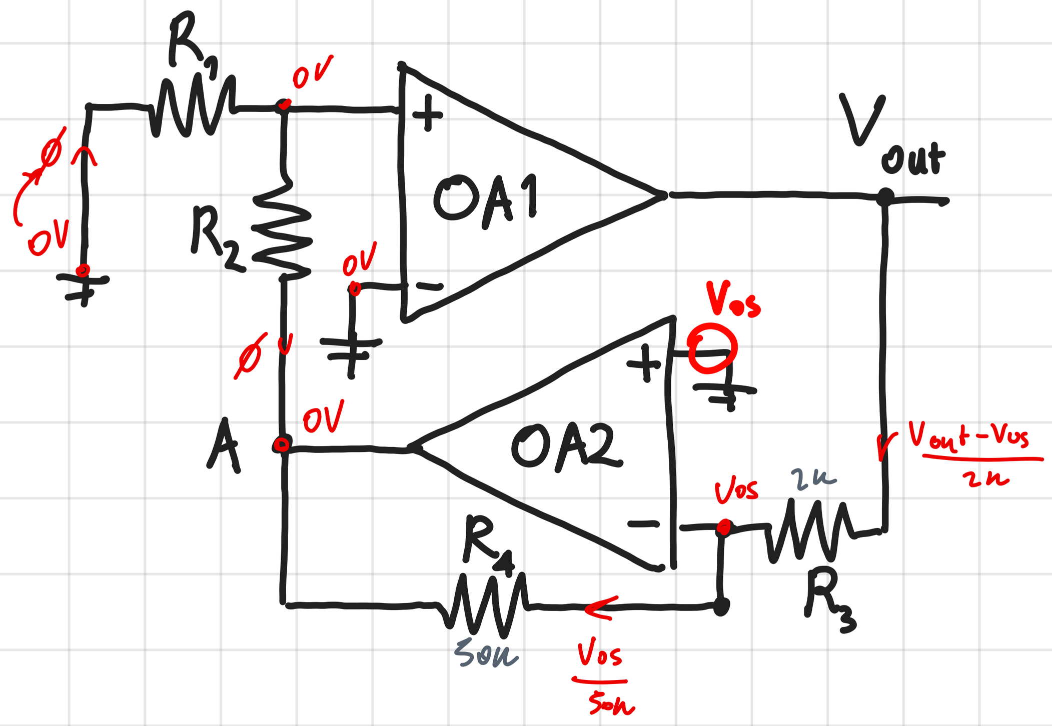


$V_{out} = \frac{V_{os}}{1k} \cdot \frac{51k}{25}$

Offset 1 contribution on the output:

↳ $V_{out_{os1}} \approx V_{os} \cdot 2$

- Offset 2:



$\rightarrow \frac{V_{out}}{50k} = \frac{V_{out} - V_{os}}{2k}$

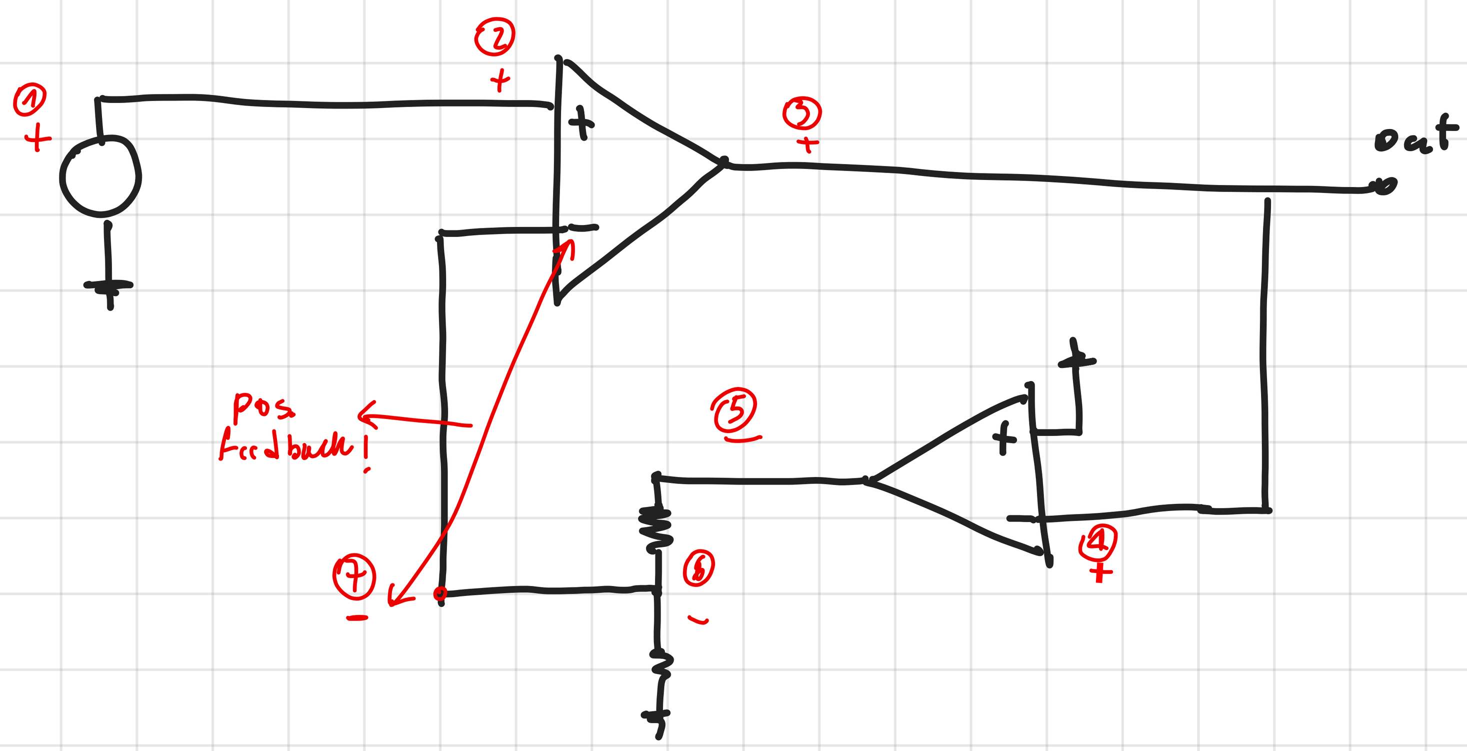
$V_{out} \cdot \frac{50k}{50k+2k} = V_{os}$

Offset 2 contribution on the output:

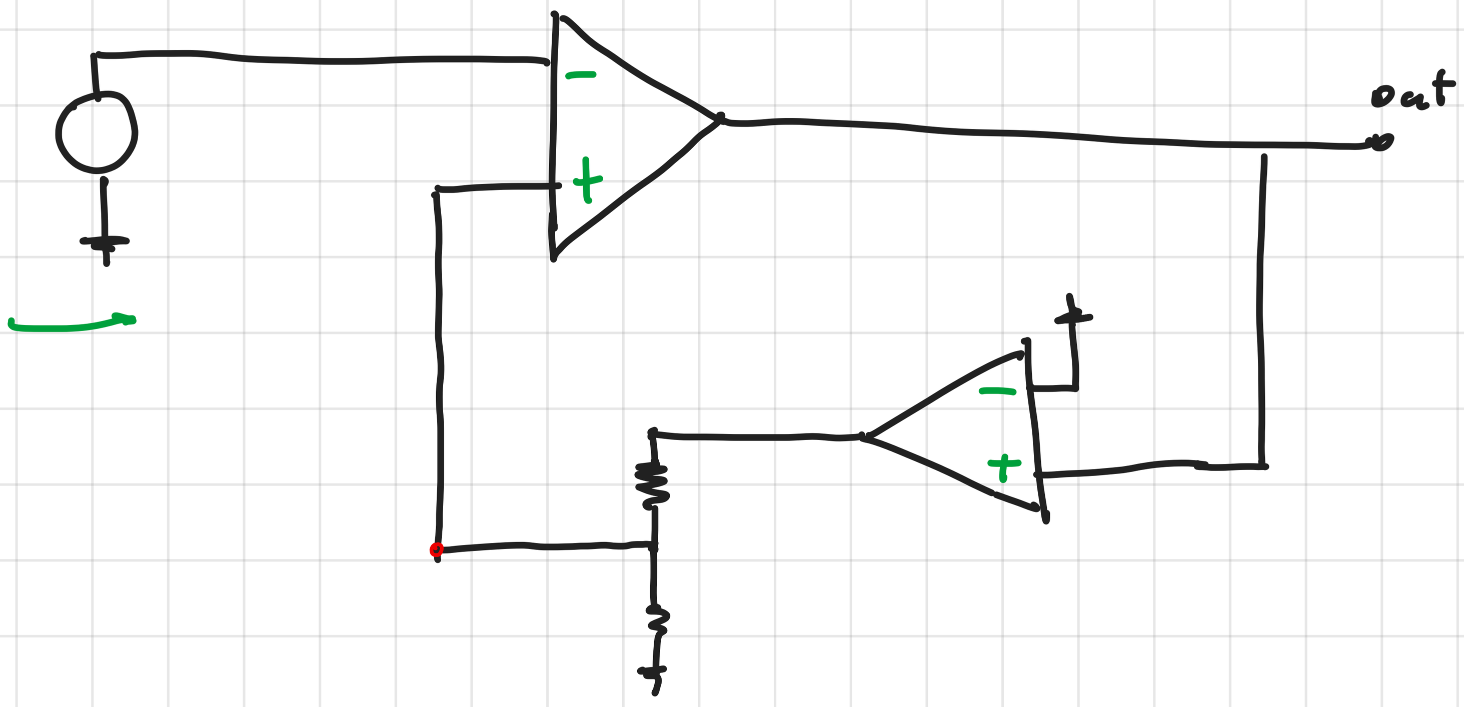
$V_{out_{os2}} = V_{os} \cdot \frac{52}{50}$

ex. Feedback effects

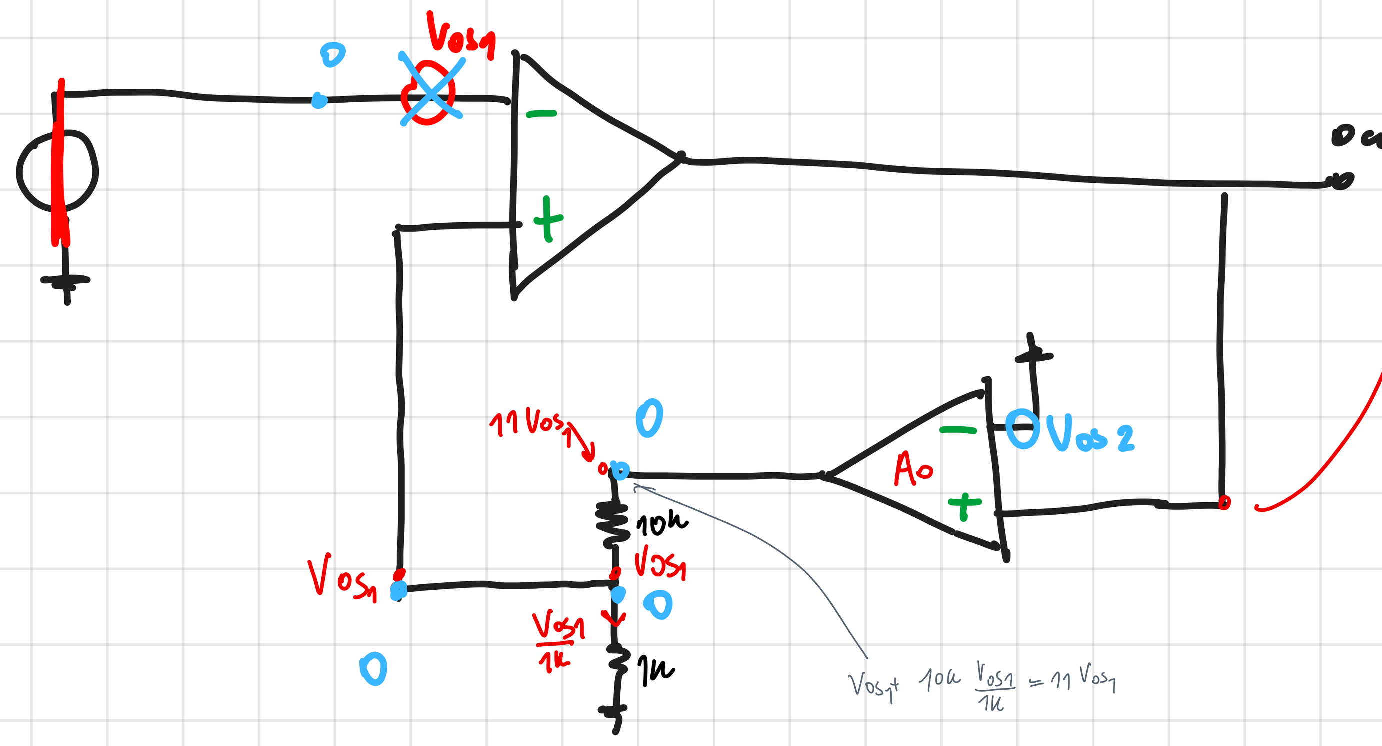
Consider the following circuit:



to make it neg. feedback we can invert the signs in the op amp



↳ If we have an offset



$V_{out} = \frac{11 V_{os1}}{A_0} \simeq 0V$

high

$\leftrightarrow V_{out} = V_{os2}$

20/10/22

E01 (Beretta)

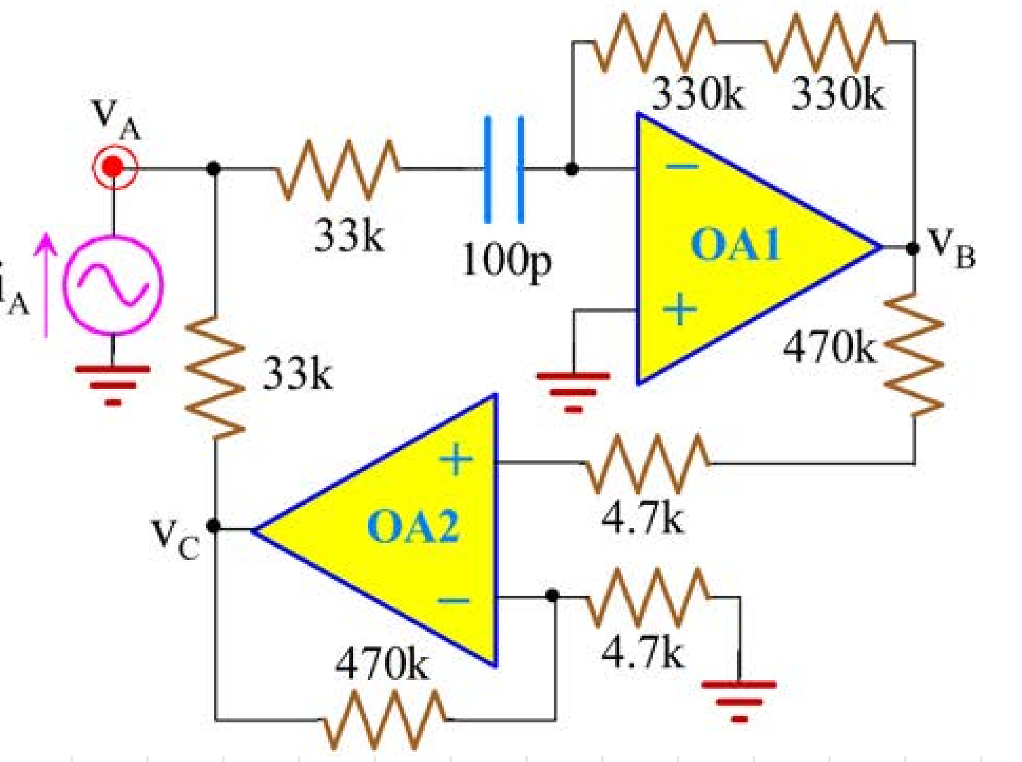
1

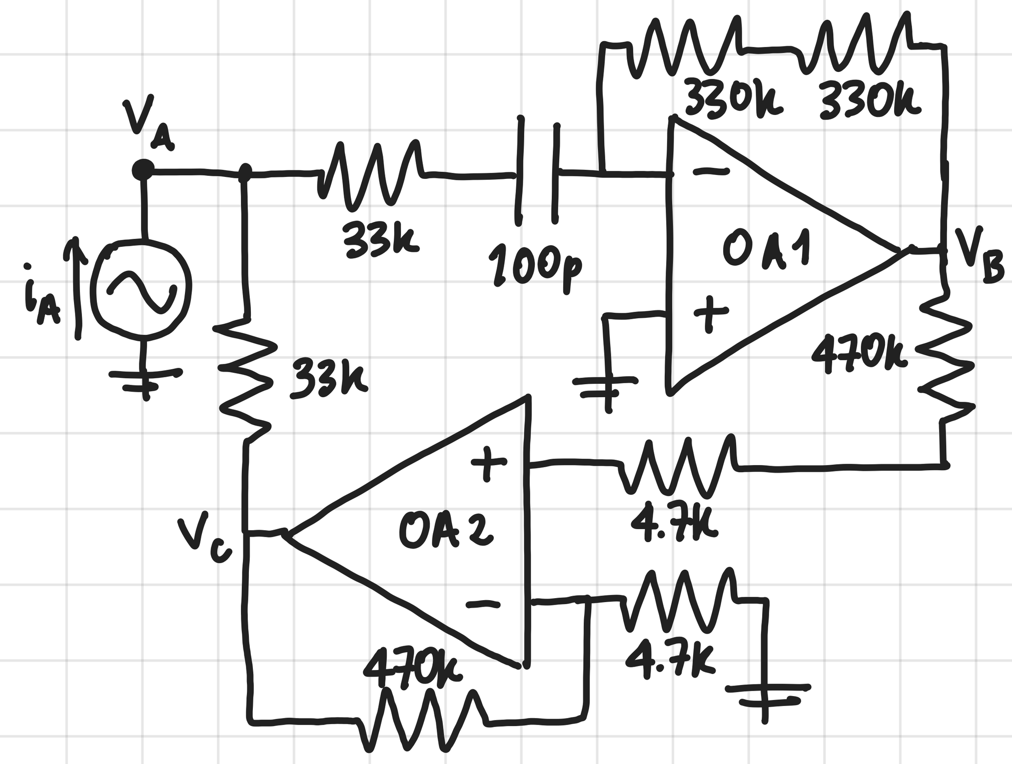
Ex. 1

Note that current (not voltage) input signal source. Consider both OpAmps ideal.

a) Compute the value of the v_A/i_A ratio at DC and AC (i.e. at very high frequency) in two ways, as a gain (output/input=…) and as an input impedance (Z_{in}=…).

b) Compute poles and zeros and plot the Bode diagram of $v_A(f)/i_A(f)$, when both OpAmps are still ideal.

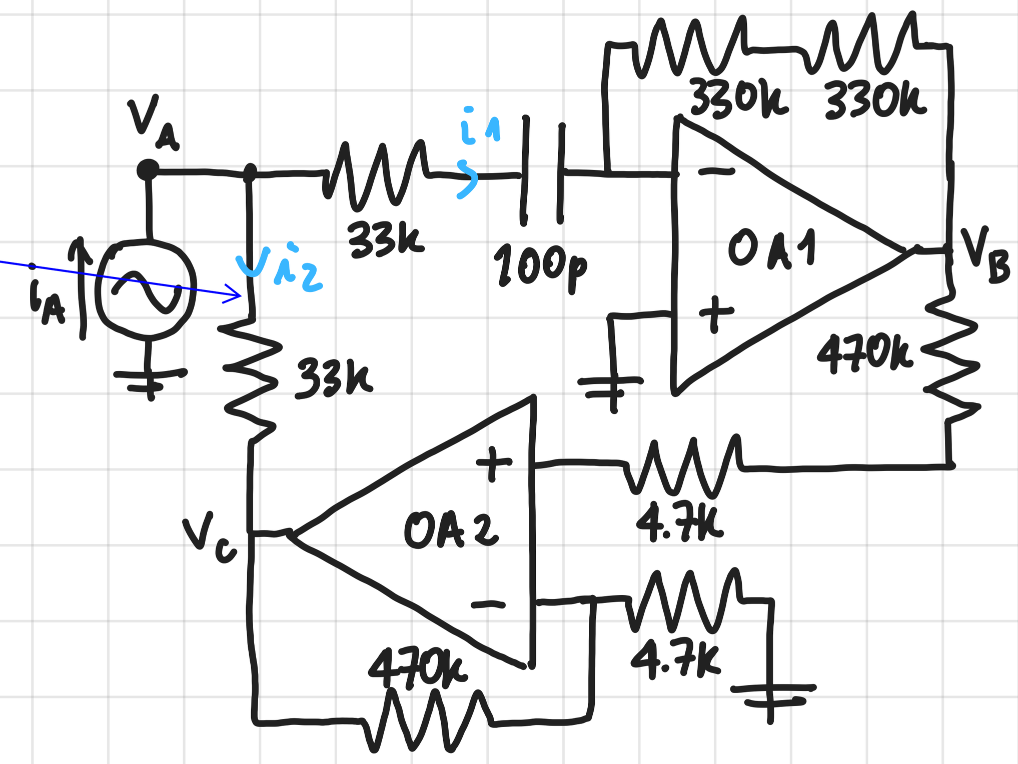




a) $\frac{V_A}{i_A}$ (I) $\frac{\text{output}}{\text{input}}$ (II) Z_{in}

@ DC $\longrightarrow$ C_{open} $\quad i_A = \frac{V_A}{33k} \Rightarrow \left.\frac{V_A}{i_A}\right|_{DC} = 33k$

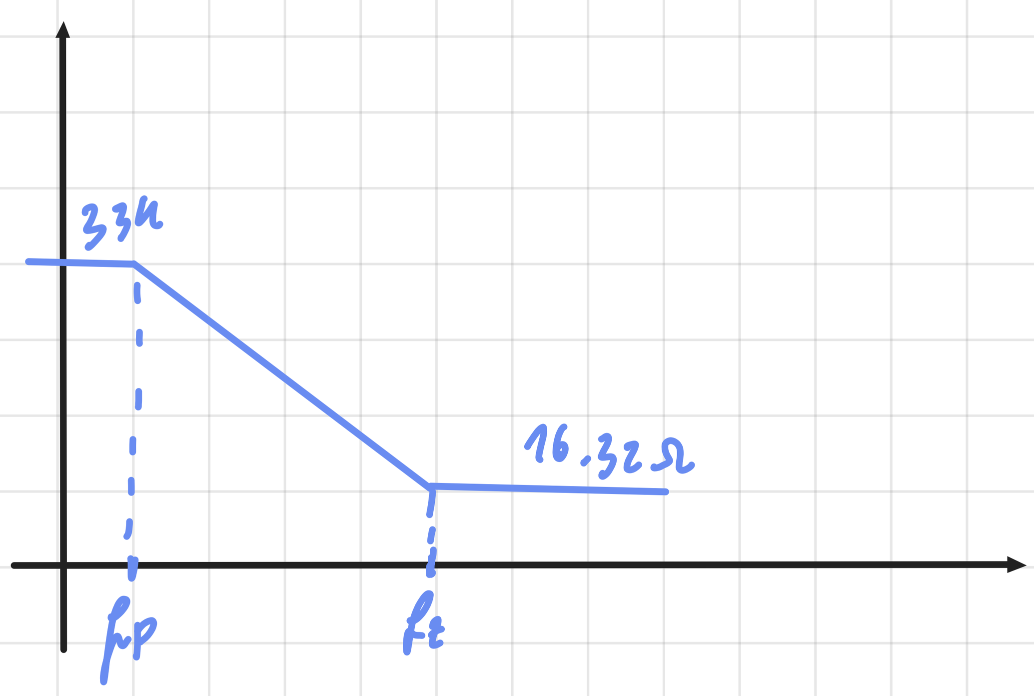
@ HF $\longrightarrow$ C_{short} $\quad i_A = \underbrace{\frac{V_A}{33k}}_{i_1} + \underbrace{\frac{V_A - V_C}{33k}}_{i_2}$



$$\left.\begin{aligned} V_B &= V_A\left(-\frac{660k}{33k}\right) \\ V_C &= V_B\left(1+\frac{470k}{4.7k}\right) \end{aligned}\right\} \quad V_C = V_A\left(-\frac{660k}{33k}\right)\left(1+\frac{470k}{4.7k}\right)$$

$$i_A = \frac{V_A}{33k} + \frac{V_A - V_A\left(-\frac{660k}{33k}\right)\left(1+\frac{470k}{4.7k}\right)}{33k}$$

(I) $\hookrightarrow$

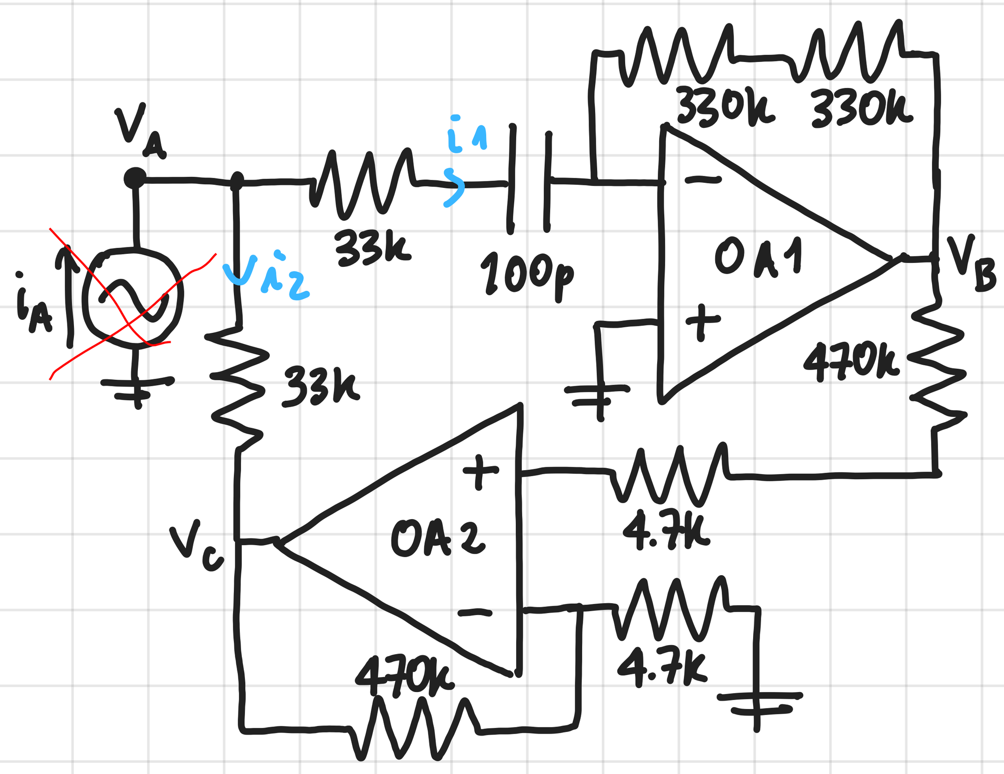


$$\left.\frac{V_A}{i_A}\right|_{HF} = \frac{33k}{2022} = 16{,}32\ \Omega$$

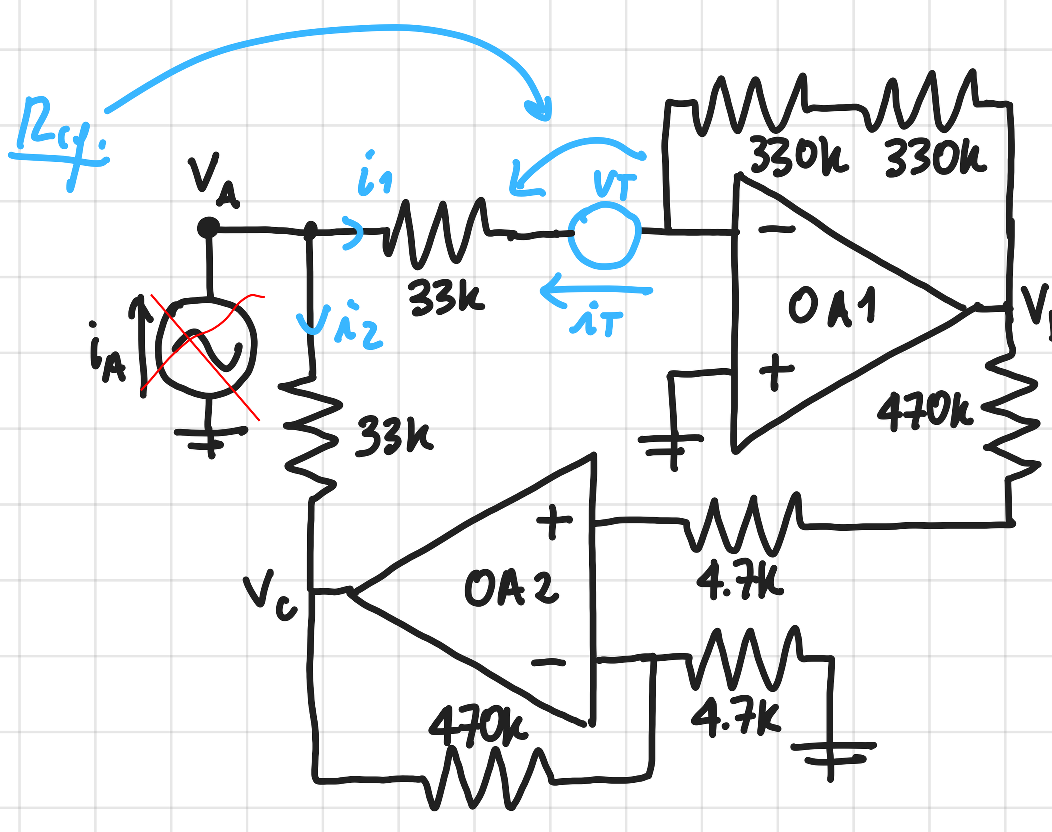
(II) $Z_{IN} = \frac{Z_{in\_no\,feedback}}{1 - G_{loop}}$ @ DC $\begin{cases} Z_{in,nf} = 33k \\ G_{loop}(0) = 0 \end{cases}$ @HF $\begin{cases} Z_{in,nf} = 33k // 33k \\ G_{loop}(\infty) = \left(1+\frac{470k}{4.7k}\right)\left(-\frac{660k}{66k}\right) = -1010 \end{cases}$

$\hookrightarrow Z_{in,HF} = \frac{33k//33k}{1-(-1010)} = 16.32\ \Omega$

b) $\frac{V_A}{i_A}(f) = ?$ $\longrightarrow$ Bode



$\longrightarrow$



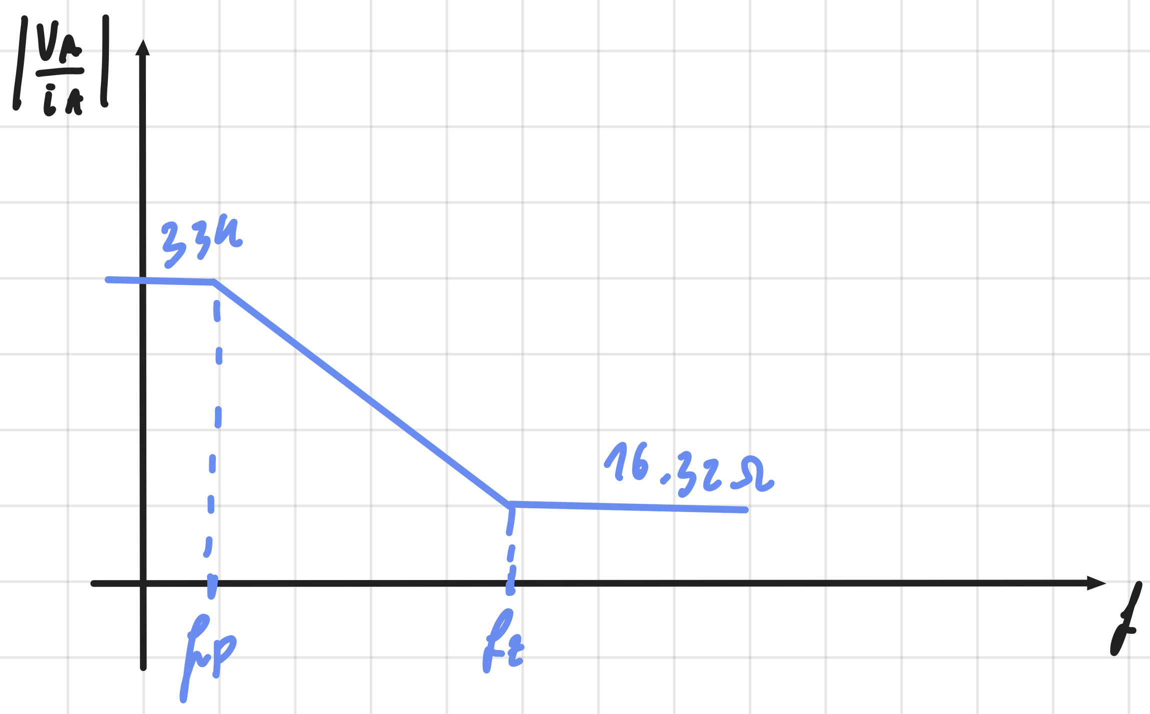
$R_{eq} \triangleq \frac{V_T}{i_T}$

$V_C = V_T - i_T(66k)$

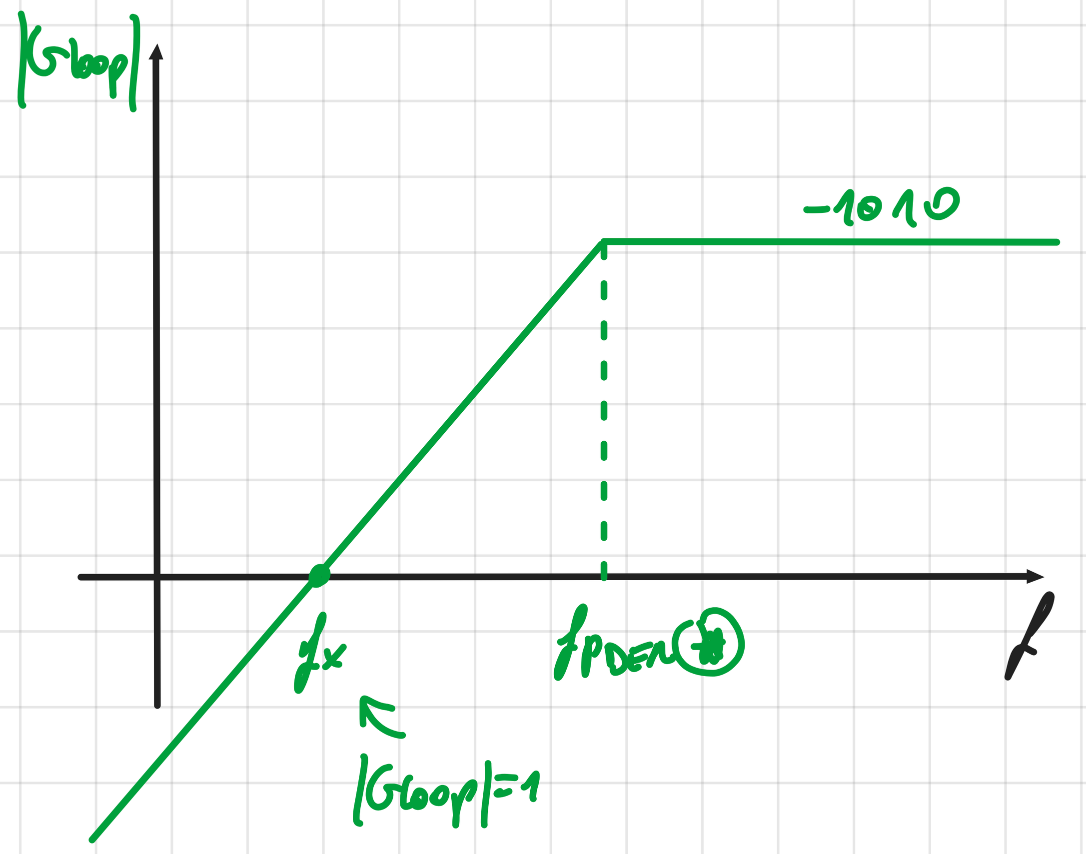
$\begin{cases} V_C = V_B \cdot 101 \\ V_B = i_T\, 660k \end{cases} \Rightarrow V_C = i_T\, 660k \cdot 101$

$\hookrightarrow i_T\, 660k \cdot 101 = V_T - i_T(66k) \Rightarrow R_{eq} = 66.72\,M\Omega$

↳ **Pole:** $f_p = \frac{1}{2\pi C R_{eq}} = 23.37\ Hz$ (C = 100p)

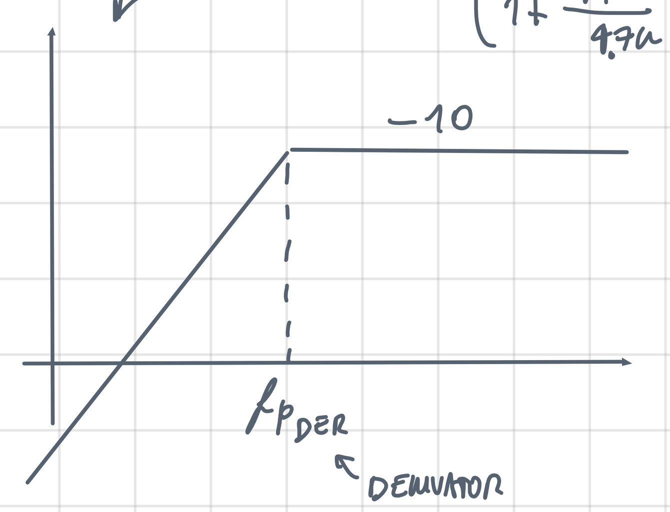


Obs. We saw that Gloop:



→ $G_{loop} = \underbrace{\frac{V_B}{V_C}\Big|_{ideal}}\cdot\underbrace{\frac{V_C}{V_B}\Big|_{ideal}}$

$\left(1+\frac{470k}{4.7k}\right) = 101$



(*) → $f_{PDER} = \frac{1}{2\pi\, 100p\, 66k} = 24.11\ kHz$

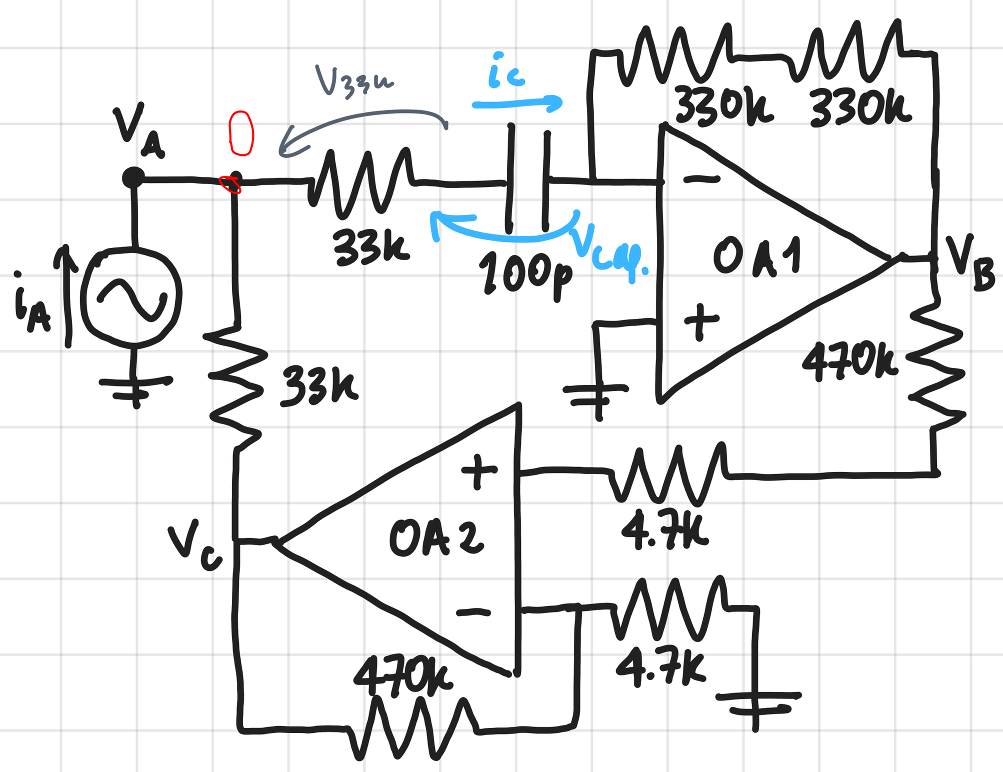
↳ We want to compute f_x in order to see when Gloop takes action on the circuit (i.e. when Gloop > 1)

→ $f_x = \frac{24.11kHz}{(10\cdot 101)} = 23.87\ Hz$

↳ Methods to find f_z

(I) graphically $f_z = \frac{Z_{in}(0)}{Z_{in}(\infty)} f_p = 48.22\ kHz$

(II) compute it from the circuit



$V_{cap} + V_{33} = 0$

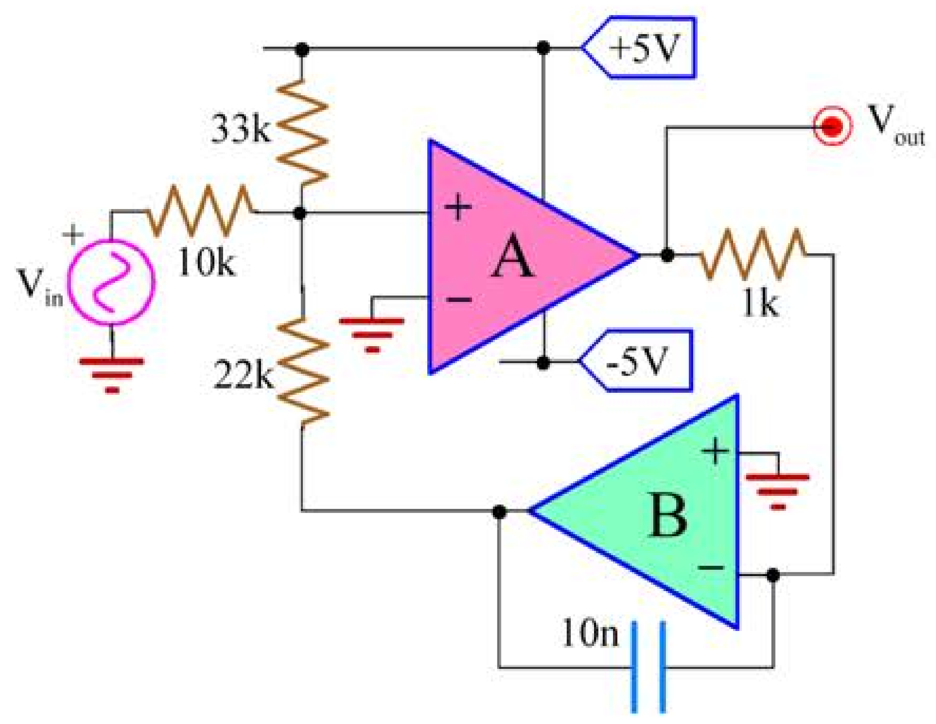
$V_{cap} + V_{cap}\, sC\, 33k = 0 \longrightarrow s = \frac{1}{C\cdot 33k}$

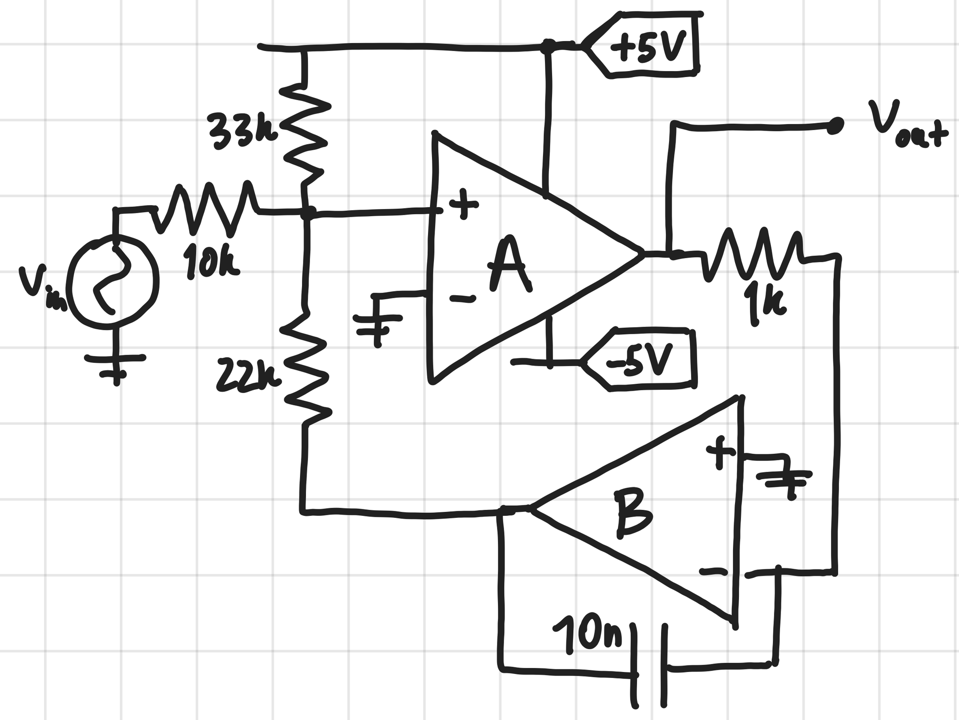
↳ $f_z = \frac{1}{2\pi\cdot 100p\, 33k} = 48.22\ kHz$

2

Ex. 2

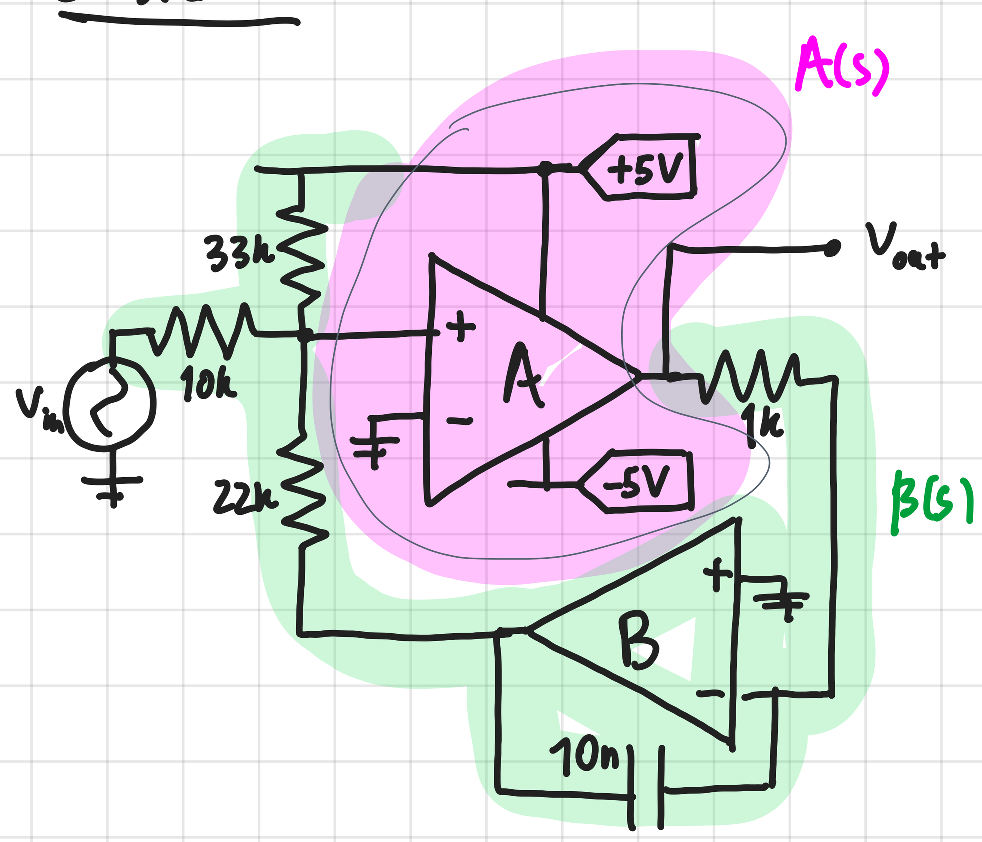
OpAmps with A0=100dB and GBWP=50MHz.
a) Check the stability of the stage, when both OpAmps are considered real.
b) Plot the ideal and the real Vout(f)/Vin(f) gains.
c) Propose a way to compensate the stage if needed.



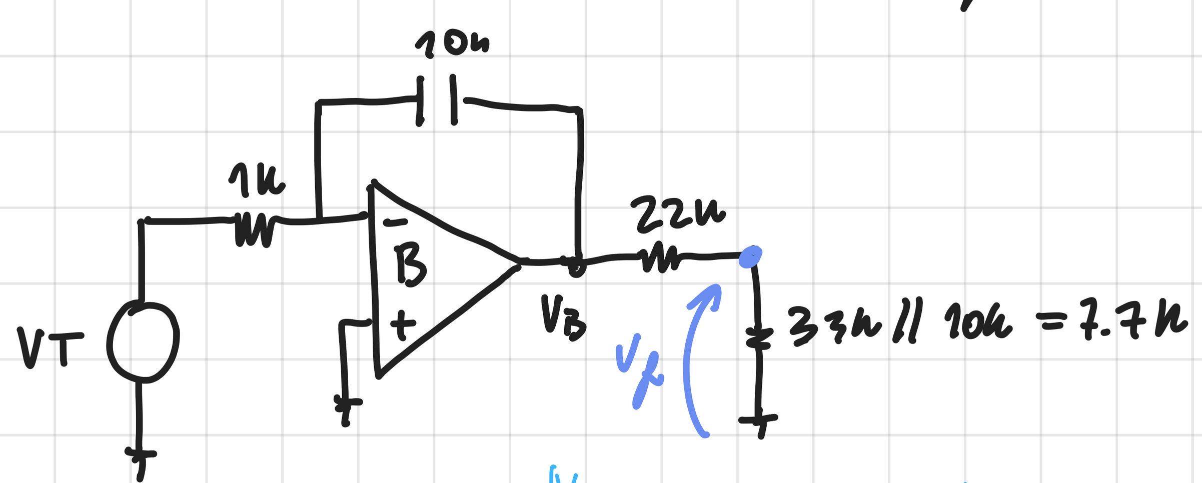


a) Stability?

Consider:

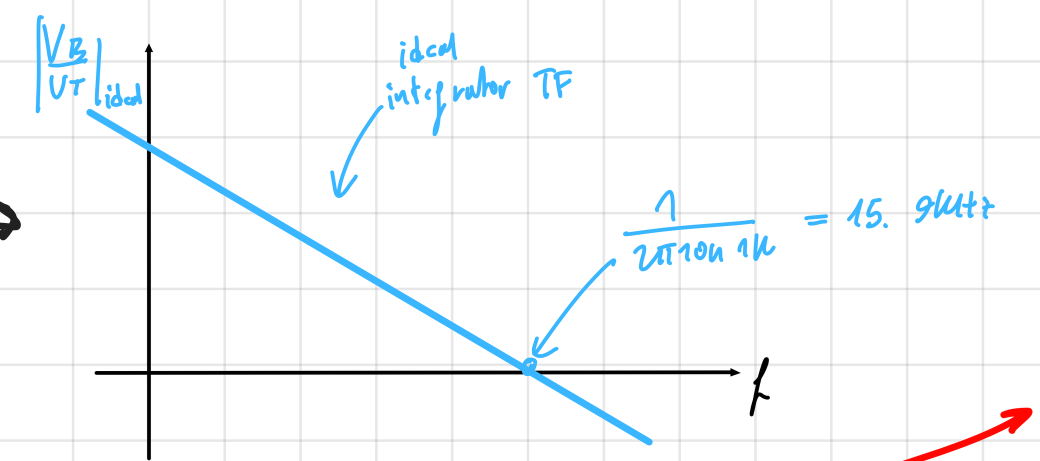


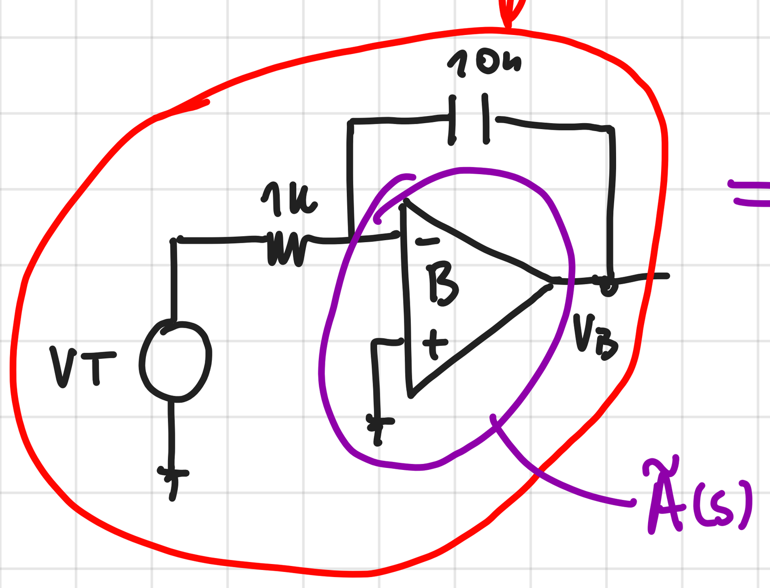
• $\beta(s)$ (switch off P.S. and all the Voltage sources and apply a test volt. V_T)



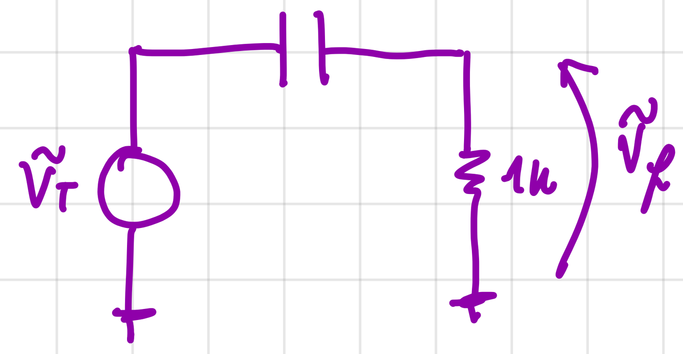
$\beta(s) = \frac{V_f}{V_T}$ ⟶ $\beta(s) = \left.\frac{V_B}{V_T}\right|_{real} \cdot \frac{7.7k}{7.7k + 22k}$

↳ $\left.\frac{V_B}{V_T}\right|_{ideal}$ ⟹





⟹ $\tilde{\beta}(s)$

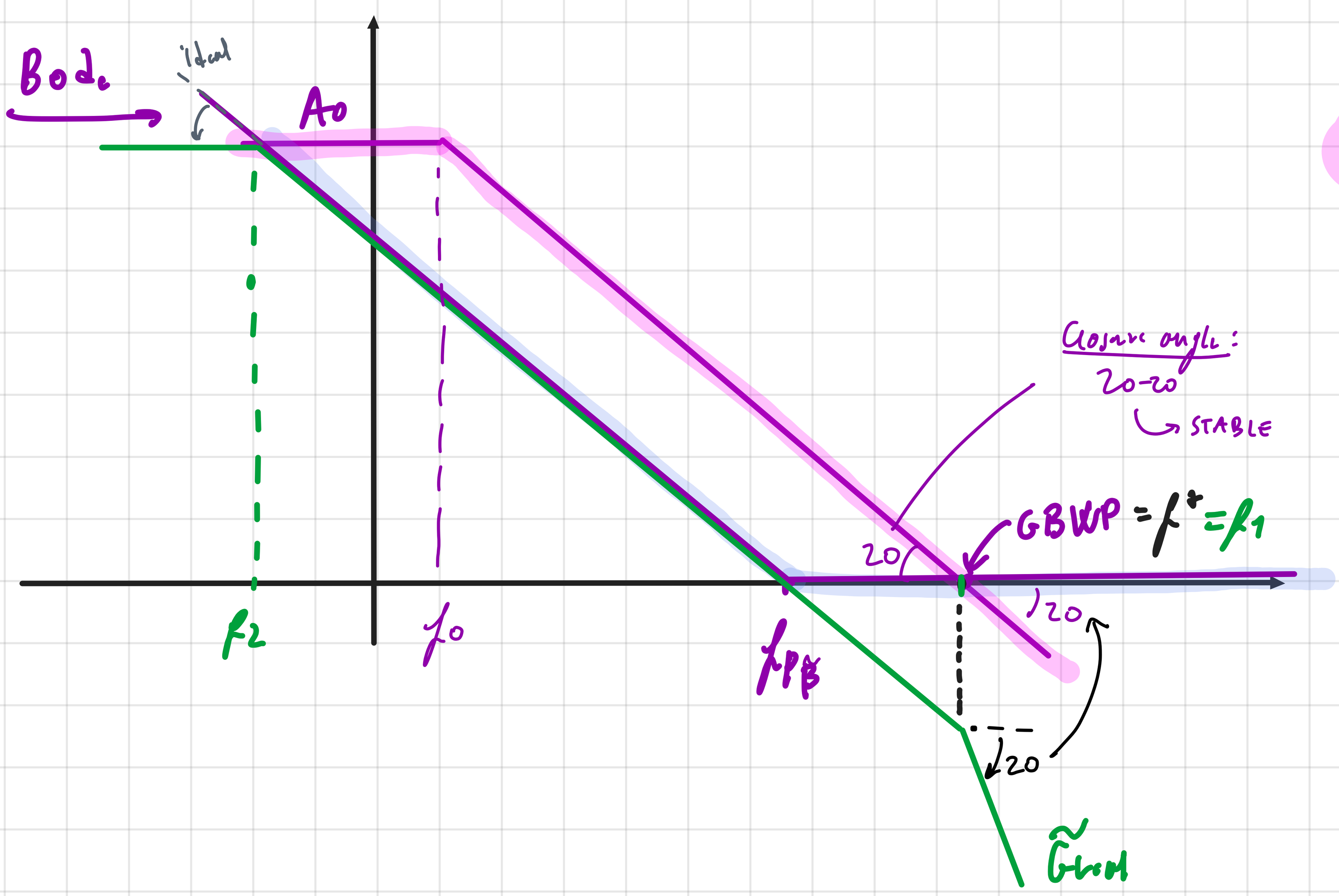


↳ To compute $\left.\frac{V_B}{V_T}\right|_{real}$ we consider this circuit and for it we analyze again $\tilde{A}(s)$ and $\tilde{\beta}(s)$

↳ • $\tilde{\beta}(0) = 0$ ⟶ $\frac{1}{\tilde{\beta}(0)} = \infty$

• $\tilde{\beta}(\infty) = 1$ ⟶ $\frac{1}{\tilde{\beta}(\infty)} = 1$

$f_{\tilde{\beta}} = \frac{1}{2\pi\, 10n\, 1k} = 15.9\ kHz$



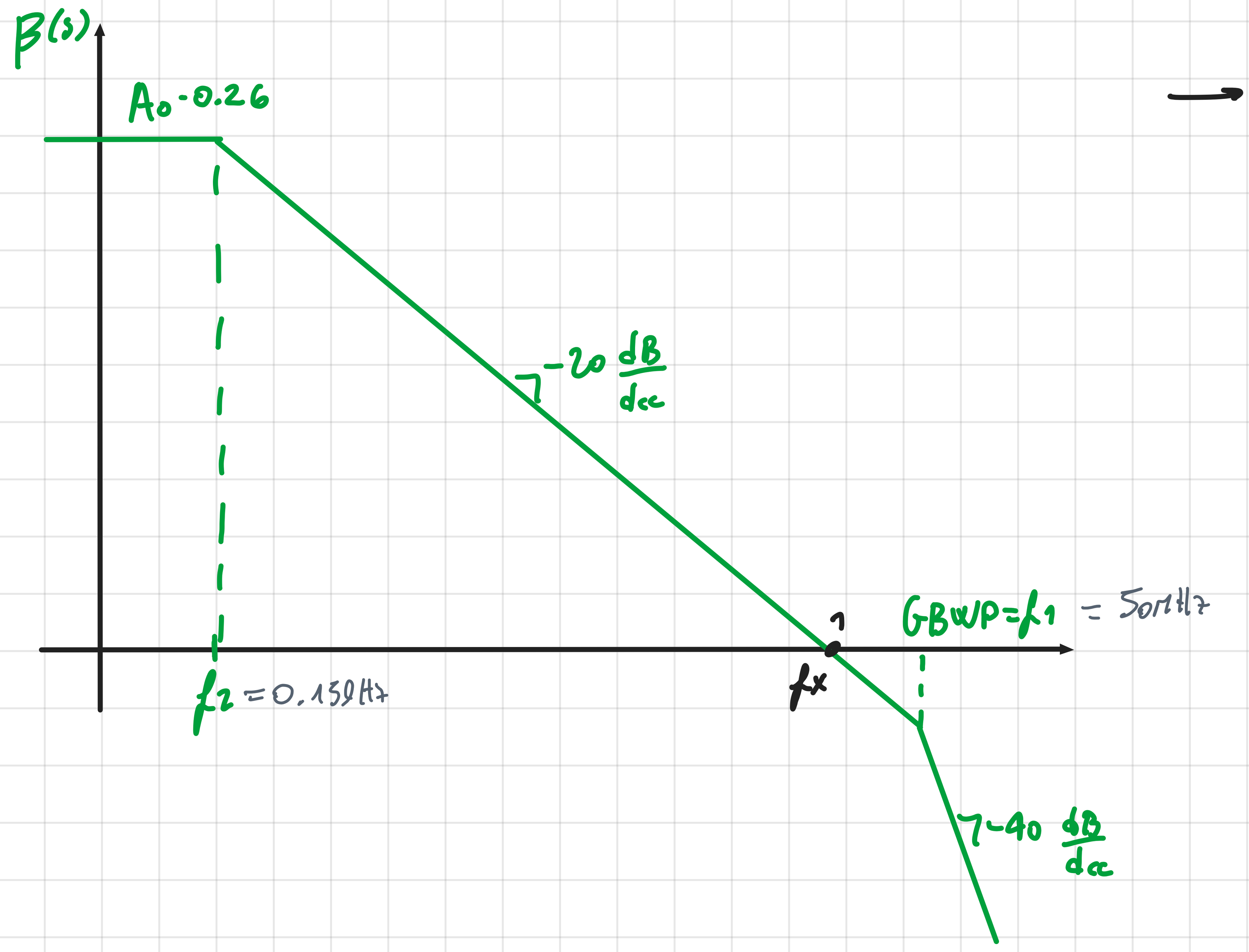
$\tilde{A}(s)$

$\frac{1}{\tilde{\beta}(s)}$

⟶ $f_2 = \frac{f_{P\tilde{\beta}} \cdot 1}{A_0} = 0.159\ Hz$

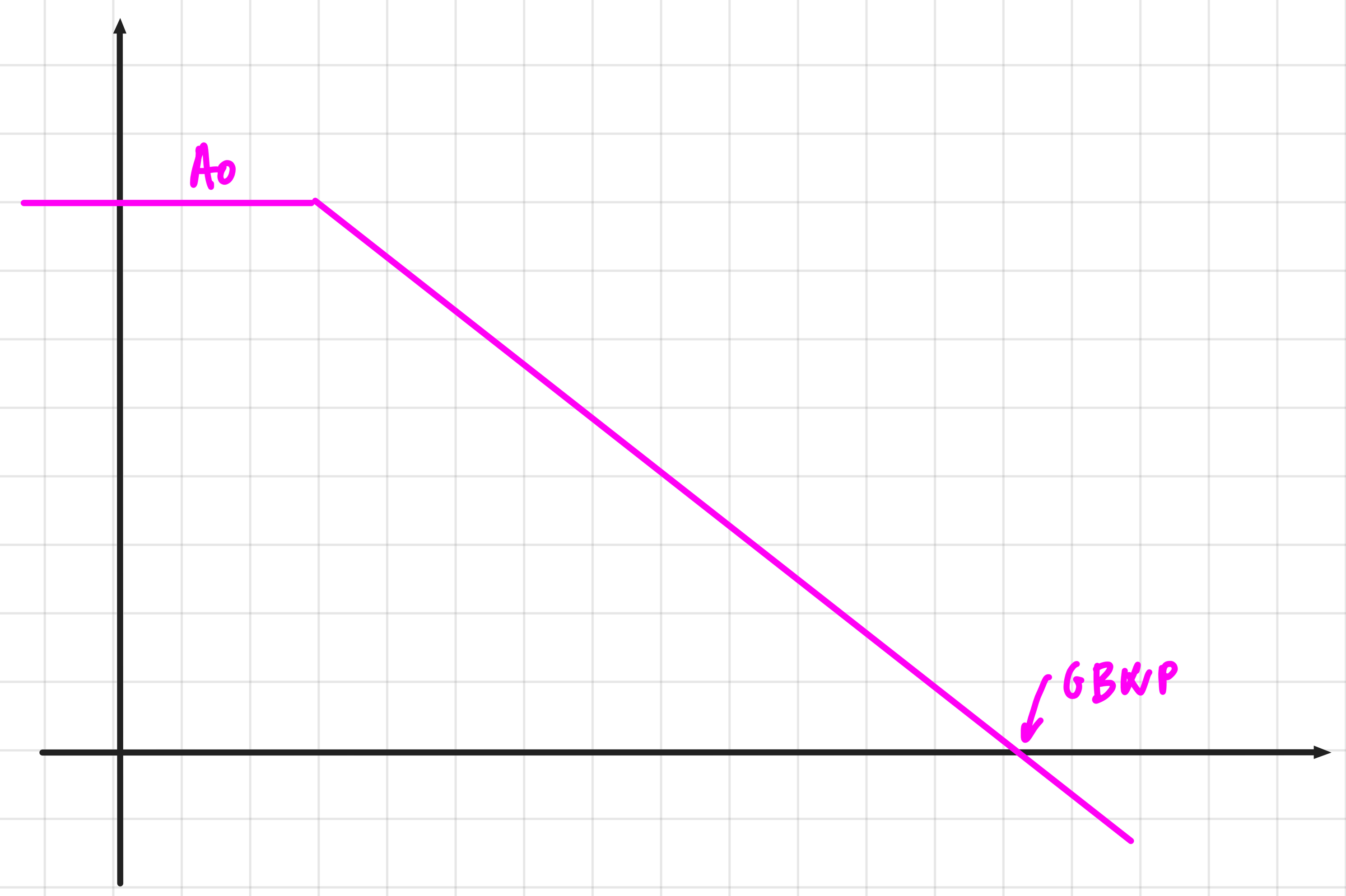
→ Then we can derive $\beta(s)$ from:

$$\beta(s) = \underbrace{\frac{V_B}{V_T}\Big|_{ideal}}_{G_{ideal}} \cdot \underbrace{\frac{7.7k}{7.7k+22k}}_{0.26}$$

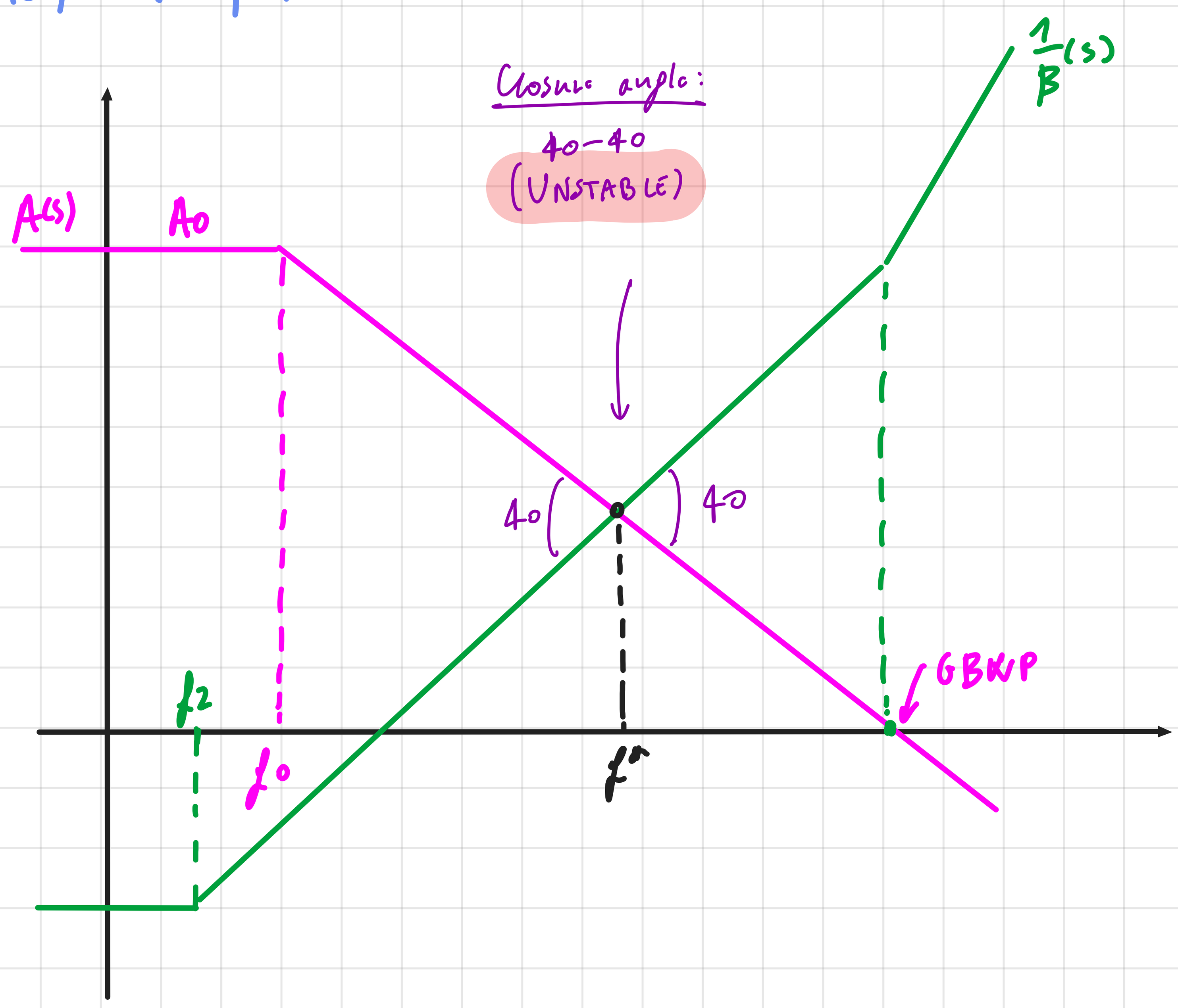


→ $f_x = A_0 \cdot 0.26\, f_2 = 4.1\,kHz$

• A(s)

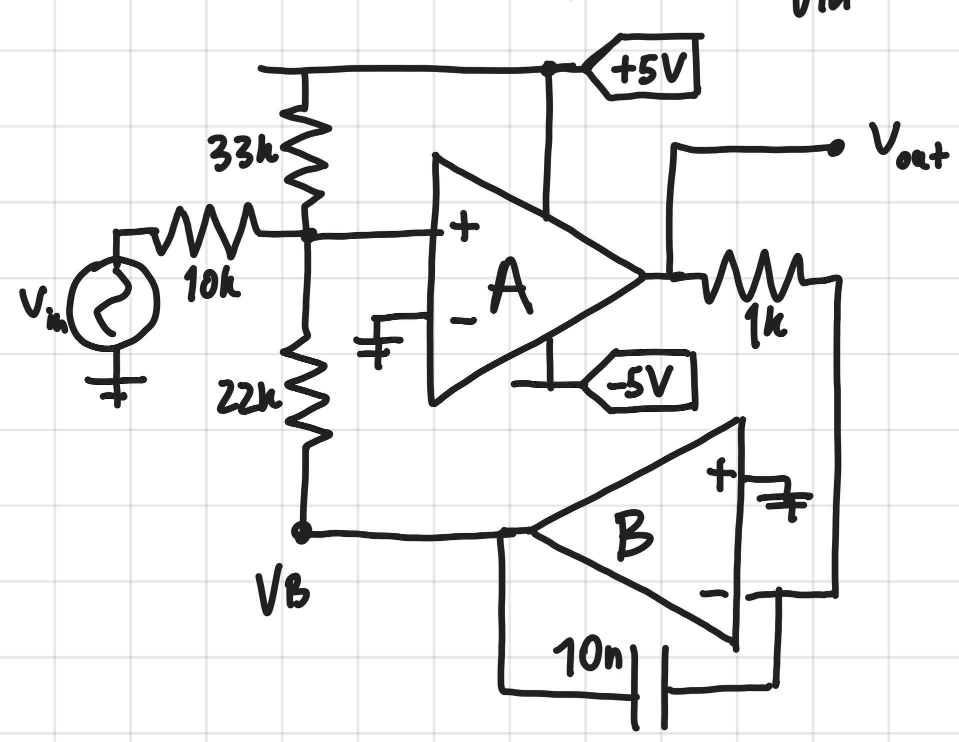


⇒ Bode $G_{loop} = A(s)\cdot\beta(s)$



→ $f^* = \sqrt{f_x \cdot GBWP} = 454\,kHz$

b) Ideal and real gain $\frac{V_{out}}{V_{in}}$



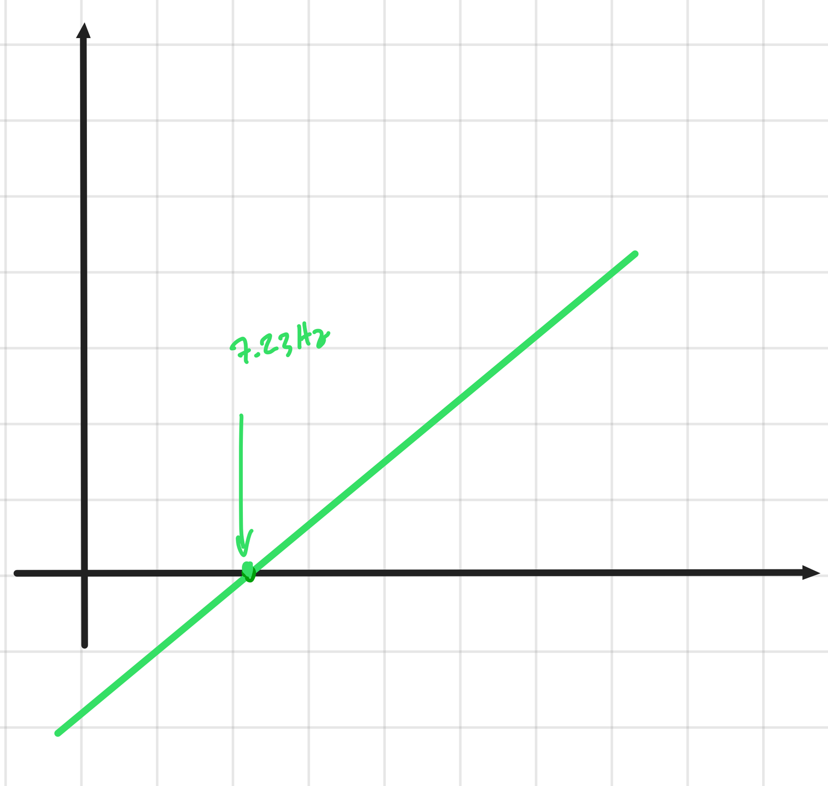
ideal

• $\frac{V_B}{V_{IN}} = -\frac{22k}{10k} = -2.2$

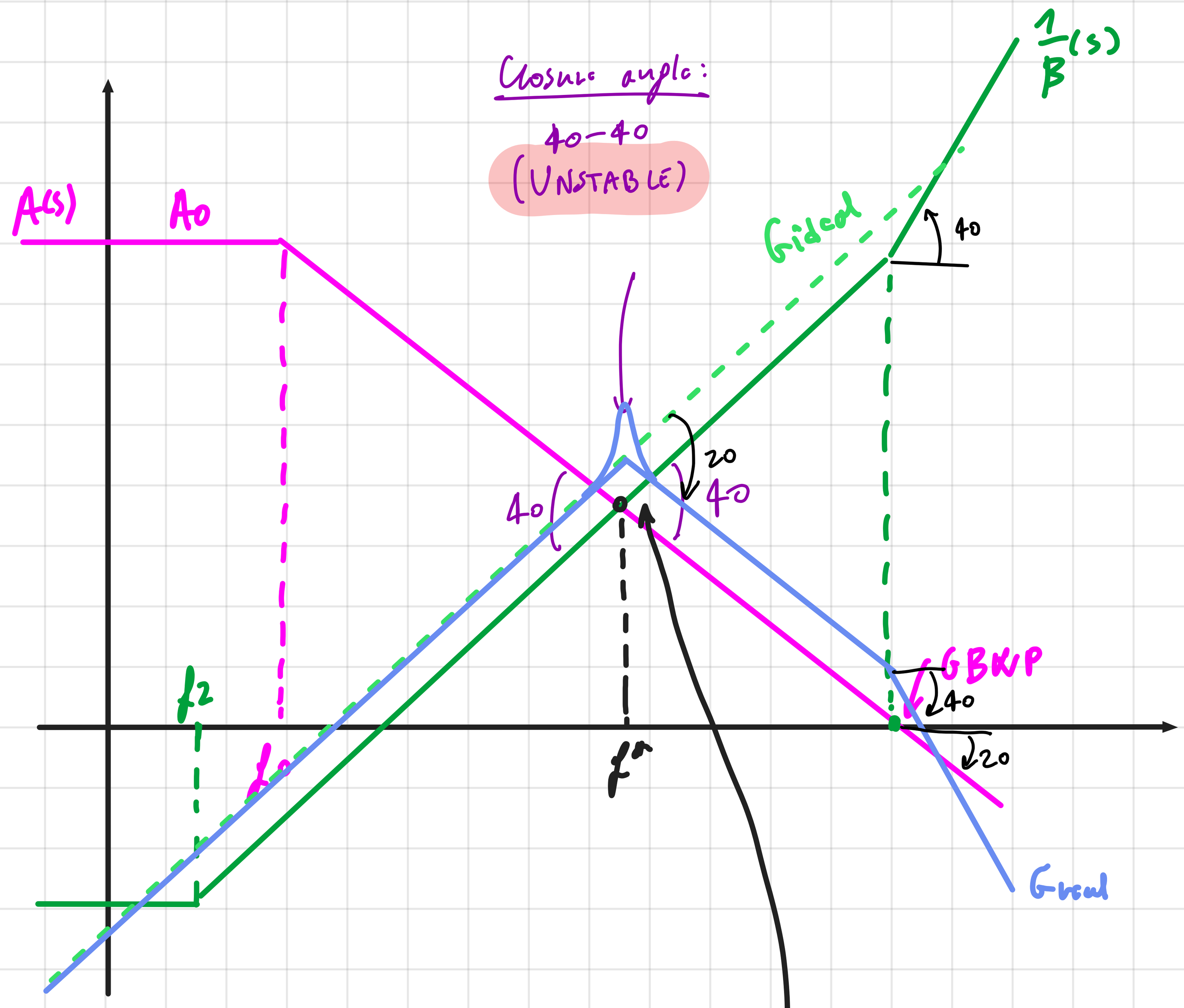
• $\frac{V_{out}}{V_B} = -s\cdot 10n\cdot 1k$

$\frac{V_{out}}{V_{in}}\Big|_{ideal} = s\cdot 10n\cdot 2.2k$ (derivator)

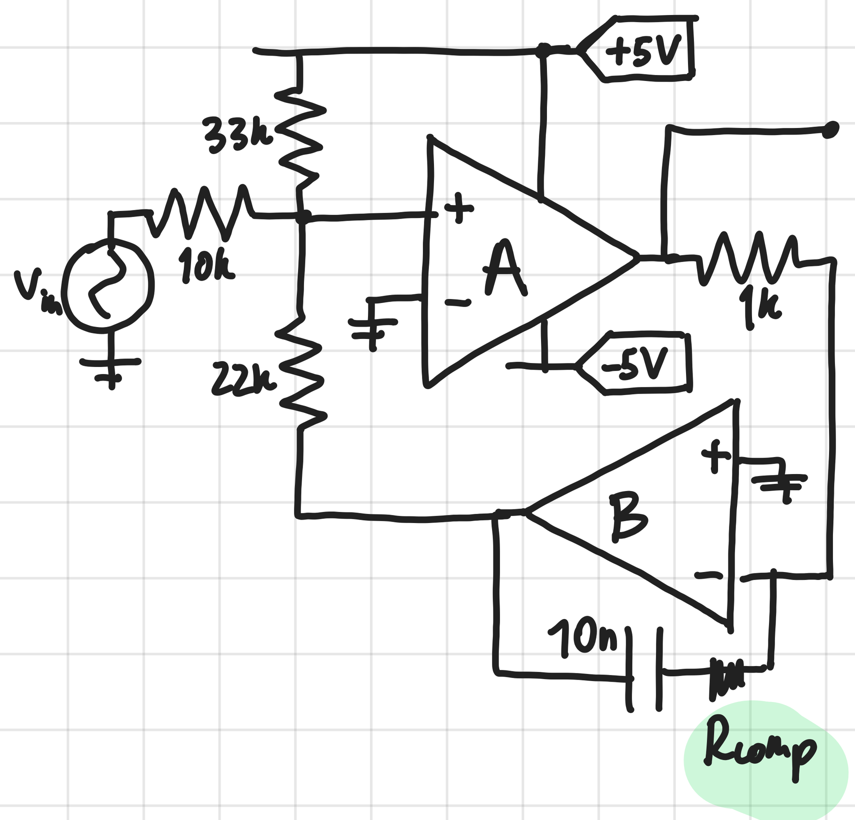
Obs. $\frac{V_{out}}{V_{in}}\Big|_{ideal} = 1$ for $f = \frac{1}{2\pi C\, 2.2k} = 7.23\,kHz$



↳ The real gain depends on the stability of the loop :



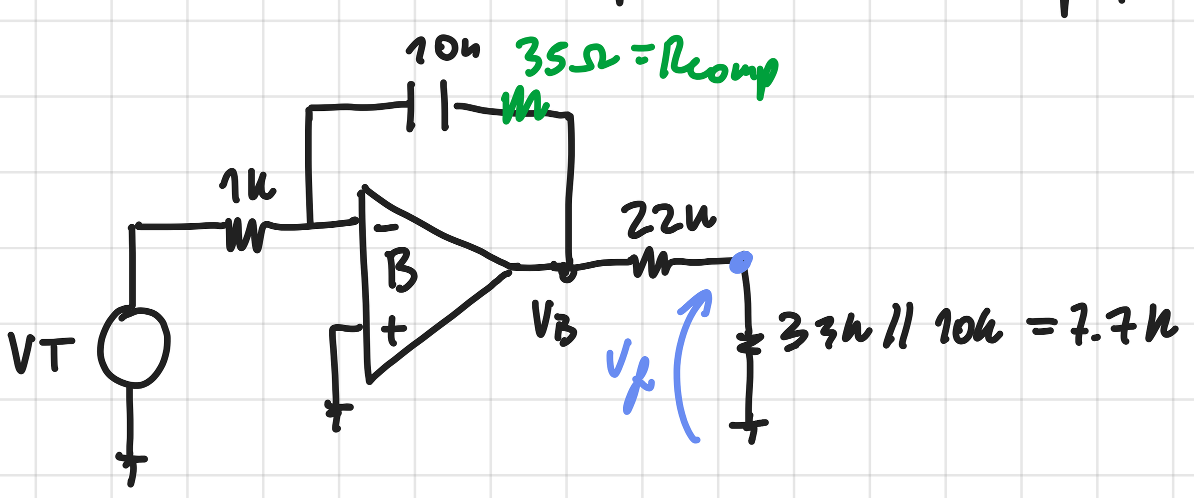
c) We would like to compensate this instability a good way could be to introduce a pole (in f^*) in the ideal gain in order to have a closure angle of 40−20 → marginally stable (PM = 45°)



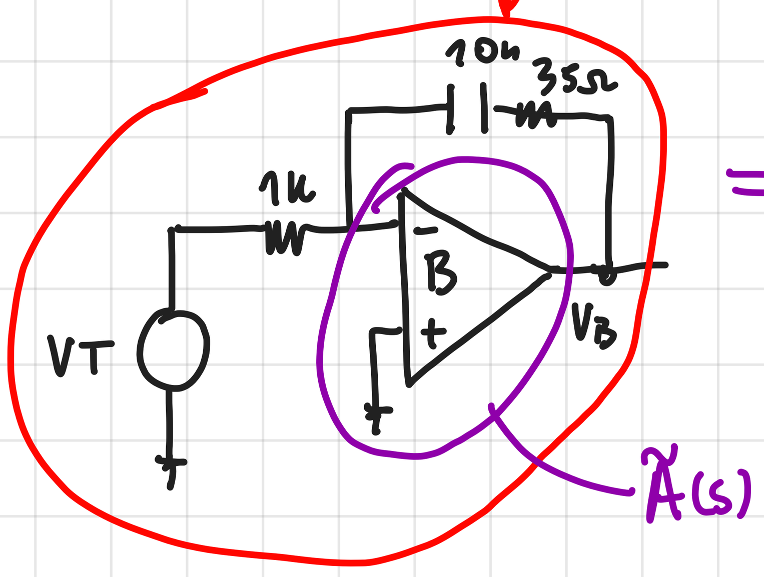
→ R_{comp}

$$f_{comp} = f^* = \frac{1}{2\pi R_{comp} C} \longrightarrow R_{comp} = \frac{1}{2\pi C f^*} = 35\,\Omega$$

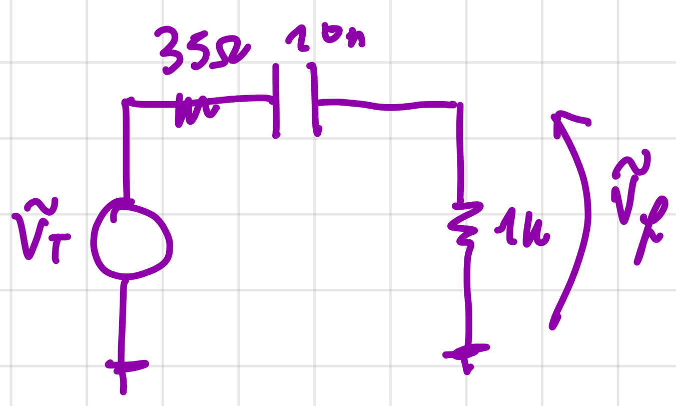
↳ We have to reperform the computations



$$\longrightarrow \beta(s) = \left.\frac{V_B}{V_T}\right|_{real} \cdot \overbrace{\frac{7.7k}{7.7k + 22k}}^{0.26}$$



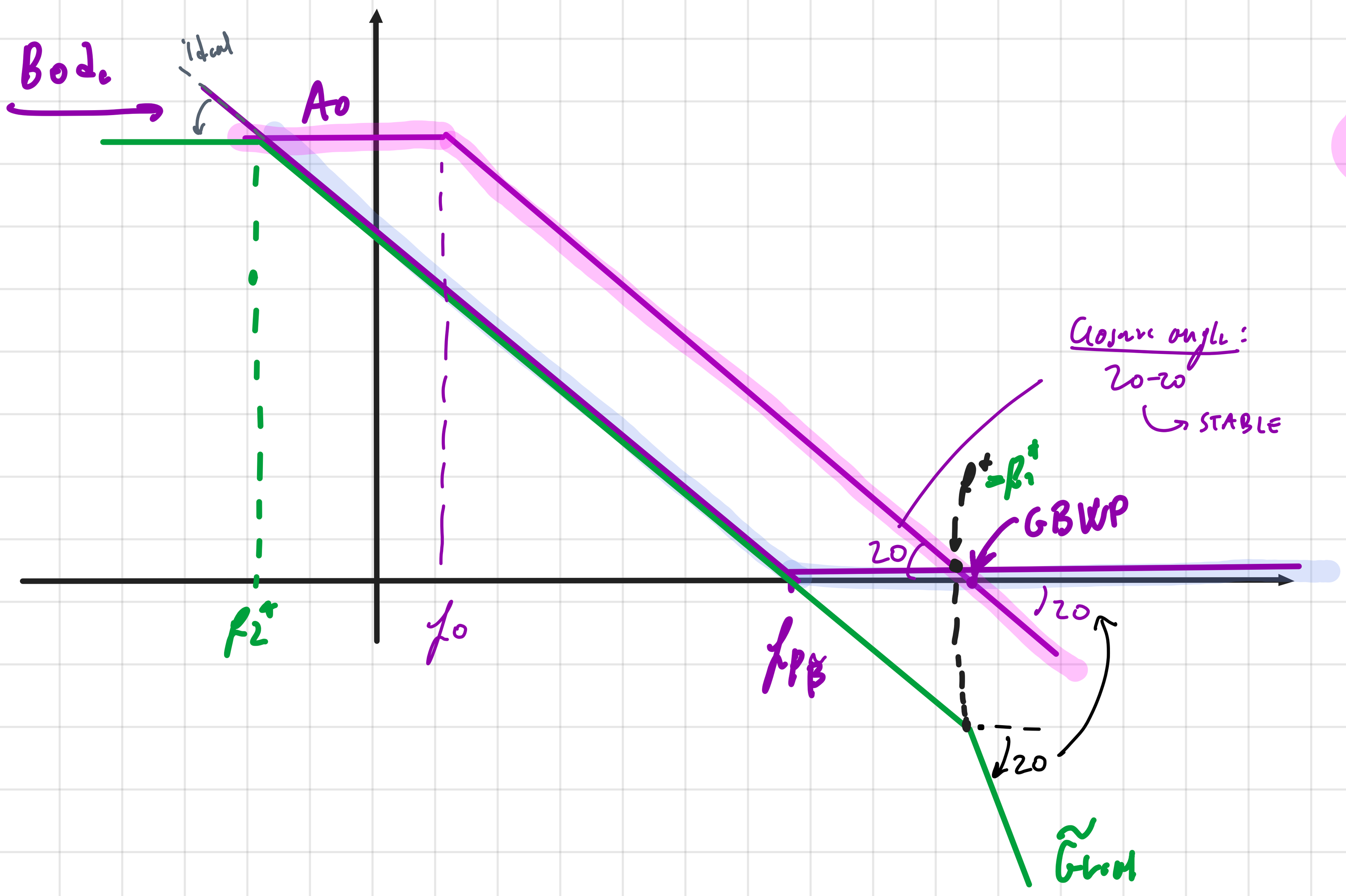
$\Rightarrow \tilde{\beta}(s)$



↳ • $\tilde{\beta}(0) = 0$

• $\tilde{\beta}(\infty) = \frac{1k}{1k + 35\Omega} = \frac{1}{1{,}035}$

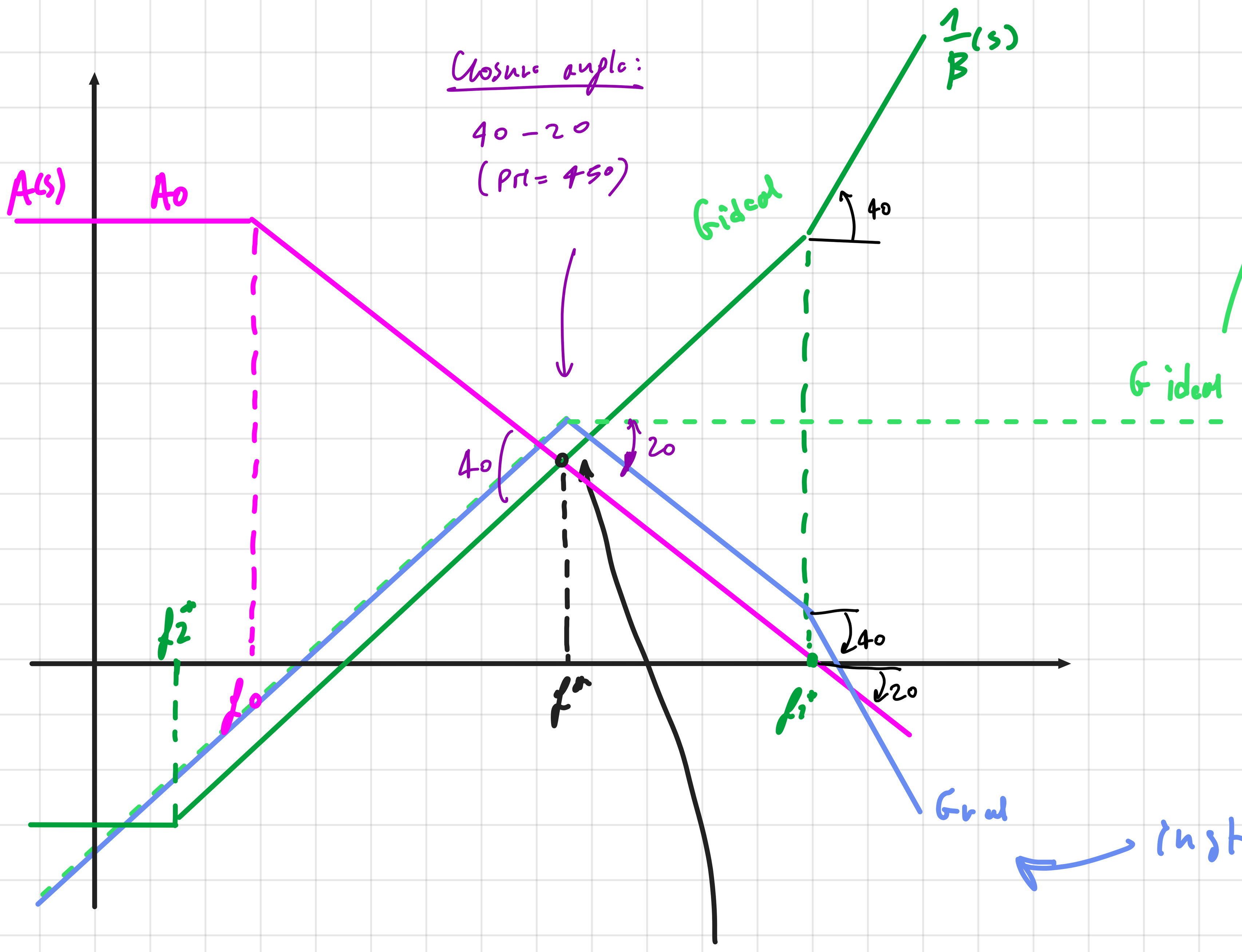
↳ $f_{p\tilde{\beta}} = \frac{1}{2\pi(1k + 35\Omega)\,10n} = 15{,}3\,kHz$



→ $f_2^* = \frac{f_{p\tilde{\beta}}}{A_0 \cdot 1{,}035} = 0.148\,Hz$

$f^* = f_1^* = \frac{GBWP}{1{,}035} = 48{,}3\,MHz$

↳ Greal



Gideal : @ HF $\left.\frac{V_{out}}{V_{in}}\right|_{ideal} = 62.8$

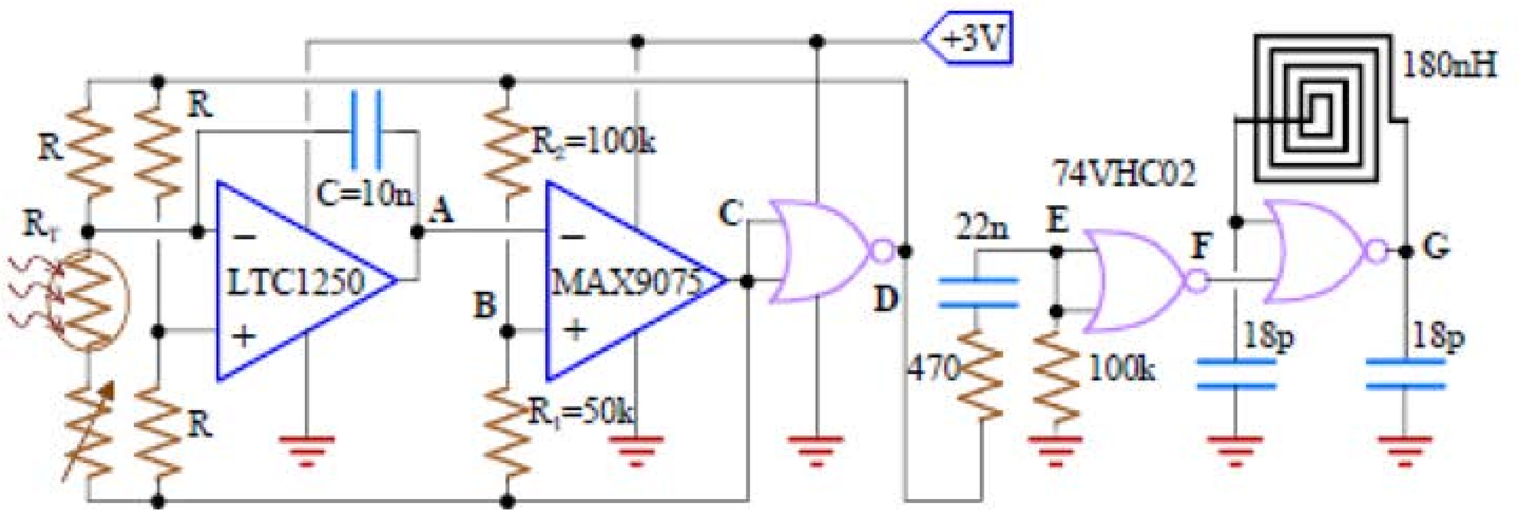
$$\begin{cases} \frac{V_B}{V_{in}} = 2.2 \\ \frac{V_{out}}{V_B} = \frac{1k}{35} \end{cases}$$

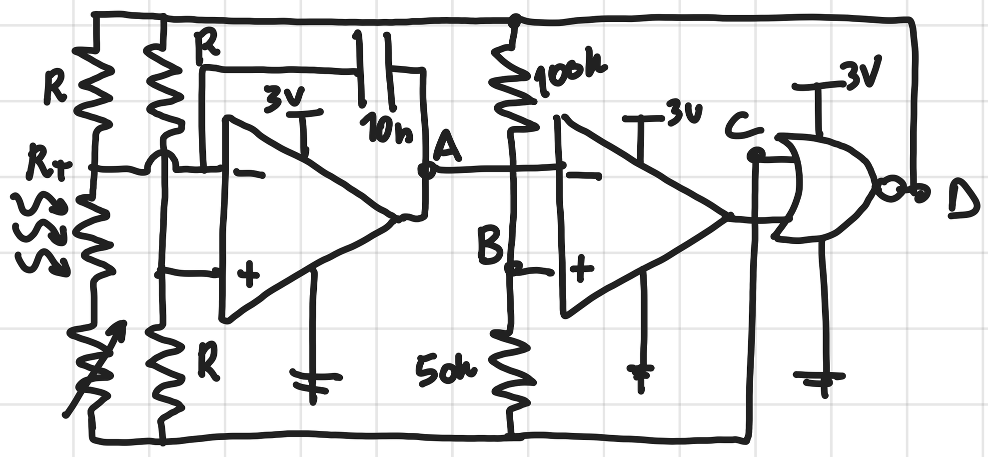
instability has been compensated

③

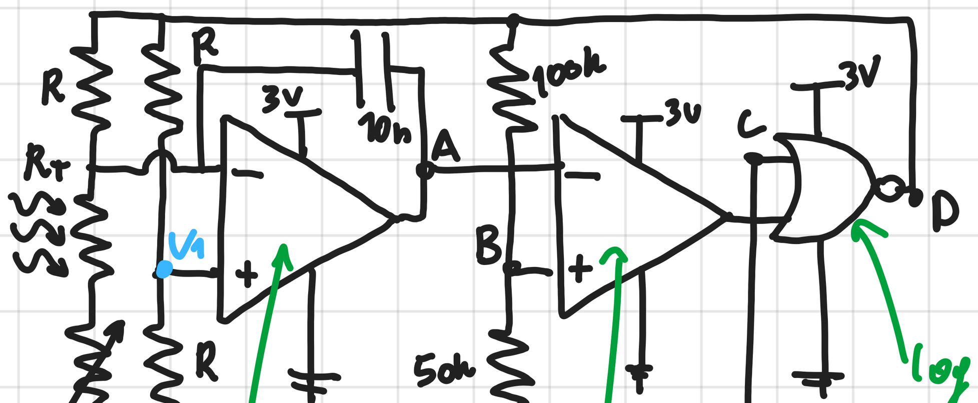
Ex. 3

The telemetry transmitter employs a sensor R_T=1kΩ with a signal fluctuation r/R_T =0.1%. The trimmer is used just to perfectly balance the bridge when no signal is applied. Hint: start when VC(0)=0V.
a) Find the two thresholds of the comparator and the corresponding currents through the 10nF capacitor.
b) Draw the voltage waveforms at nodes A, B, C, D, and compute the oscillation period at node C as a function of the signal r/R_T and C. Say if the front end is "ratiometric" or not (i.e. the output is independent of VDD).
c) Draw the voltage waveforms at nodes E, F, G (hint: the last gate oscillates at 80MHz when enabled).





a)



Opamp (neg. feedback)

Comparator

logic port NOR

• $\underline{V_{th1} \text{ and } V_{th2}}$

• low-comp. $V_C = 0V \longrightarrow V_D = 3V \longrightarrow V_B = \frac{3V \cdot 50k}{150k} = 1V$

• high-comp. $V_C = 3V \longrightarrow V_D = 0V \longrightarrow V_B = \frac{3V \cdot 100k}{150k} = 2V$

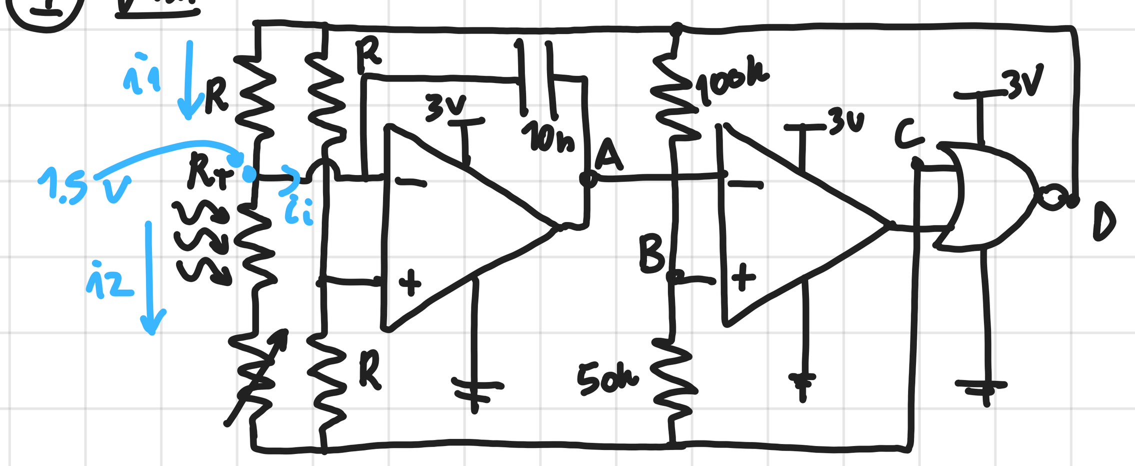
↳ when $V_1^+ = V_1^- = 3\frac{R}{R+R} = 1.5V = V_{th1}$

$(V_{th2} = -1.5V$ symmetric)

switching the P.S. up with the one down
$(V_D = 3 \to 0)$ $(V_D = 0 \to 3)$

• current through capacitor

Ⓘ V_{th1}



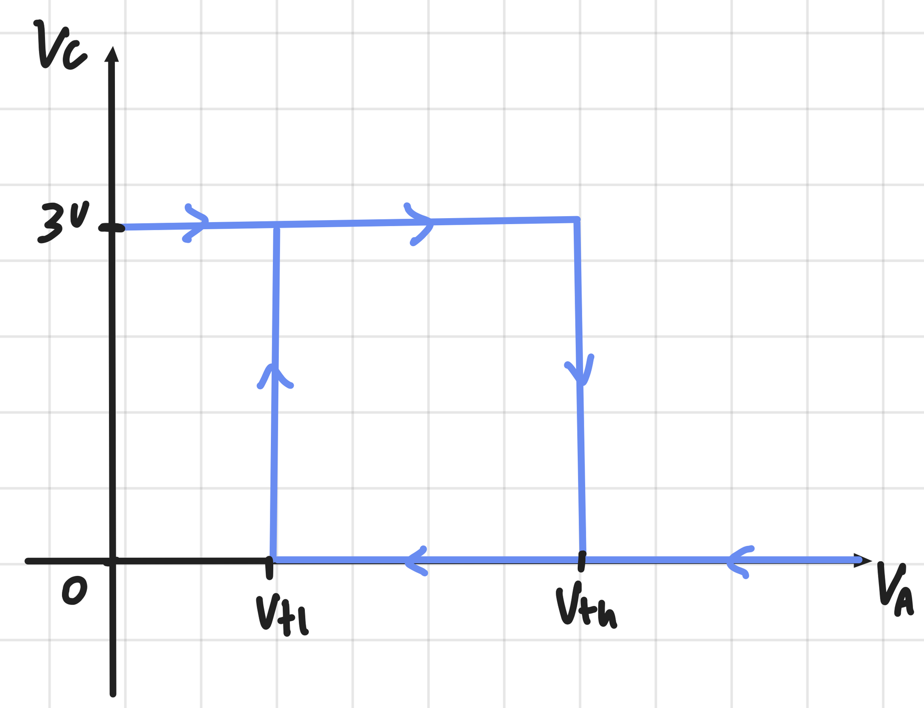
$i_1 = \frac{1.5V}{R}$ $\quad i_2 = \frac{1.5V}{R+r}$

↳ $i_i = i_1 - i_2 = \frac{(\cancel{R}+r-\cancel{R})\,1.5V}{R(R+r)} \cong 1.5\mu A$

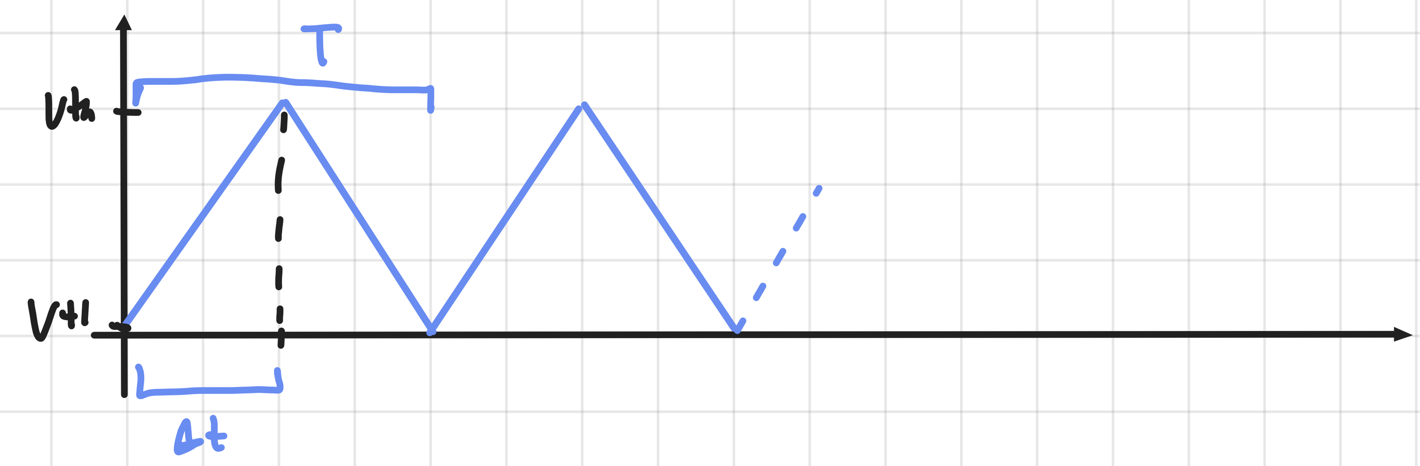
negligible $\quad \frac{r}{R} = 0.1\%$ $\quad (R = 1k\Omega)$

Ⓘⓘ $V_{th2} \longrightarrow i_1 = -\frac{1.5V}{R}$ $\quad i_2 = \frac{-1.5V}{R+r}$ $\longrightarrow i_i = -1.5\mu A$

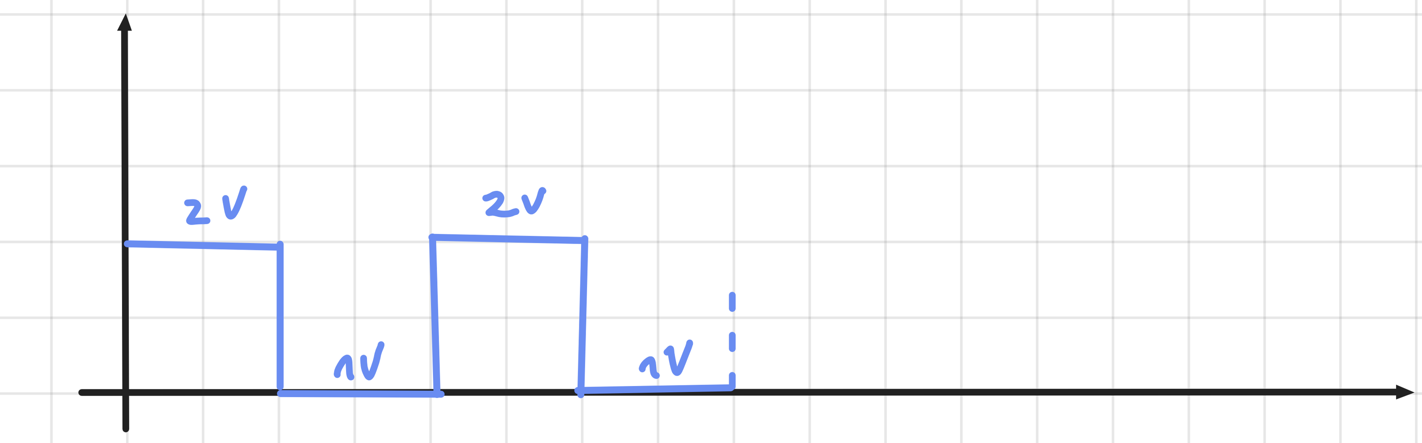
b)



Node A:



Node B:



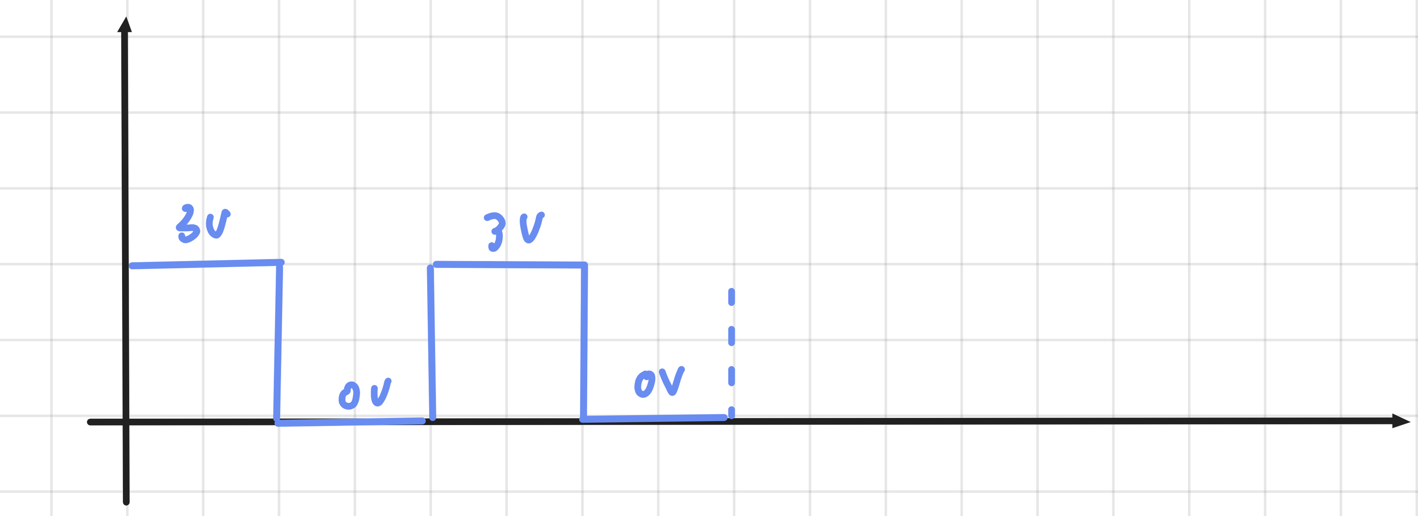
↳ To compute the oscillation period:

$\frac{\Delta V_A}{\Delta t} = \frac{i_i}{C}$

generic case (before $V_{DD}=3V$)

↳ $i_i = \frac{V_{DD}}{2} \cdot \frac{1}{R} - \frac{V_{DD}}{2}\frac{1}{(R+r)} = \frac{V_{DD}\, r}{2R(R+r)} \cong \frac{V_{DD}\, r}{2R^2}$

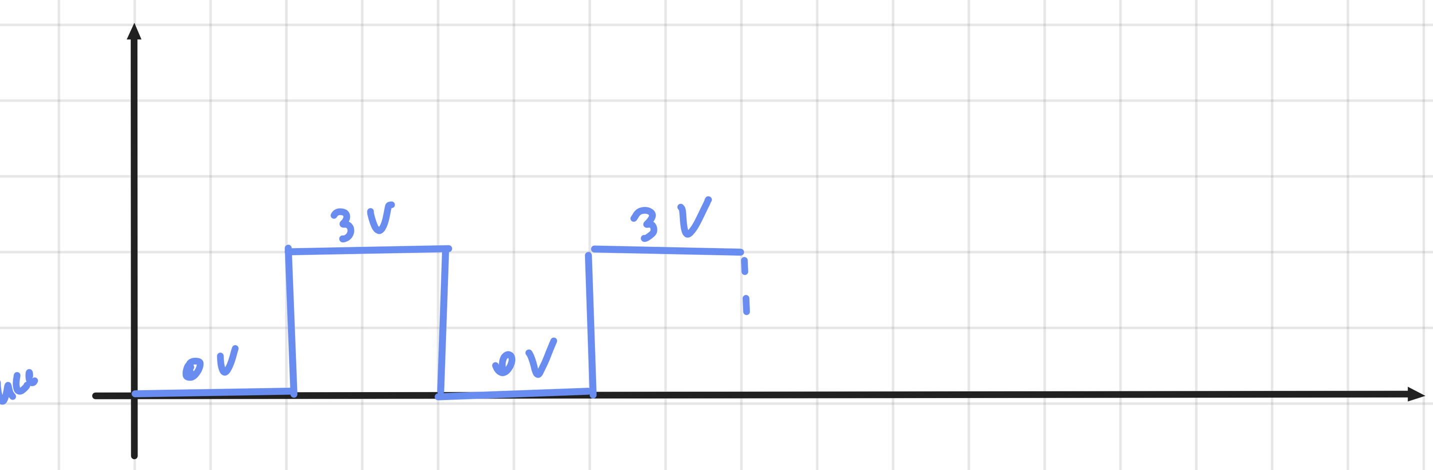
Node C



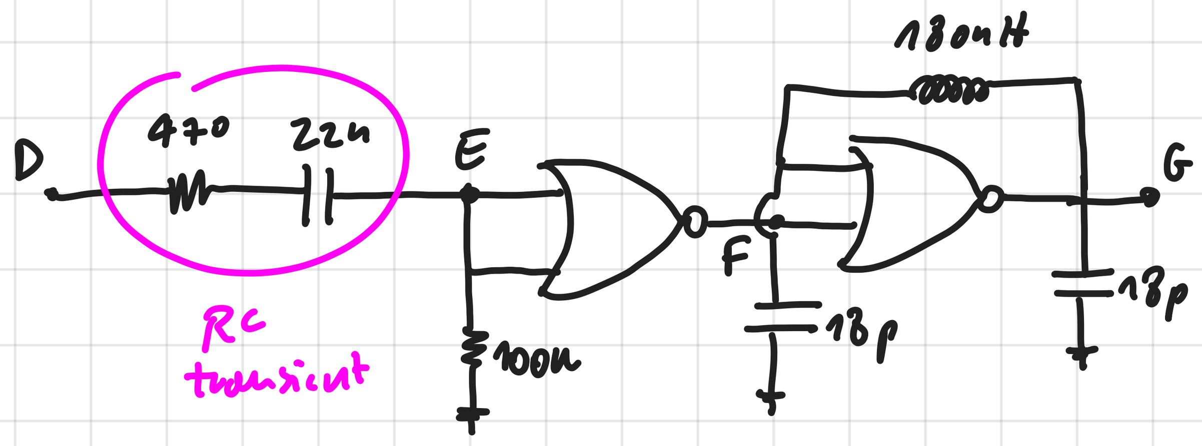
$\Delta V_A = V_{th} - V_{tl} = \frac{V_{DD} \cdot 100k}{150k} - \frac{V_{DD}\, 50k}{150k} = \frac{V_{DD}}{3}$

↳ $\frac{\Delta V_A}{\Delta t} = \frac{V_{DD}\, r}{2R^2 C}$

Node D



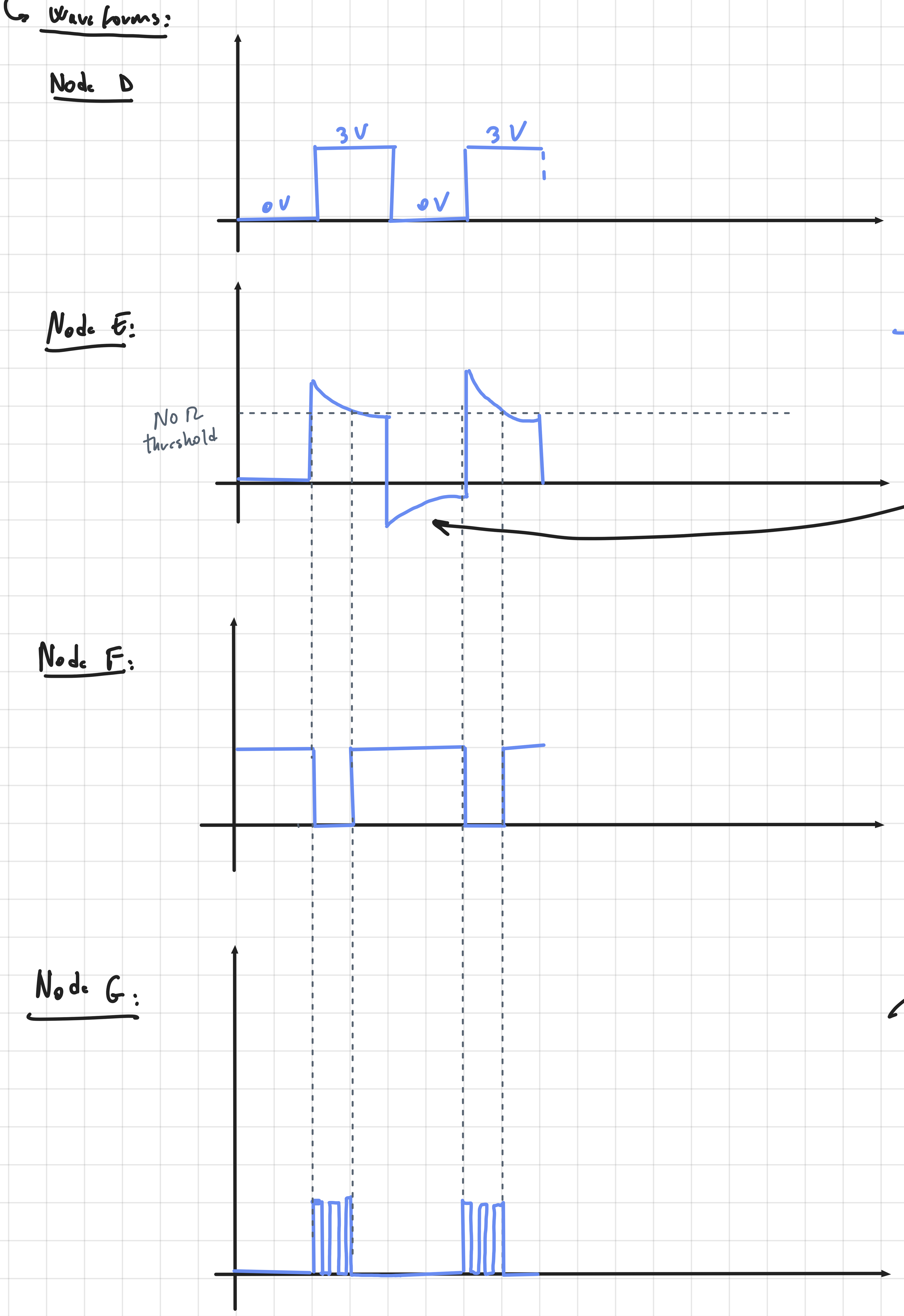
$\Rightarrow \Delta t = \frac{2}{3}\frac{R^2 C}{r}$ (no P.S. V_{DD} dependance) $\longrightarrow$ Period $T = 2\Delta t = \frac{4}{3}\frac{RC}{\frac{r}{R}}$ ← variation of resistance c)



↳ We want to compute the period of the transient due to the RC

↳ $\tau = C(100k + 470) \triangleq 2.2\,ns$

↳ Waveforms:



→ We are changing the capacitance but the $5\tau > \Delta t = \frac{T}{2}$ so at the end of the capacitor switch mode = 3V we'll still have some residual charge

↗ 80 MHz oscillation when G is enabled

Ex. 4

Reverse bias a photodiode at 3.3V and acquire its reverse current, in the 0-100 µA range, from DC to 10kHz.

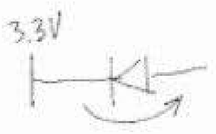
a) Every 100ms, detect the max intensity and restart.

b) Turn on an LED when the light varies faster than ±1µA/µs (both increasing and decreasing)

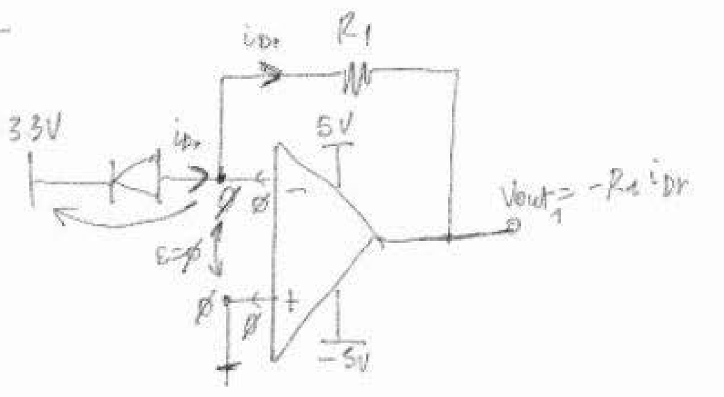
also look at prof sol. and see commments

Ex. 4 (ES1 Borla)

- Reverse bias a photo diode at 3.3V $\rightarrow$



- Acquire it's reverse current (in the 0-100µA range) $\rightarrow$

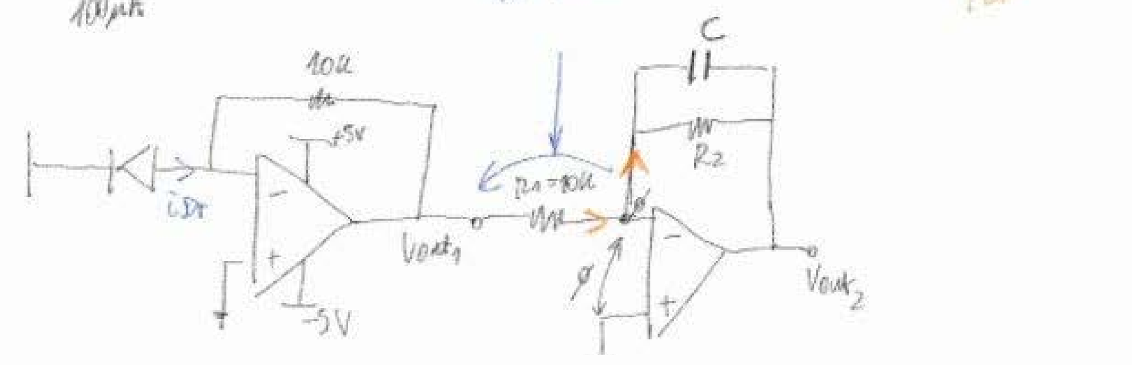


$\hookrightarrow$ to stay in 0-100µA $\quad -5V < V_{out_1} < 5V$

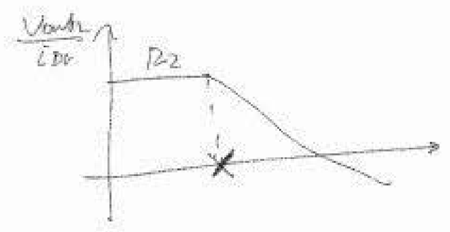
$\hookrightarrow$ choose $R_1 \ll \frac{5V}{100\mu A} = 10k$

so $V_{out_1} = -R_1 i_{Dr} \longrightarrow i_{Dr} = \frac{V_{out_1}}{R_1} = i_{Dr}$

- From DC to 10kHz $\longrightarrow$



@ DC $\quad V_{out_2} = -\frac{R_2}{R_1} V_{out_1} = -\frac{R_2}{R_1} \cdot (-R_1) i_{Dr} = \underbrace{R_2}_{G_{DC}} i_{Dr}$



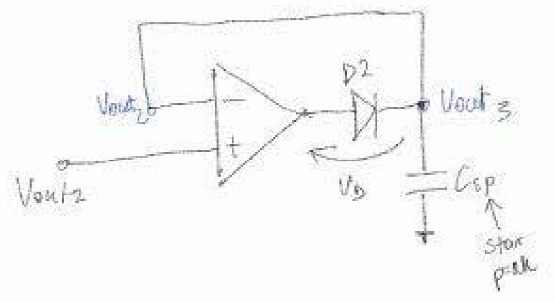
@ AC $\quad V_{out_2} = 0 \rightarrow G_{AC} = 0$

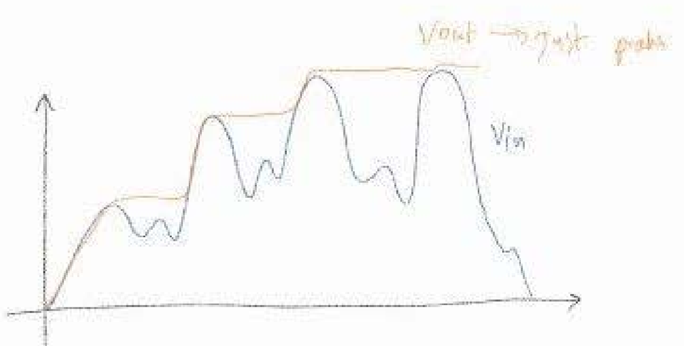
pole $\rightarrow \frac{1}{2\pi C R_2} = 10kHz$

e.g. $C = 500\,pF$, $R_2 \cong 32k\Omega$

a) Peak detection: every 100ms, detect the max intensity and restart

Peak detection:

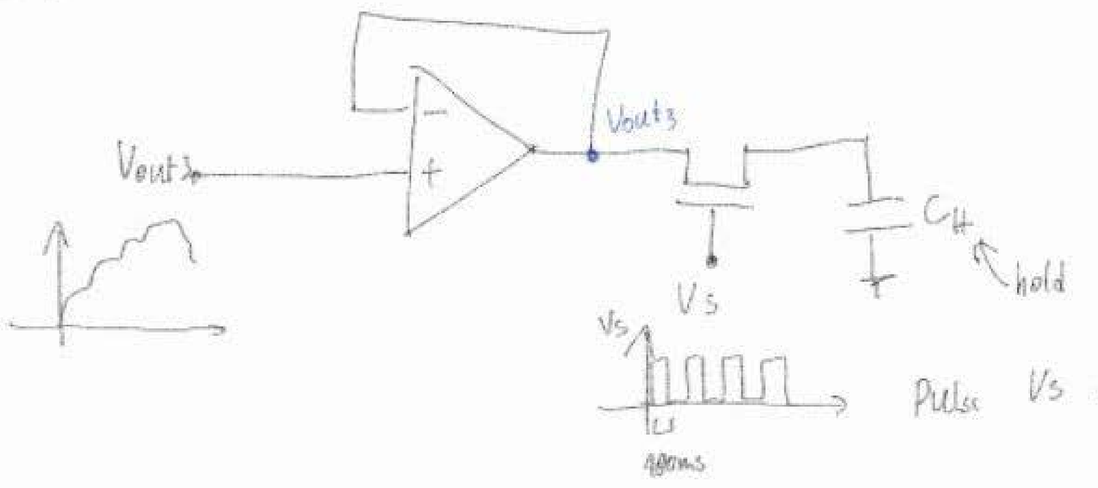




start: $V_{out_2}^0 > 0 \longrightarrow$ D2 ON $\rightarrow$ Till $(\varepsilon = \emptyset) \rightarrow V_{out_3} = V_{out_2}^0$ stored in C_{sp}

Iterate in time
- $\hookrightarrow$ If $V_{out_2}\downarrow (< V_{out_2}^0) \rightarrow V_D < 0 \Rightarrow$ D2 OFF $\longrightarrow C_{sp}$ stay still with the stored V_{out_2}
- $\hookrightarrow$ If $V_{out_2}\uparrow (> V_{out_2}^0) \rightarrow V_D > 0 \Rightarrow$ D2 ON $\rightarrow C_{sp}$ store new value

Sample: (S&H)



Pulse V_S with freq. $f_{pulse} = \frac{1}{2 \cdot 100ms} = 5\,Hz$

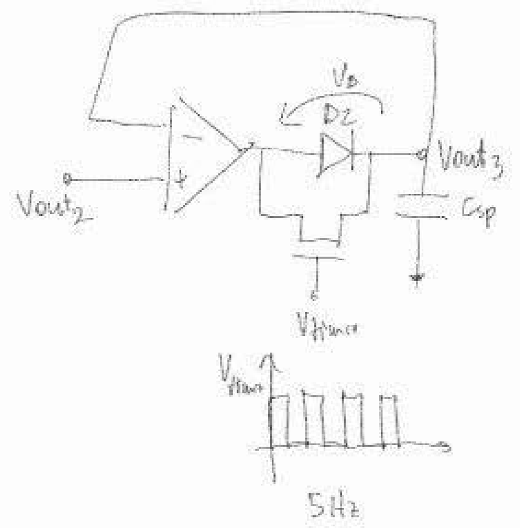
Restart (peak + S&H)

$\rightarrow V_{out_2}\uparrow \; (V_{out_2}(t) > V_{out_2}(t-1)) \rightarrow V_{out_3}(t) = V_{out_2}(t)$

$\rightarrow V_{out_2}\downarrow \; (V_{out_2}(t) < V_{out_2}(t-1)) \rightarrow V_{out_3}(t) = V_{out_3}(t-1)$

When $\bullet\, V_S = 1 \longrightarrow V_{out_3}$

$\bullet\, V_S = 0 \longrightarrow V_{out_3} = 0$

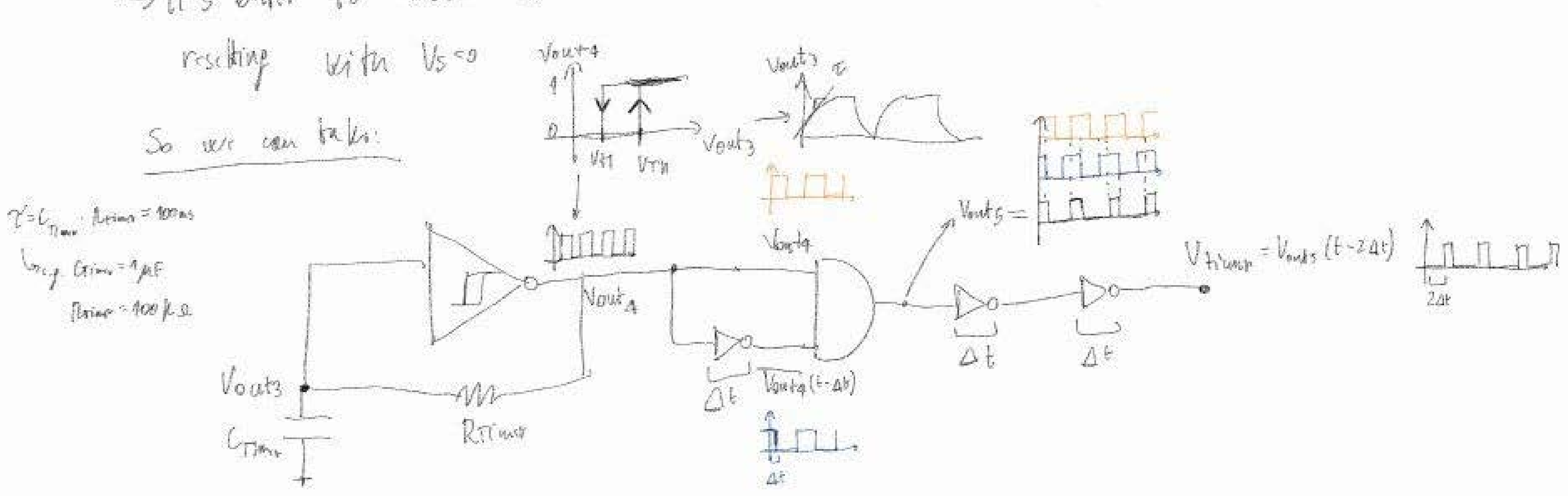


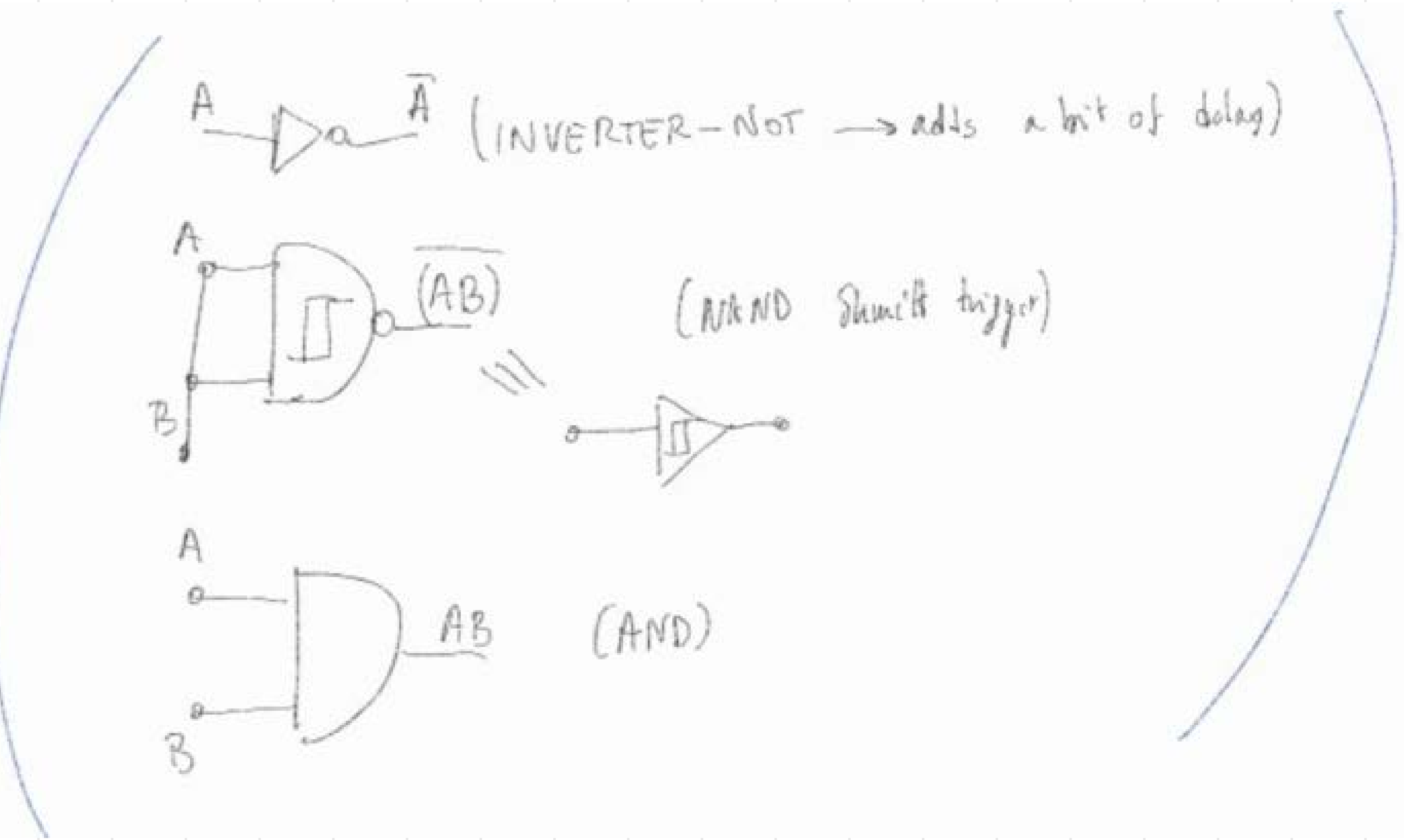
$\hookrightarrow$ It's better to wait a little bit to allow the C_{sp} capacitor to discharge before resetting with $V_S = 0$

So we can have:

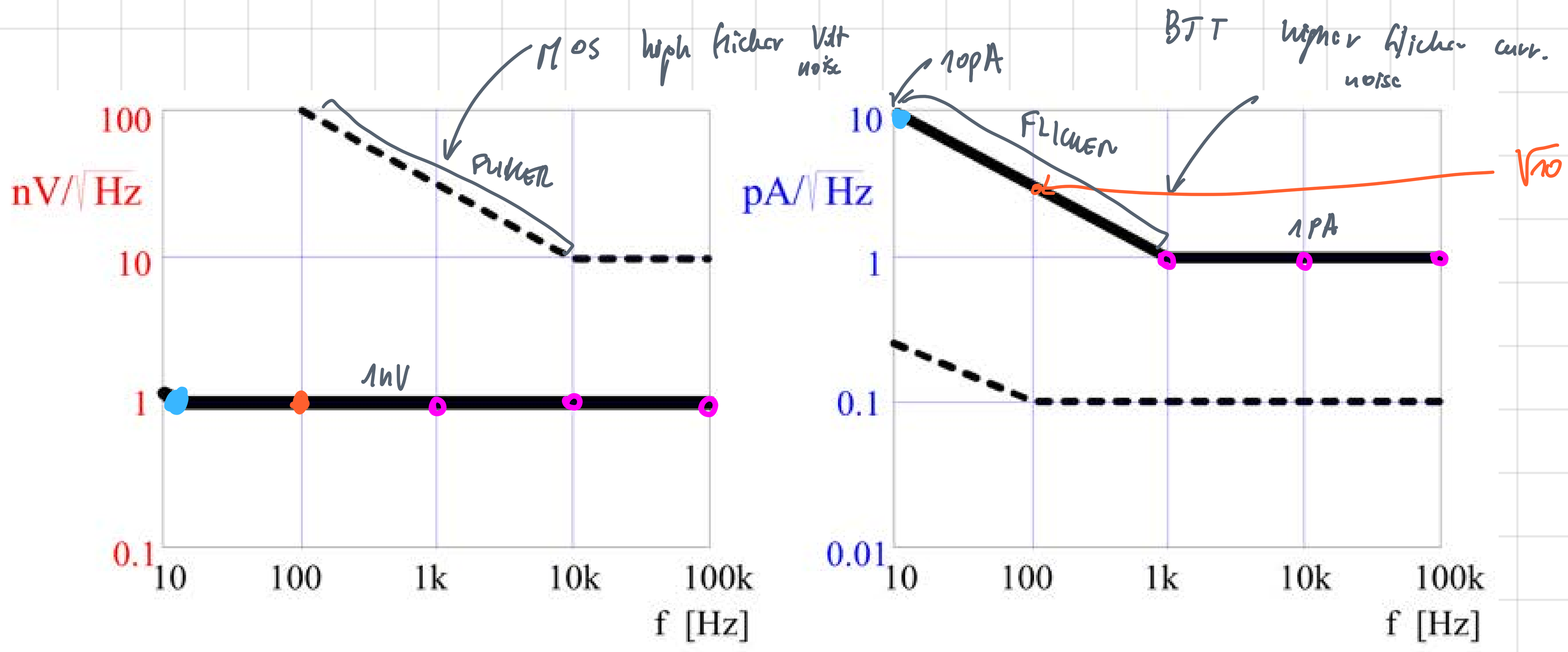
$\tau = C_{Timer} \cdot R_{Timer} = 100ms$

e.g. $C_{Timer} = 1\mu F$, $R_{Timer} = 100k\Omega$





(1)

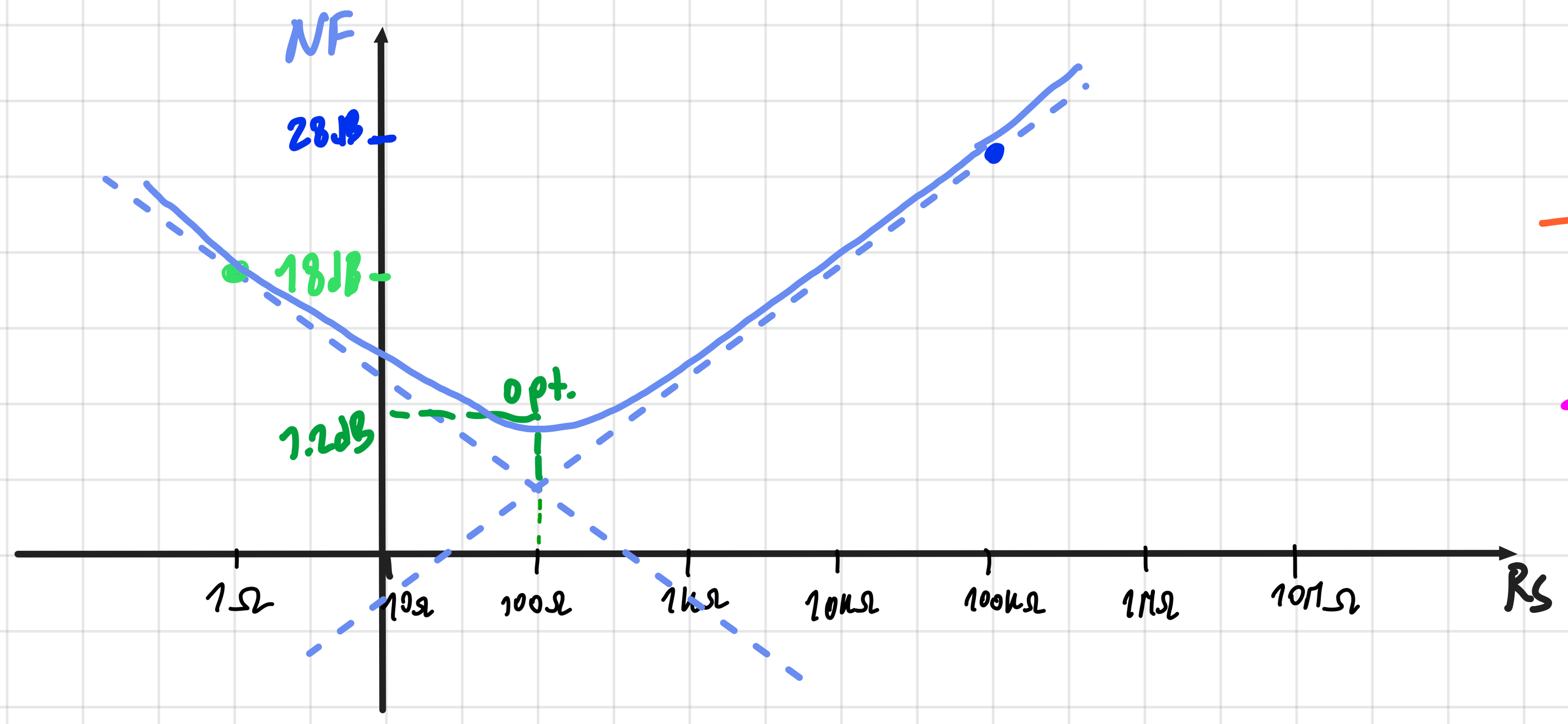


MOS (dashed lines) and BJT (solid lines) transistors at $I_C=I_D=1mA$

a) Draw the NF plots vs. R_S=10Ω÷10MΩ, at 10, 100, 1k, 10k and 100kHz

b) Select the lowest noise transistor for R_S=10kΩ

a) NF for BJT:



$$\rightarrow R_{Sopt} = \sqrt{\frac{v_{in,eq}^2/\Delta f}{i_{in,eq}^2/\Delta f}} = \sqrt{\frac{v_{in,eq}^2}{i_{in,eq}^2}} = \frac{1nV}{10p} = 100\,\Omega$$

$$\rightarrow R_{Sopt} = \frac{1nV}{3.2pA} = 316\,\Omega$$

$$\rightarrow R_{Sopt} = \frac{1nV}{1pA} = 1k\,\Omega$$

$$\hookrightarrow NF_{opt} = 10\log_{10}\left(1 + 2\,\frac{v_{in}\cdot i_{in}}{4kT}\right)\frac{10^{-21}}{1.66\cdot 10^{-20}} = 1.2\,dB$$

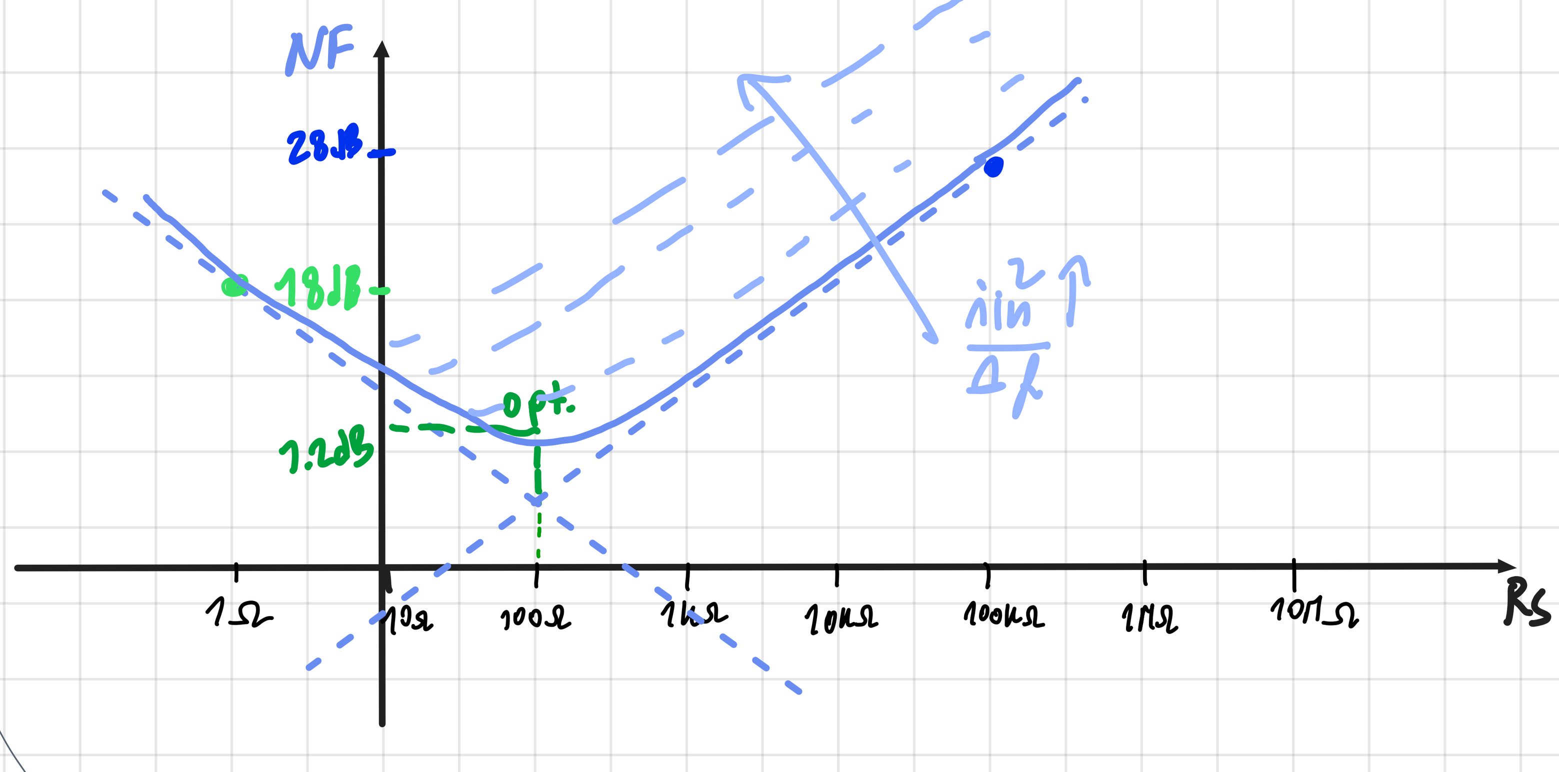
- $4KT = 1.66\cdot 10^{-20}$ ....

→ We compute $NF_{R_S high}$ and $NF_{R_S low}$ in order to understand the slopes
(like 100kΩ, 1MΩ..)

$$\hookrightarrow \bullet\ NF_{100k\Omega} = 10\log_{10}\left(1 + \underbrace{\left(\frac{1n}{4on}\right)^2}_{negligible} + \left(\frac{10p\cdot 100k}{4on}\right)^2\right) \simeq 28\,dB$$

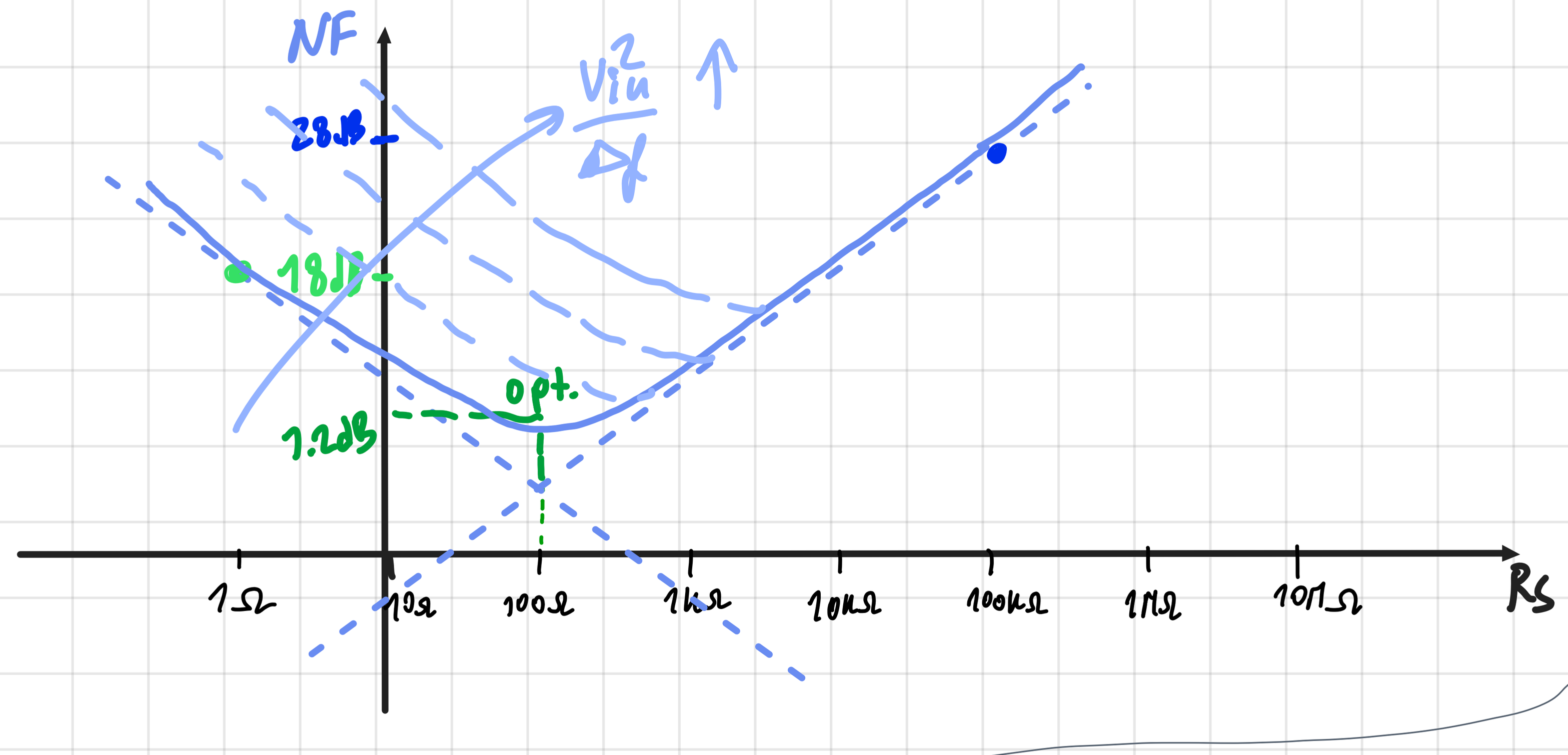
$$\hookrightarrow \bullet\ NF_{1\Omega} = 10\log_{10}\left(\underbrace{1}_{negligible} + \left(\frac{1n}{0.12}\right)^2 + \underbrace{\left(\frac{10p\cdot 1\Omega}{0.12}\right)^2}_{negligible}\right) \simeq 18\,dB$$

Note: If we increase $\frac{i_{in}^2}{\Delta f}$ this is the NF:



$\hookrightarrow R_{S_{opt}} \downarrow$

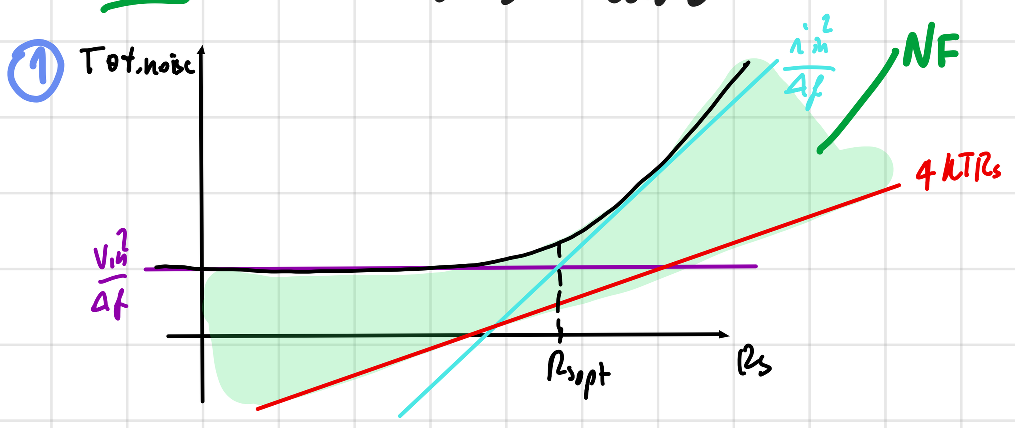
If we increase $\frac{v_{in}^2}{\Delta f}$ this is the NF:



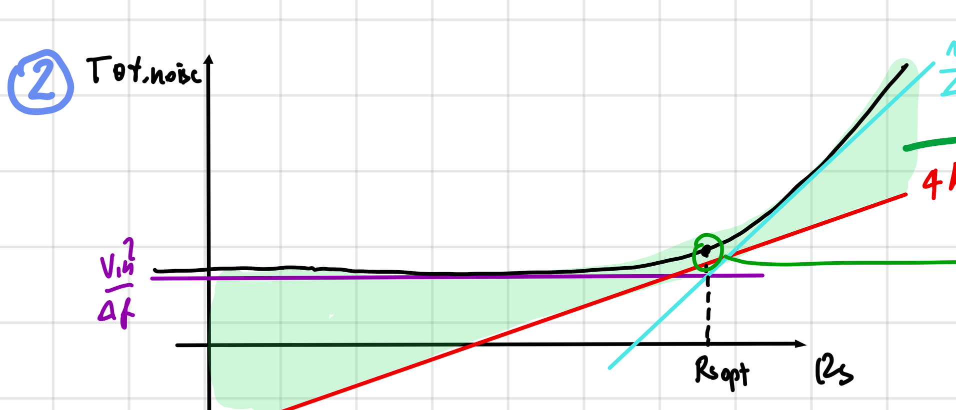
$\hookrightarrow R_{S_{opt}} \uparrow$

Obs. Total noise cases

(1)



(2)

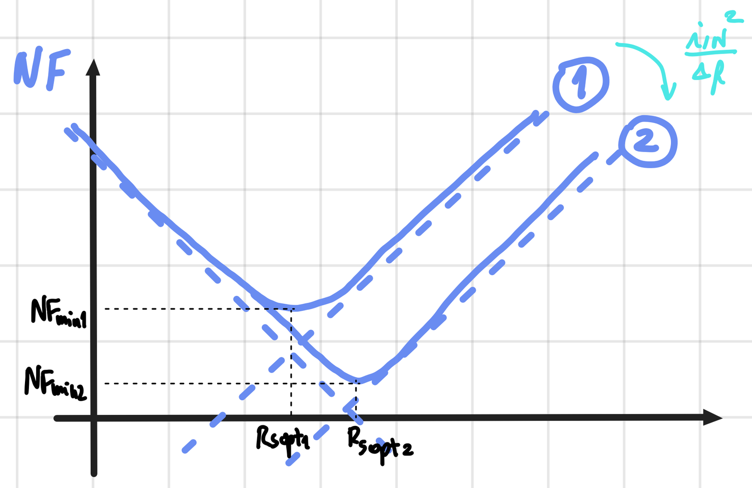


(so for $\frac{i_{in}^2}{\Delta f}\downarrow$ $R_{Sopt}\uparrow$)

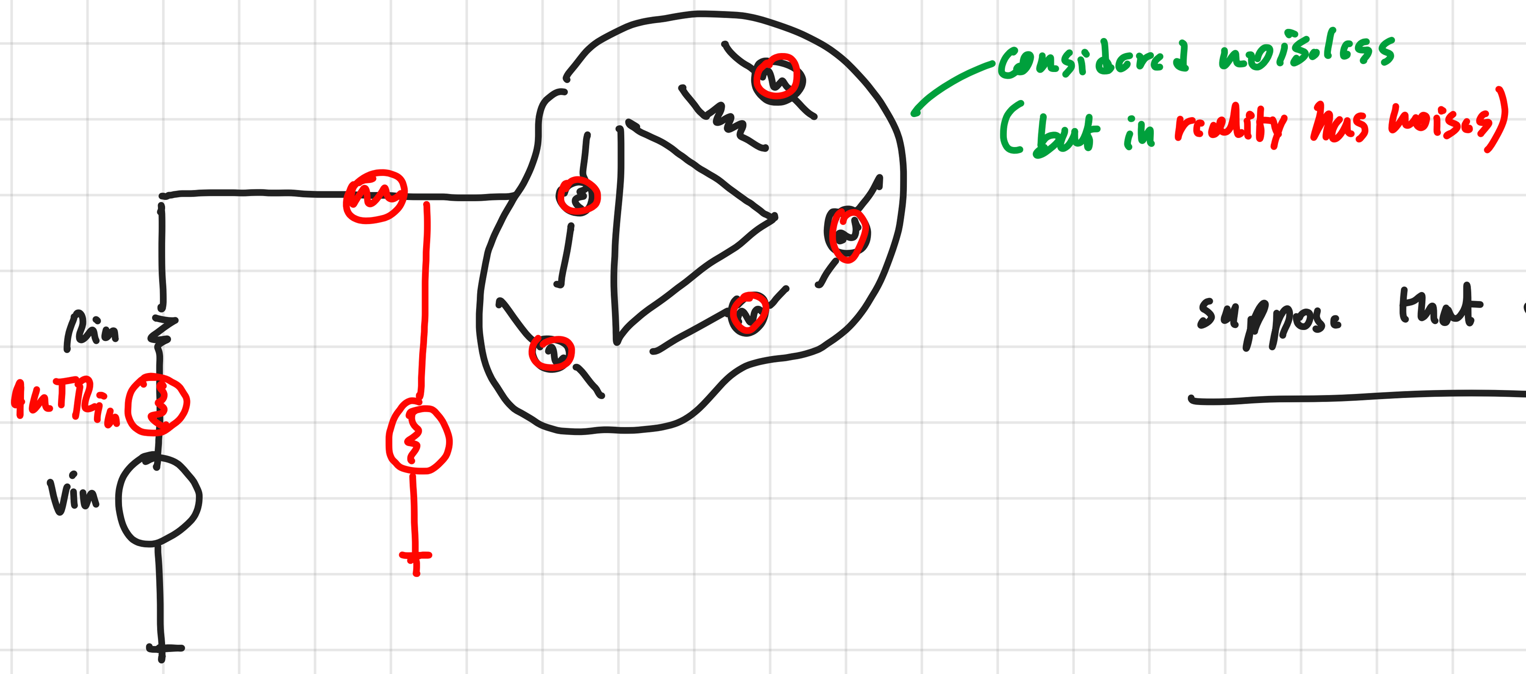
very low $\frac{i_{in}^2}{\Delta f}$

NF lower

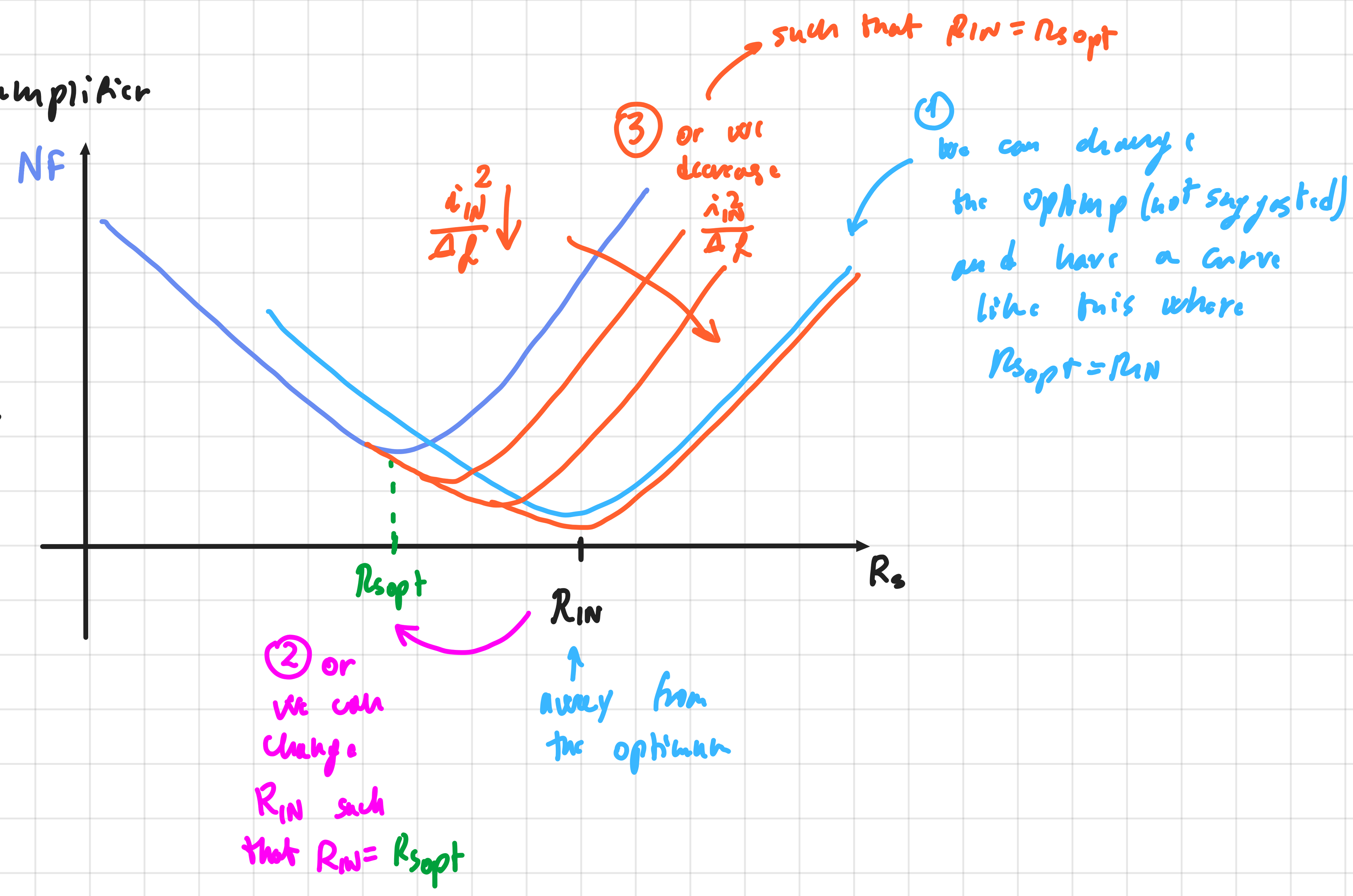
→ the min NF is much lower than the previous case. Thus, we have decreased $\frac{i_{in}^2}{\Delta f}$ in order for the total noise to "touch" the thermal error 4kTRs



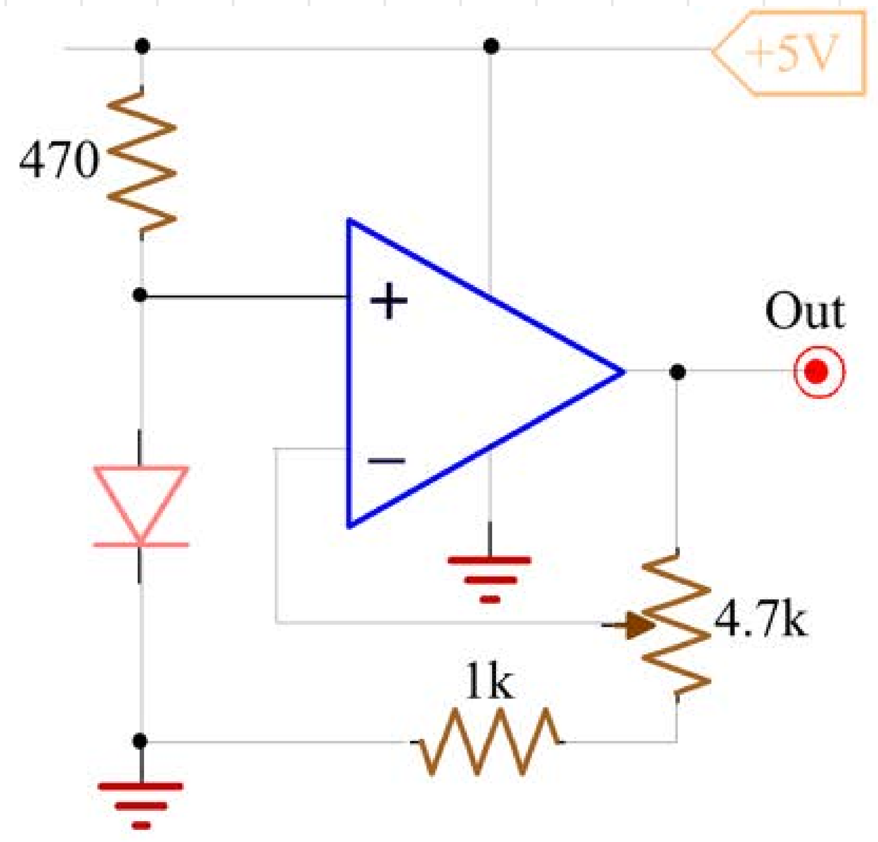
Note: Suppose we have a circuit connected to an amplifier

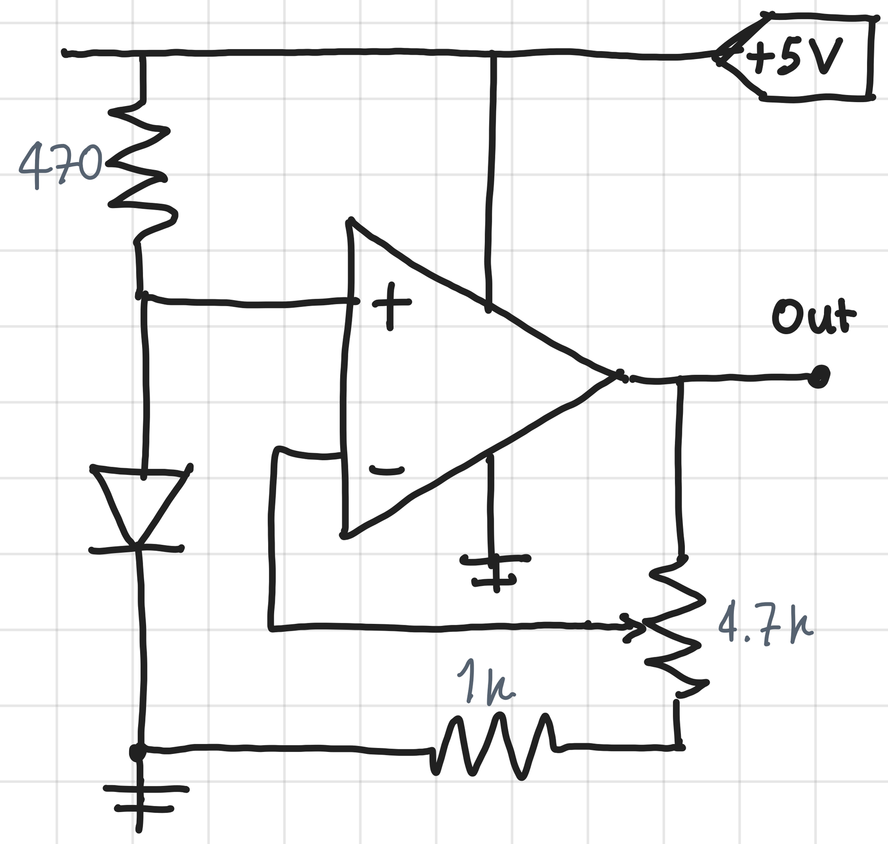


Suppose that the NF



②



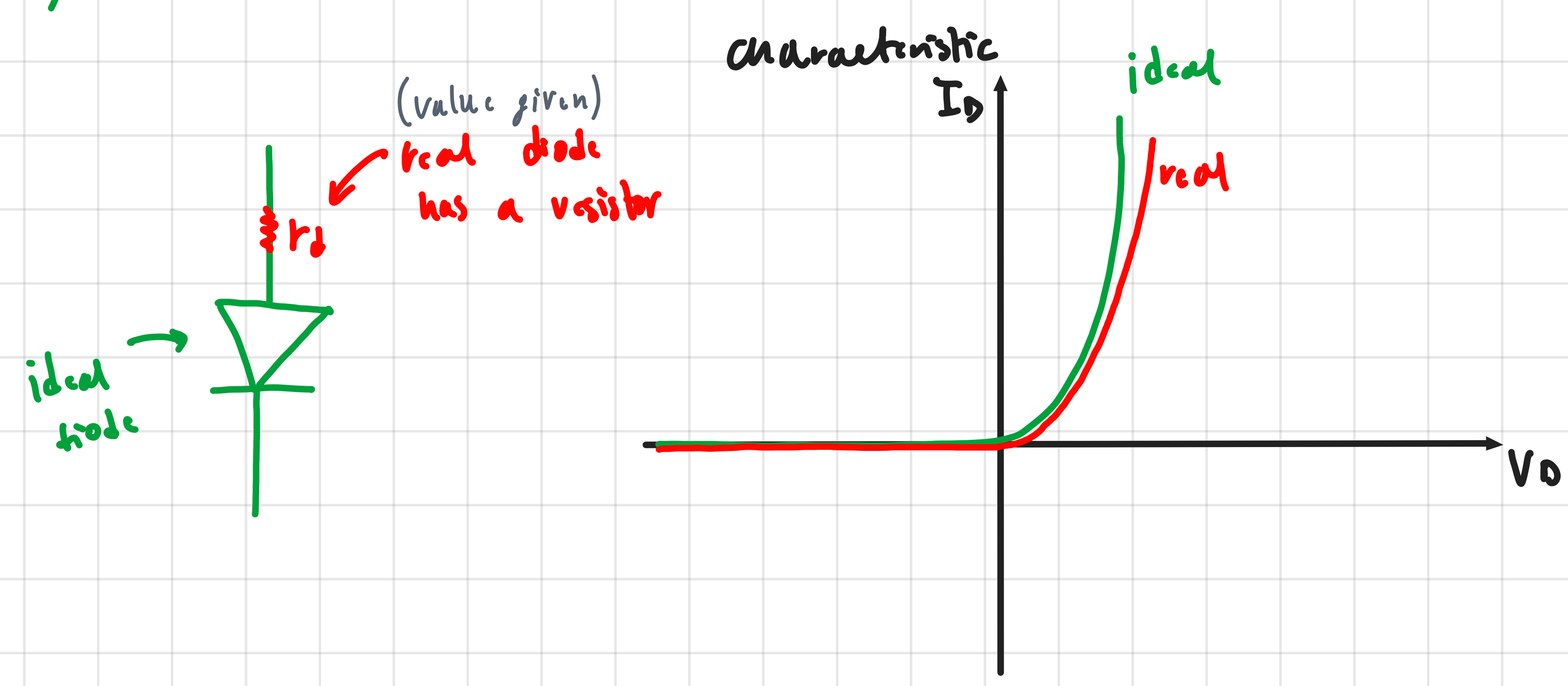


OpAmp: A_0=100dB, GBWP=10MHz, ~~4nV/√Hz and 5pA/√Hz noise~~

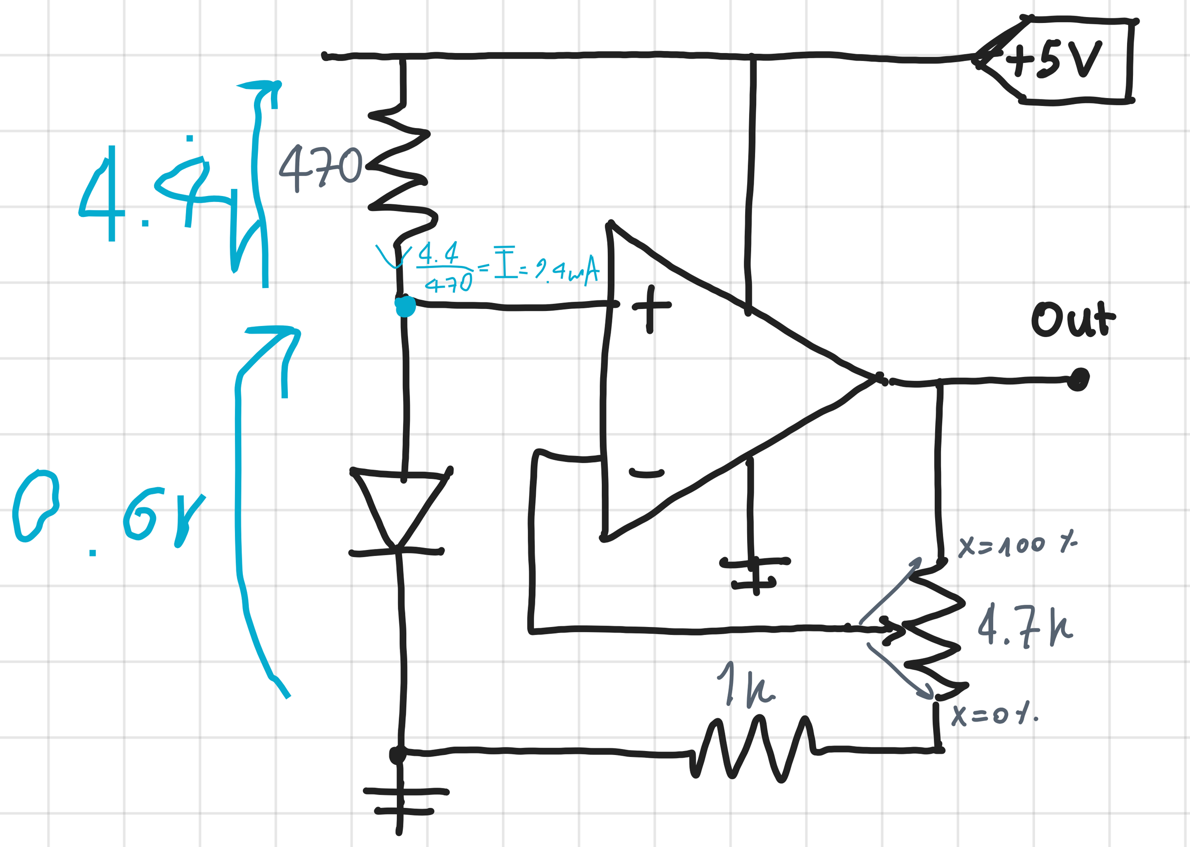
a) Compute output rms noise, with trimmer's cursor at the two ends

b) Discuss the role of the 1kΩ resistor

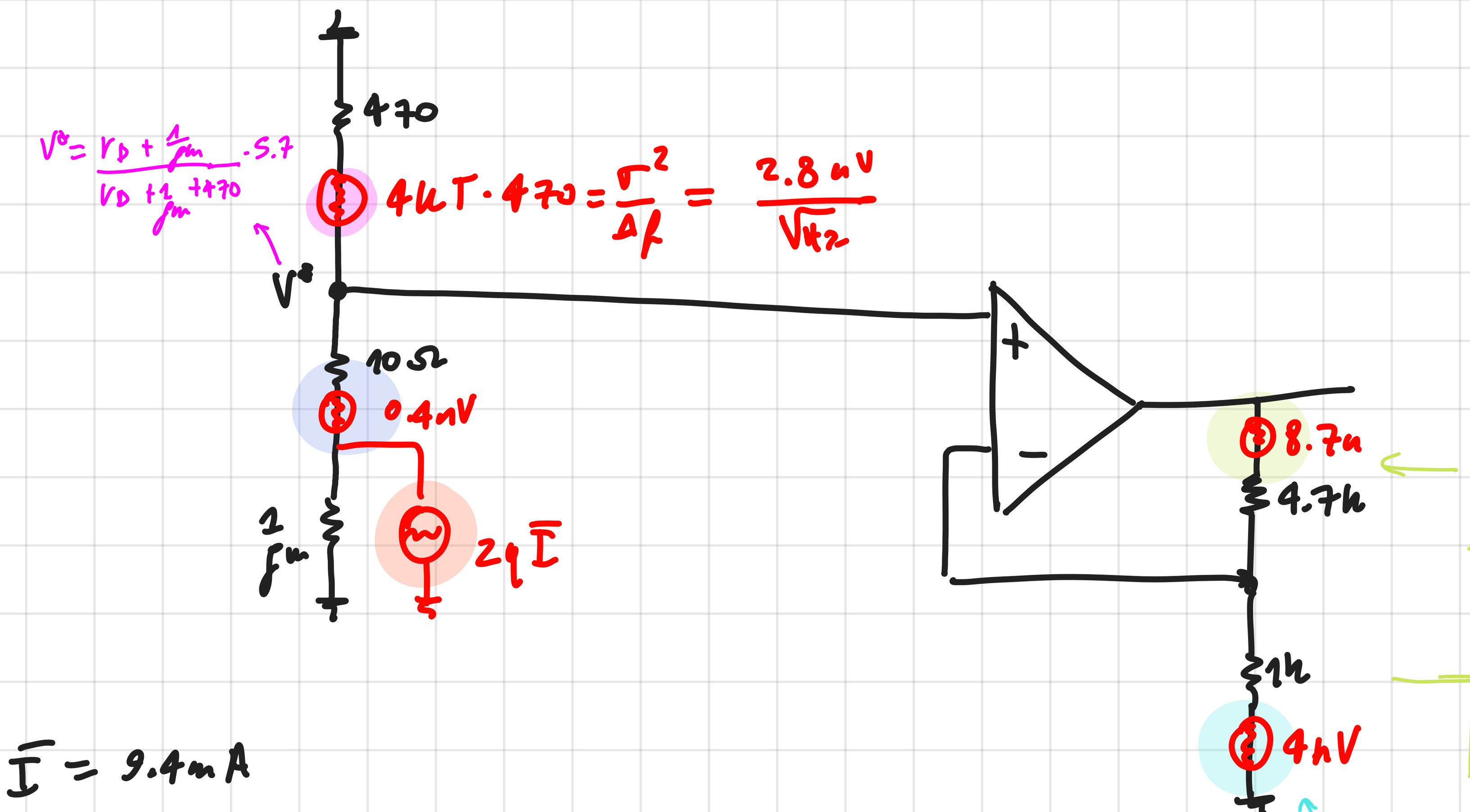
a) Remember:

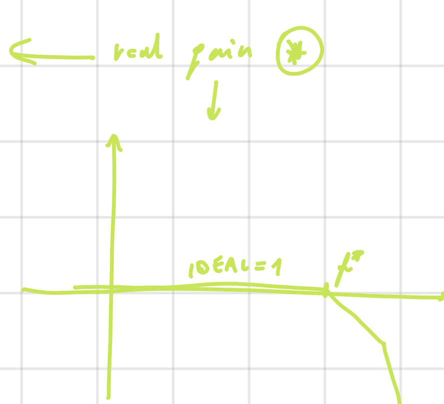


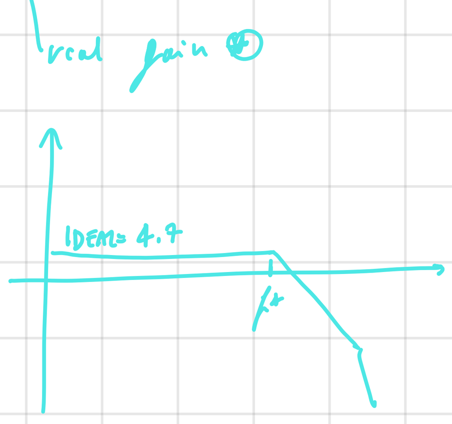
Consider the all circuit:



• x = 0%





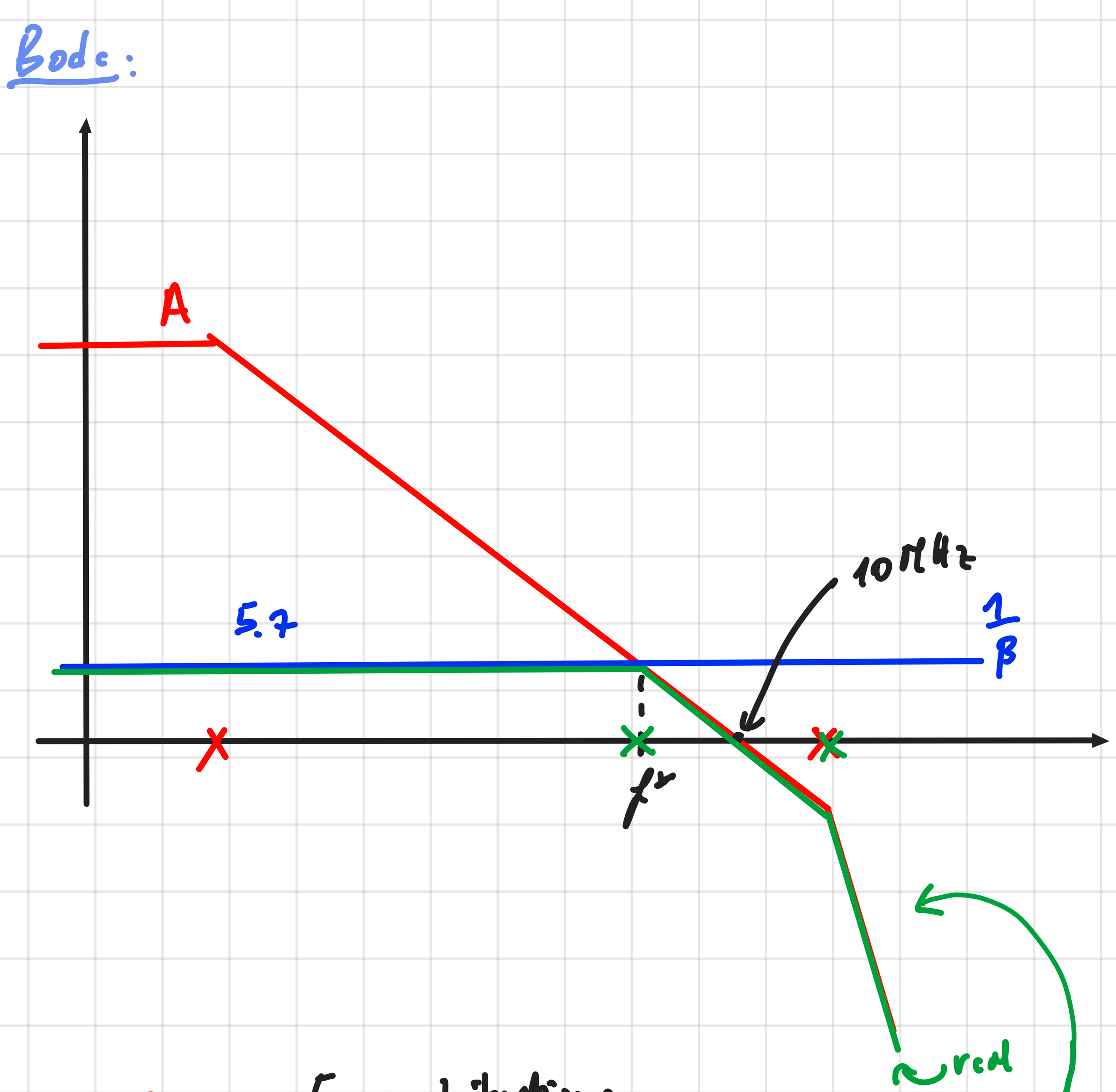


$\hookrightarrow \; I = 9.4mA$

$\frac{1}{g_m} = \frac{V_{th}}{I} = \frac{25mV}{9.4mA} = 2.7\Omega$

$2qI = \frac{i_n^2}{\Delta f} = \left(55\frac{pA}{\sqrt{Hz}}\right)^2$

Bode:



we consider just 1 (dominant) pole for the real gain

$\hookrightarrow f_{bw_{1pole}} = \frac{\pi}{2} f^*$

Noise analysis: 5 contributions

$$V^2_{out_{noise\,rms}} = \overline{V_{out}^2} = \underbrace{\left(\frac{2.8nV}{\sqrt{Hz}}\cdot\frac{r_D+\frac{1}{g_m}}{r_D+\frac{1}{g_m}+470}\cdot 5.7\right)^2 f_{bw}}_{725\mu V_{rms}} + \underbrace{\left(0.9nV\cdot\frac{470}{470+r_D+\frac{1}{g_m}}\cdot 5.7\right)^2\cdot\frac{\pi}{2}\cdot 1.8MHz}_{3.8\mu V_{rms}} + \underbrace{\left(55p\cdot\frac{\frac{1}{g_m}}{\frac{1}{g_m}+r_D+470}\cdot 470\cdot 5.7\right)^2\cdot\frac{\pi}{2}\cdot 1.8MHz}_{1.4\mu V_{rms}} +$$

$$+ \underbrace{\left(8.7n\cdot 1\right)^2\frac{\pi}{2}\,1.8MHz}_{14.6\mu V_{rms}} + \underbrace{\left(4n\cdot\frac{4.7k}{1k}\right)^2\frac{\pi}{2}\,1.3MHz}_{31.6\mu V_{rms}} \cong 726\mu V = 0.7\,mV_{rms}$$

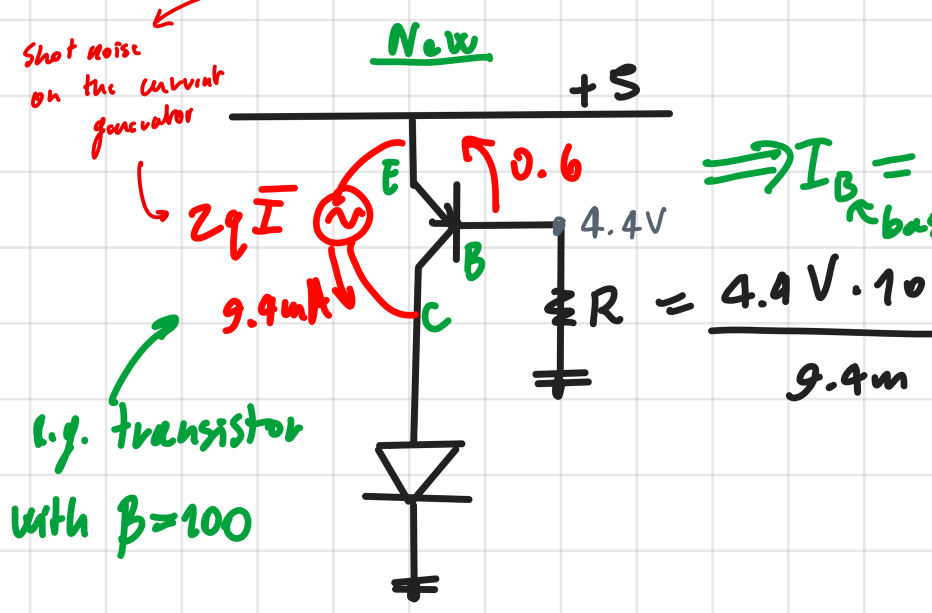
↳ So when $X = 0\%$ Gain = 5.7 $\sigma_{rms} = 0.7\ mV_{rms}$

Obs. If the circuit has a too high noise we can change the circuit like this:

must be computed on the new circuit

sufficiently smaller wrt the thermal noise of the original circuit

New

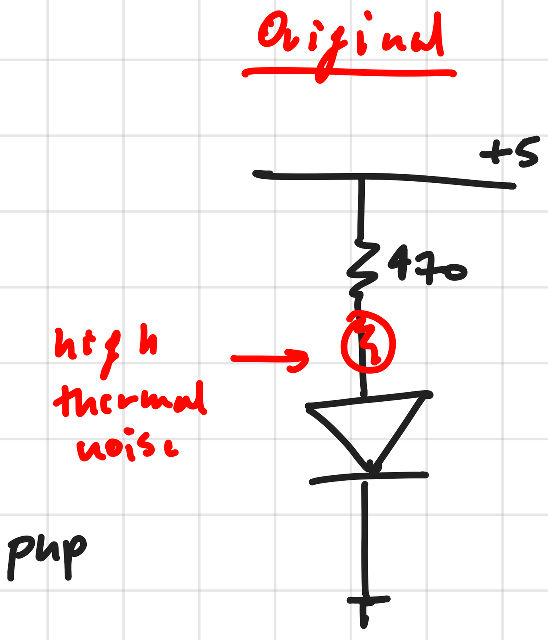


$$\Rightarrow I_{B_{base}} = \frac{9.4\ mA}{100}$$

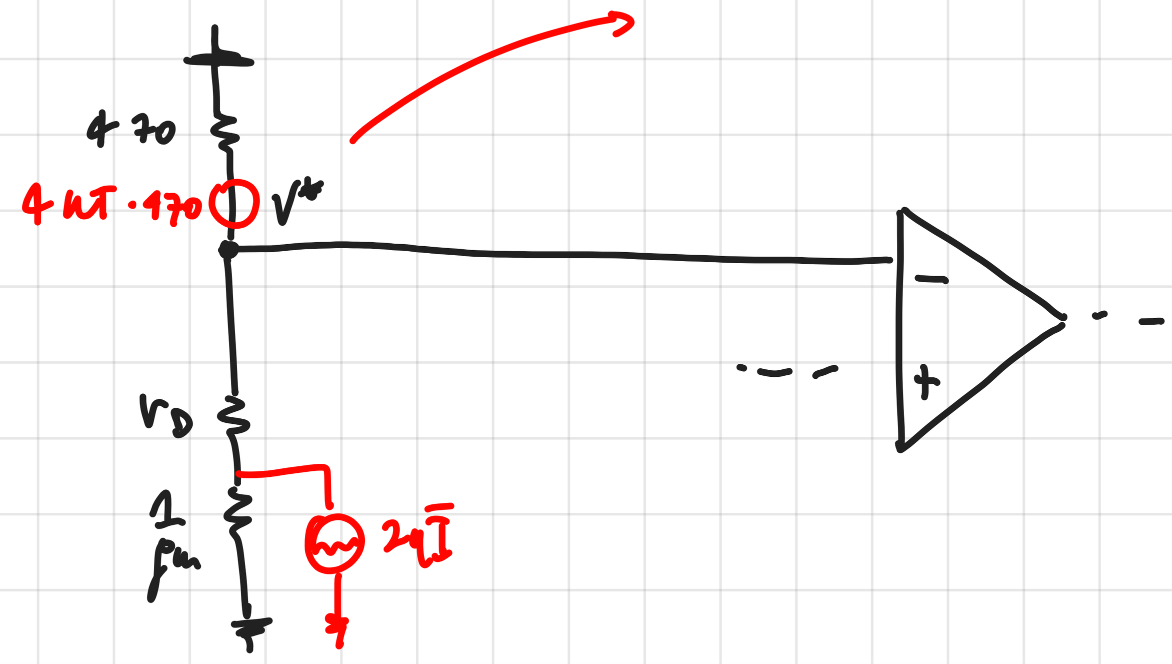
$$R = \frac{4.4\ V \cdot 100}{9.4m} \approx 47k\Omega$$

← Instead of using the resistor (too high thermal noise) we can use a transistor pnp

Original



Obs. To reduce the noise, what should we do?



1st contribution: $V^+ = 4kT \cdot \underbrace{470}_{R} \left(\frac{\overbrace{r_D + \frac{1}{g_m}}^{12.7}}{\underbrace{r_D + \frac{1}{g_m}}_{12.7} + \underbrace{470}_{R}} \right)^2$ ← BAD CONTRIBUTION (high value wrt the other ones)

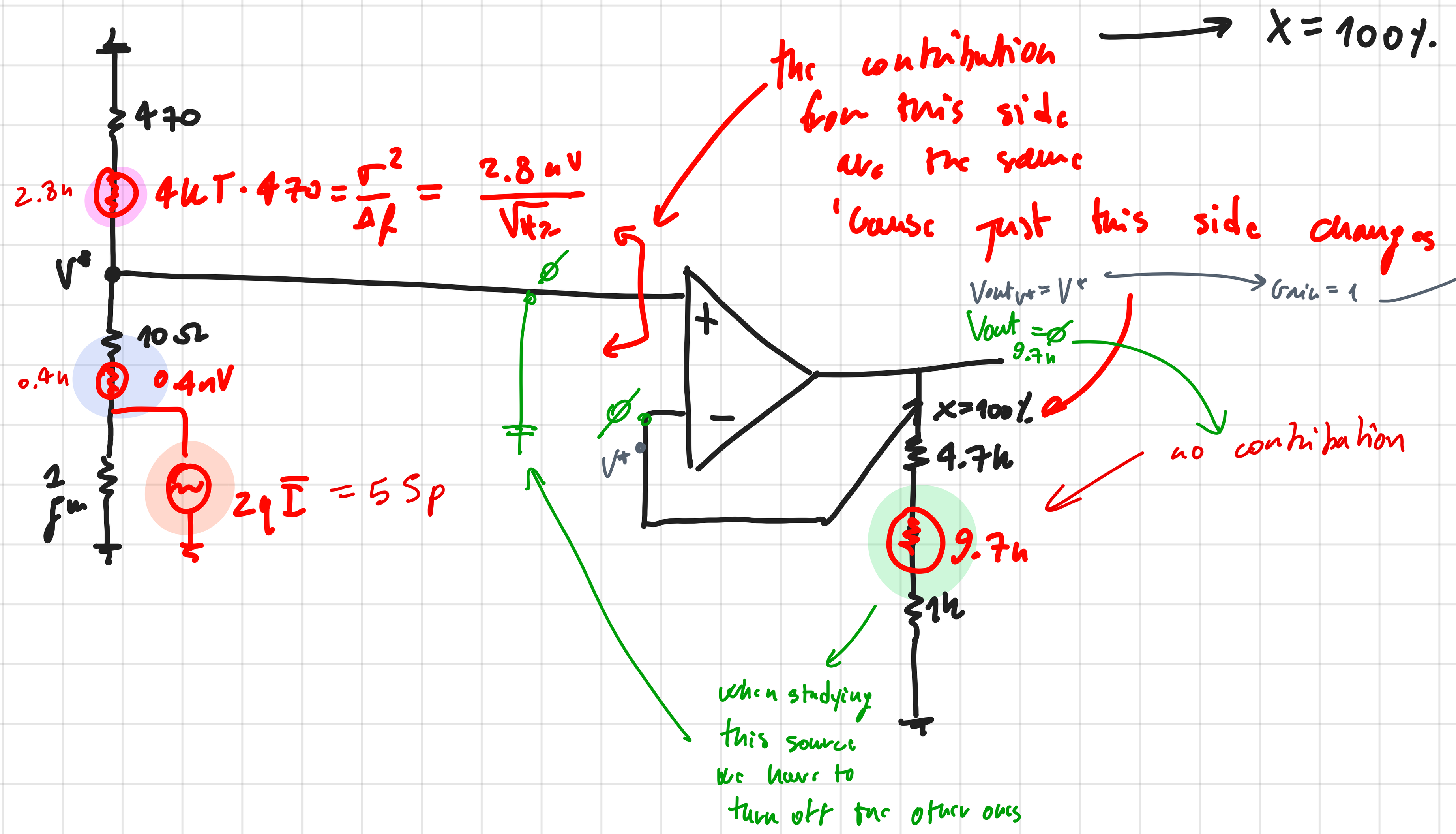
we want to reduce it

↳ Should I reduce or increase R? → $V^+ = 4kTR \cdot \left(\frac{12.7}{12.7 + R} \right)^2$

↳ If we increase a lot R such that $R >> 12.7$ $V^+ \propto \frac{1}{R}$

↳ So for $R \uparrow$ $V^+ \downarrow$ (reduce the noise) becomes negligible

- $X = 100\%$

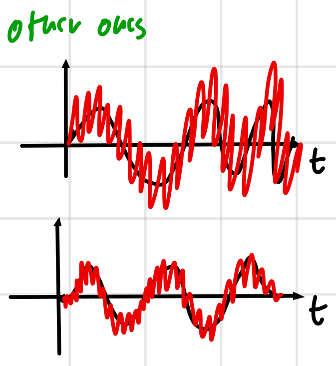


→ $X = 100\%$ Gain = 1 $\sigma_{rms} = 0.05\ mV_{rms}$

final σ_{rms}

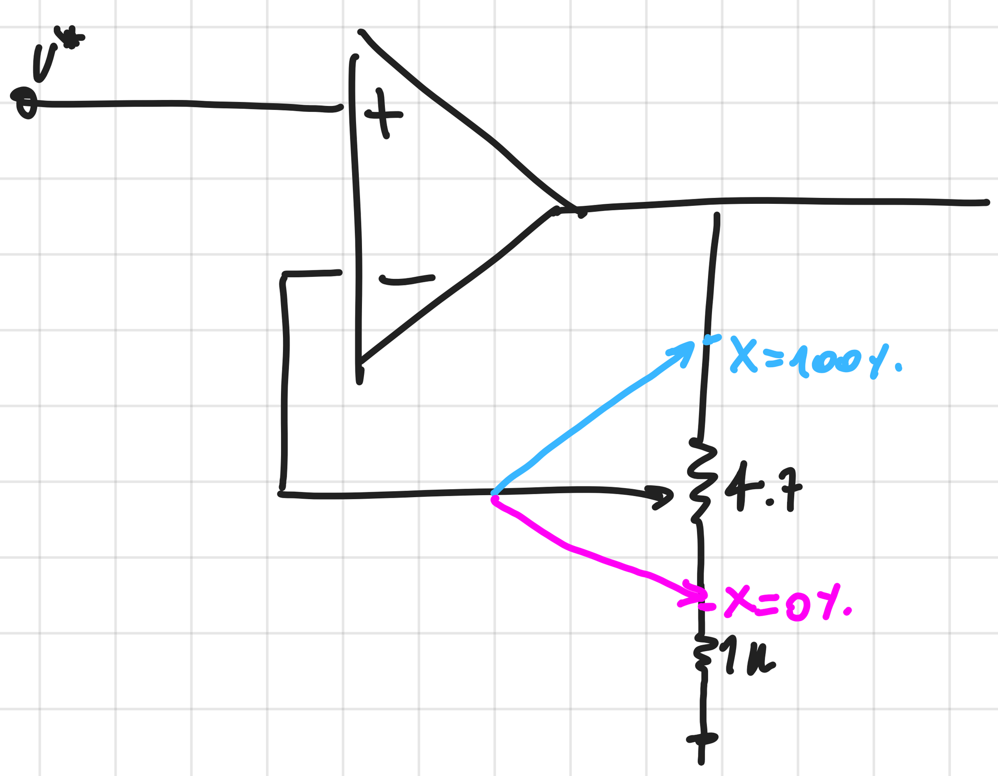
Obs. $X = 0\%$ Gain = 5.7 $\sigma_{rms} = 0.7\ V_{rms}$

$X = 100\%$ Gain = 1 $\sigma_{rms} = 0.05\ V_{rms}$



concerning noise the best config. is $X = 100\%$, but we should also compare them computing the SNR

b)

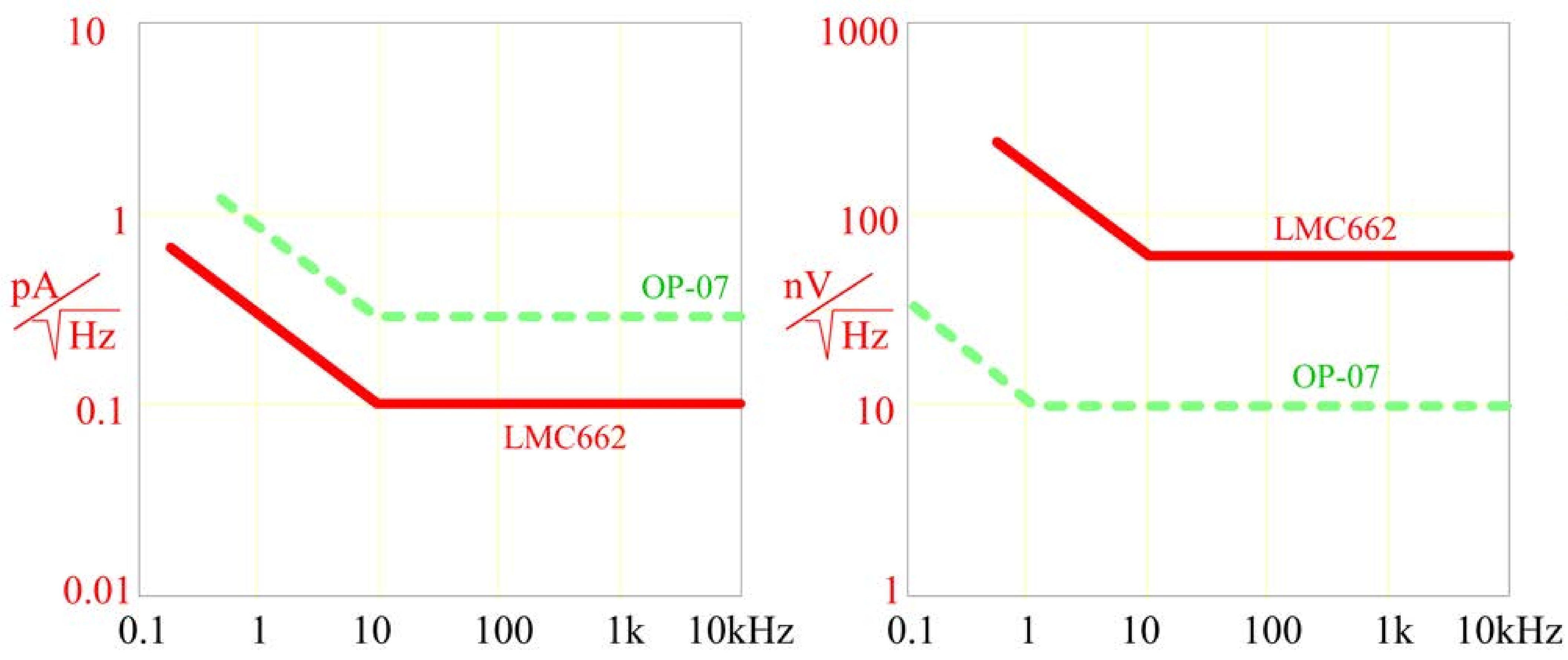


- $G = 1 + \frac{R_F}{R_1} = 1 + \frac{4.7k}{1k} = 5.7$

- $G = 1 + \frac{R_F}{R_1} = 1 + \frac{4.7k}{\emptyset} = \infty$

role of 1k depending on $X = 0\% / 100\%$

③



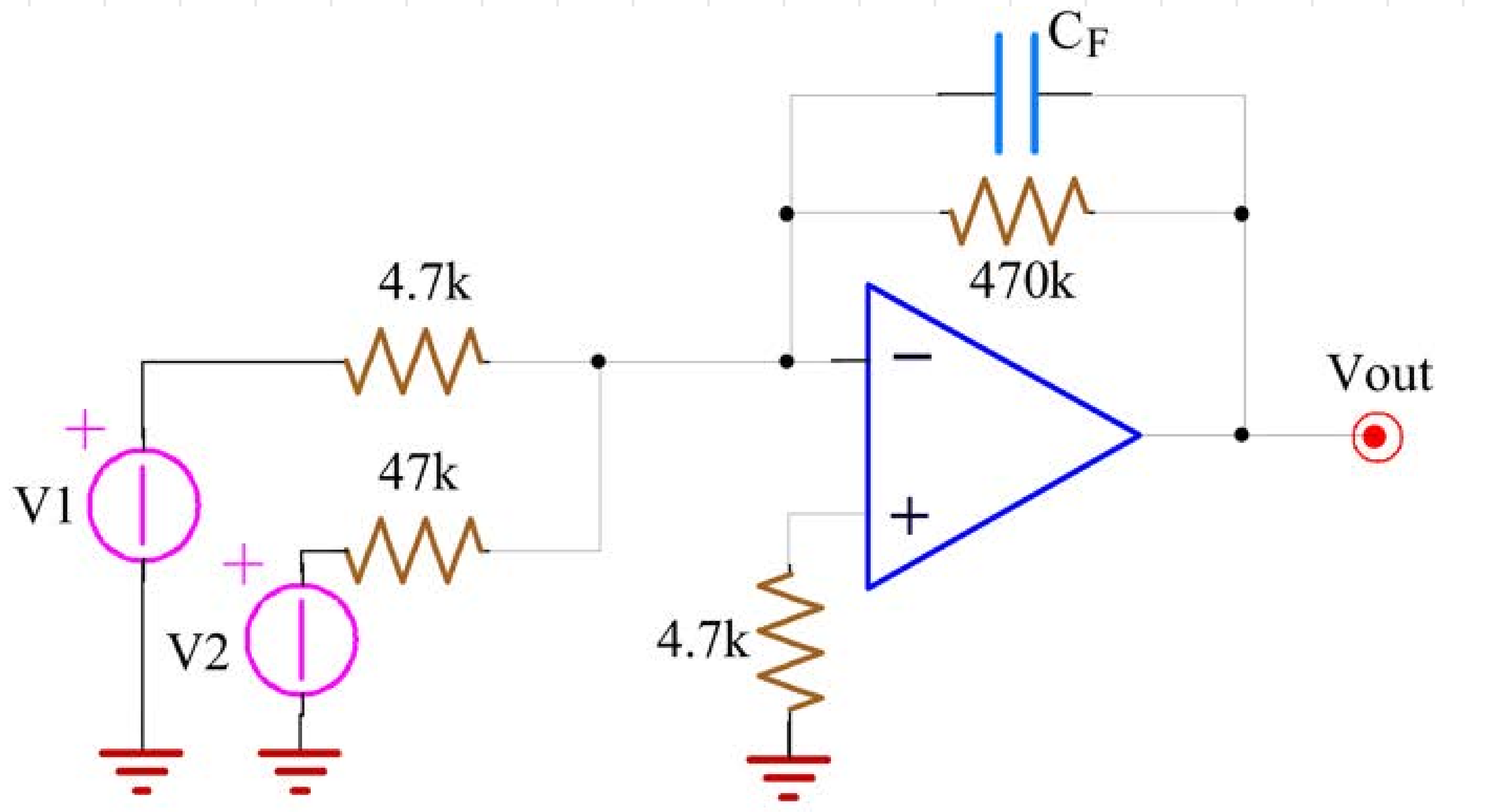
Given these two OpAmps

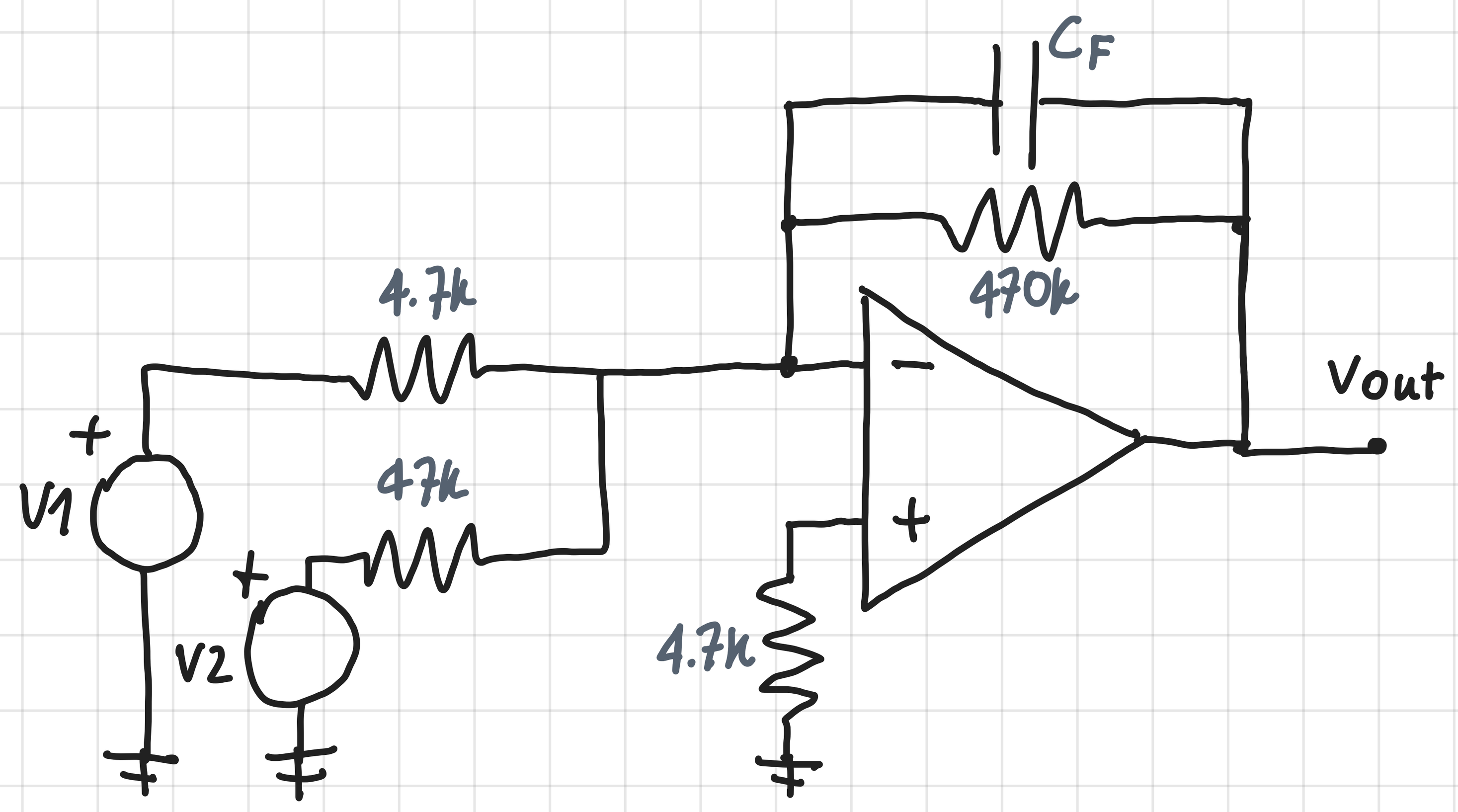
a) Draw the *NF* plots vs. R_S in the $1k\Omega$ - $1G\Omega$ range

b) Select the best OpAmp for $R_S = 1M\Omega$ at *1Hz* and at *1kHz*

(Skipped)

4





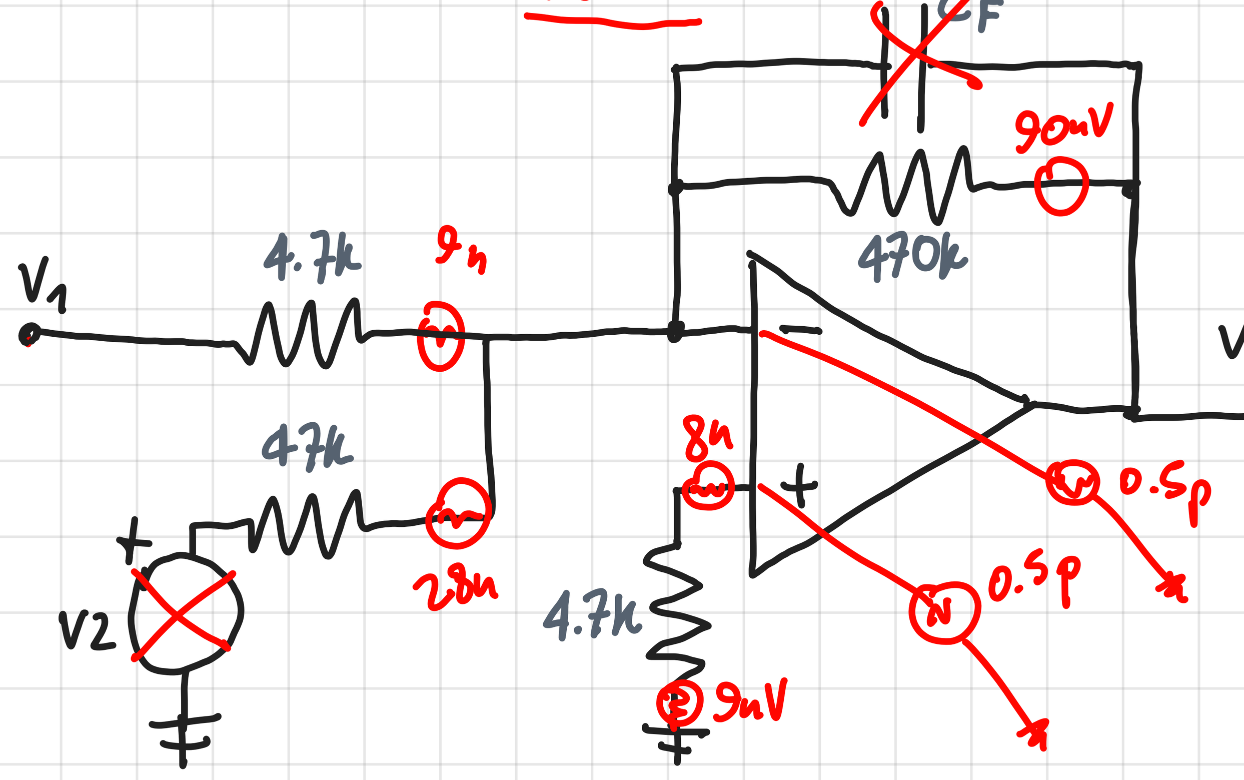
OpAmp with $v^2_{in}/\Delta f=(8nV/\sqrt{Hz})^2$ and $i^2_{in}/\Delta f=(0.5pA/\sqrt{Hz})^2$

a) Compute the noise equivalents for input V1

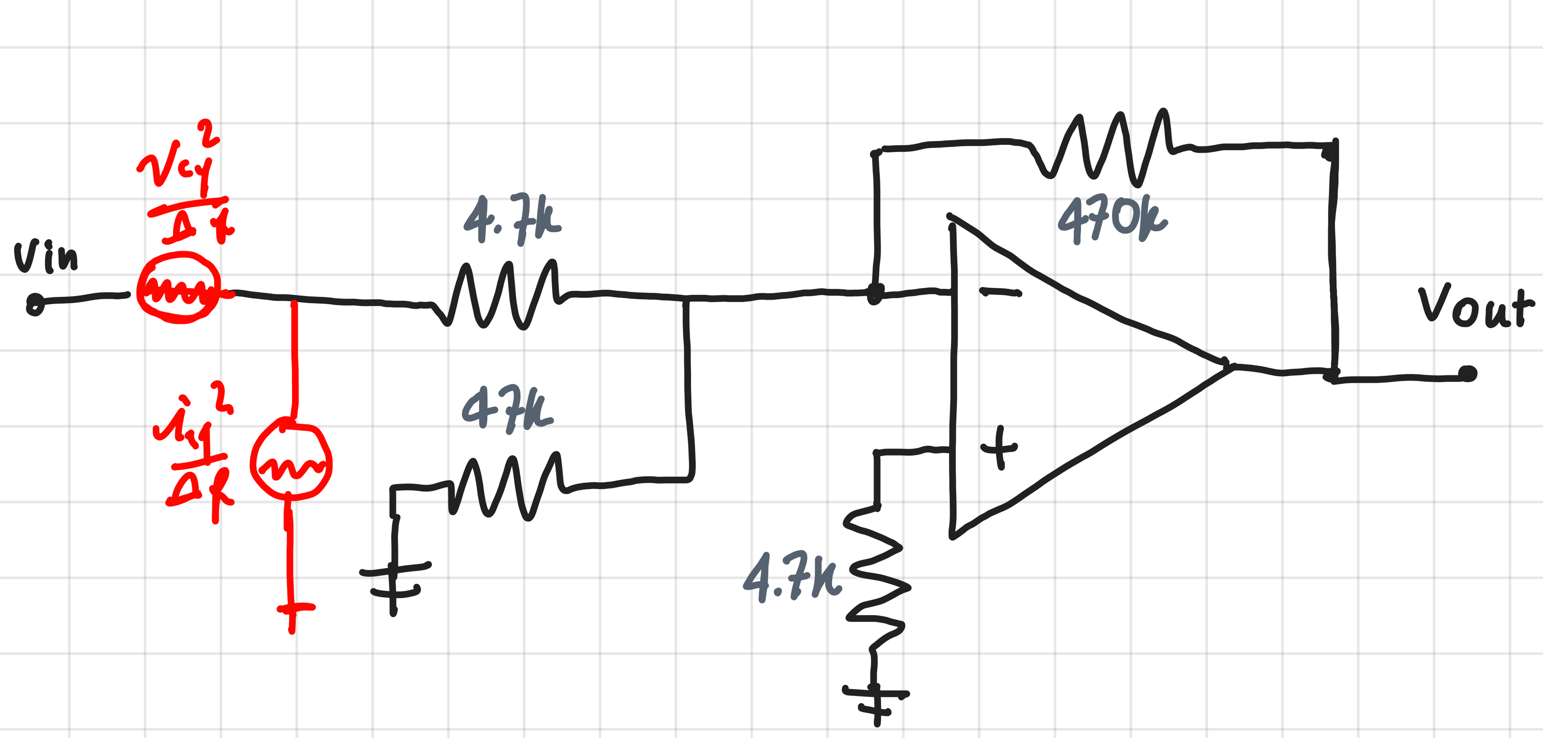
b) Compute the output rms noise

a)

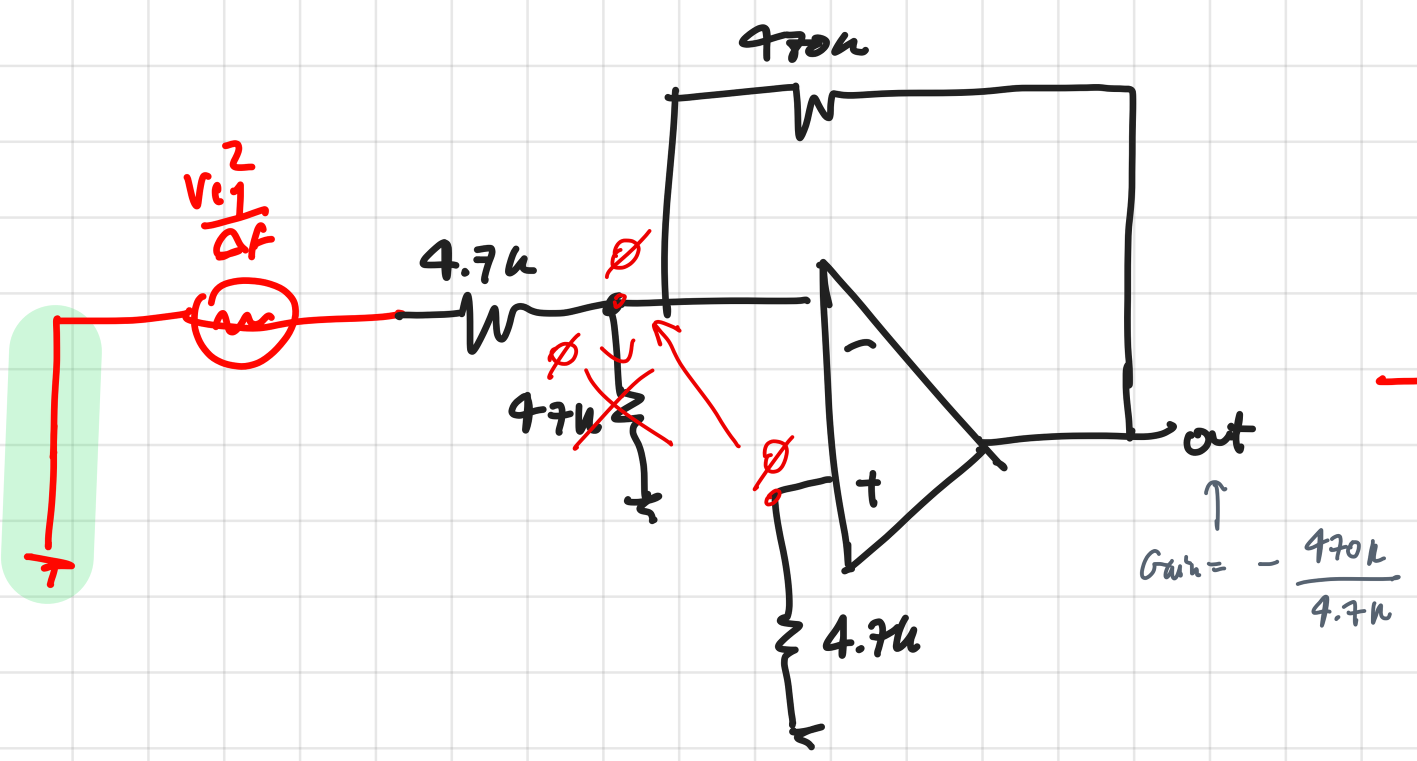
Real



Ideal



1 • Compute the noise equivalent VOLTAGE generator $\frac{V_{eq}^2}{\Delta f}$ → to do so we shortcircuit ($R_{in}=0$) the input
⇓
(no current generator $\frac{i_{eq}^2}{\Delta f}$)



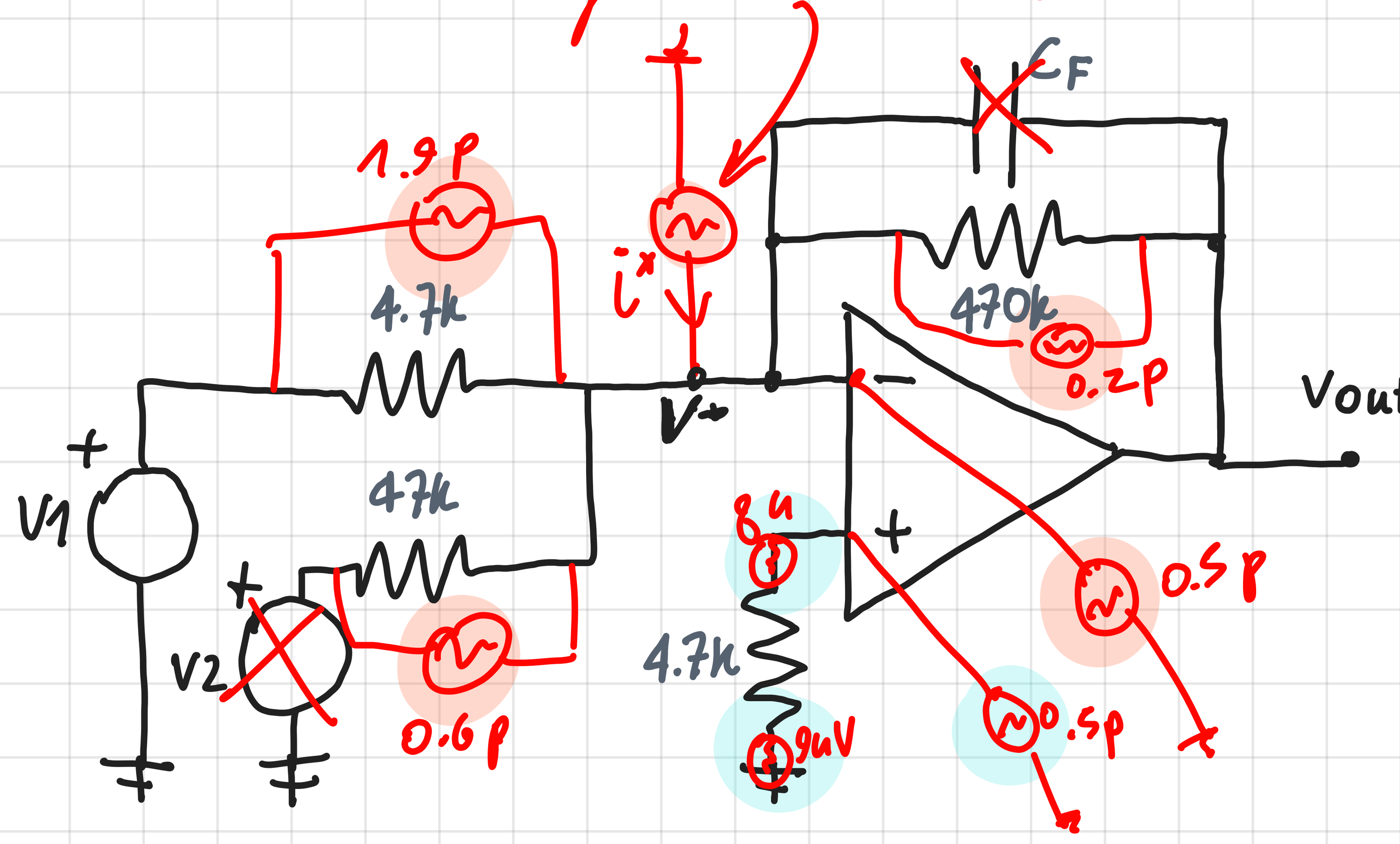
Output voltage eq. spectral density:

$$\sigma_{out}^2 = \left(\frac{V_{eq}^2}{\Delta f}\right)\left(-\frac{470k}{4.7k}\right)^2$$

• Let's study now the real circuit and compute the contributions of all the single sources

↳ Sometimes, instead of studying the voltage eq. generator sources, it's easier to directly study their contributions for the current equivalent generator:

consider
↳ real current generator (taking into account all the noise contributions)



• We'll study some contributions with the real curr. gen. sum:

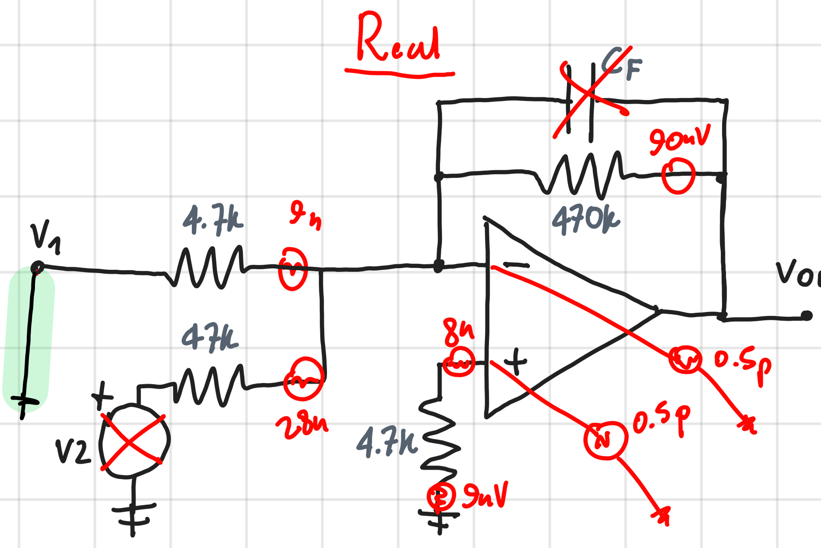
$$\frac{i^{*2}}{\Delta f} = (1.9p)^2+(0.2p)^2+(0.6p)^2+(0.5p)^2=(2.1p)^2 \simeq (2p)^2$$

↳ $$\frac{\sigma^2_{out_{i^*}}}{\Delta f} = \left(\frac{2.1p\cdot 470k}{\sqrt{Hz}}\right)^2 \simeq \left(\frac{1\mu V}{\sqrt{Hz}}\right)^2$$

• We study the rest of the contributions with a real voltage gen. sum:

$$\frac{v^{*2}}{\Delta f} = \left(\frac{9nV}{\sqrt{Hz}}\right)^2 + \left(\frac{8nV}{\sqrt{Hz}}\right)^2 + \left(\frac{0.5p\cdot 4.7k}{\sqrt{Hz}}\right)^2 = \left(\frac{12n}{\sqrt{Hz}}\right)^2$$

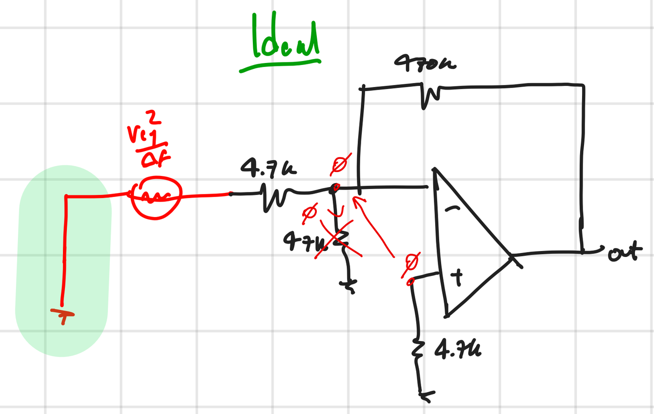
$$\hookrightarrow \frac{\sigma^2_{out}}{\Delta f}\Big|_{v^*} = (12n)^2\left(1+\frac{470k}{(47k // 4.7k)}\right)^2 \cong \left(\frac{1.3\mu V}{\sqrt{Hz}}\right)^2$$



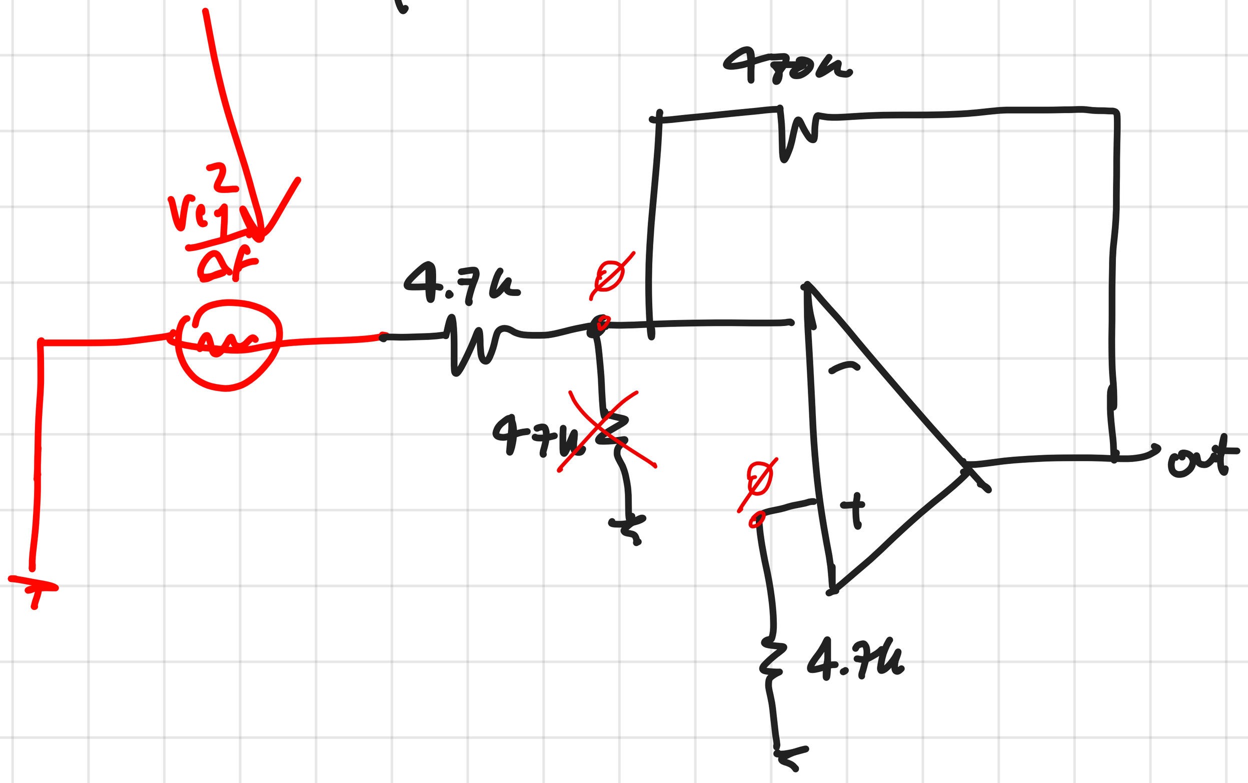
↳ We have the sum of all the contributions from the real circuit

Total noise:
$$\frac{\sigma^2_{out}}{\Delta f} = \left(\frac{1\mu V}{\sqrt{Hz}}\right)^2 + \left(\frac{1.3\mu V}{\sqrt{Hz}}\right)^2 = \left(\frac{1.6\mu V}{\sqrt{Hz}}\right)^2$$

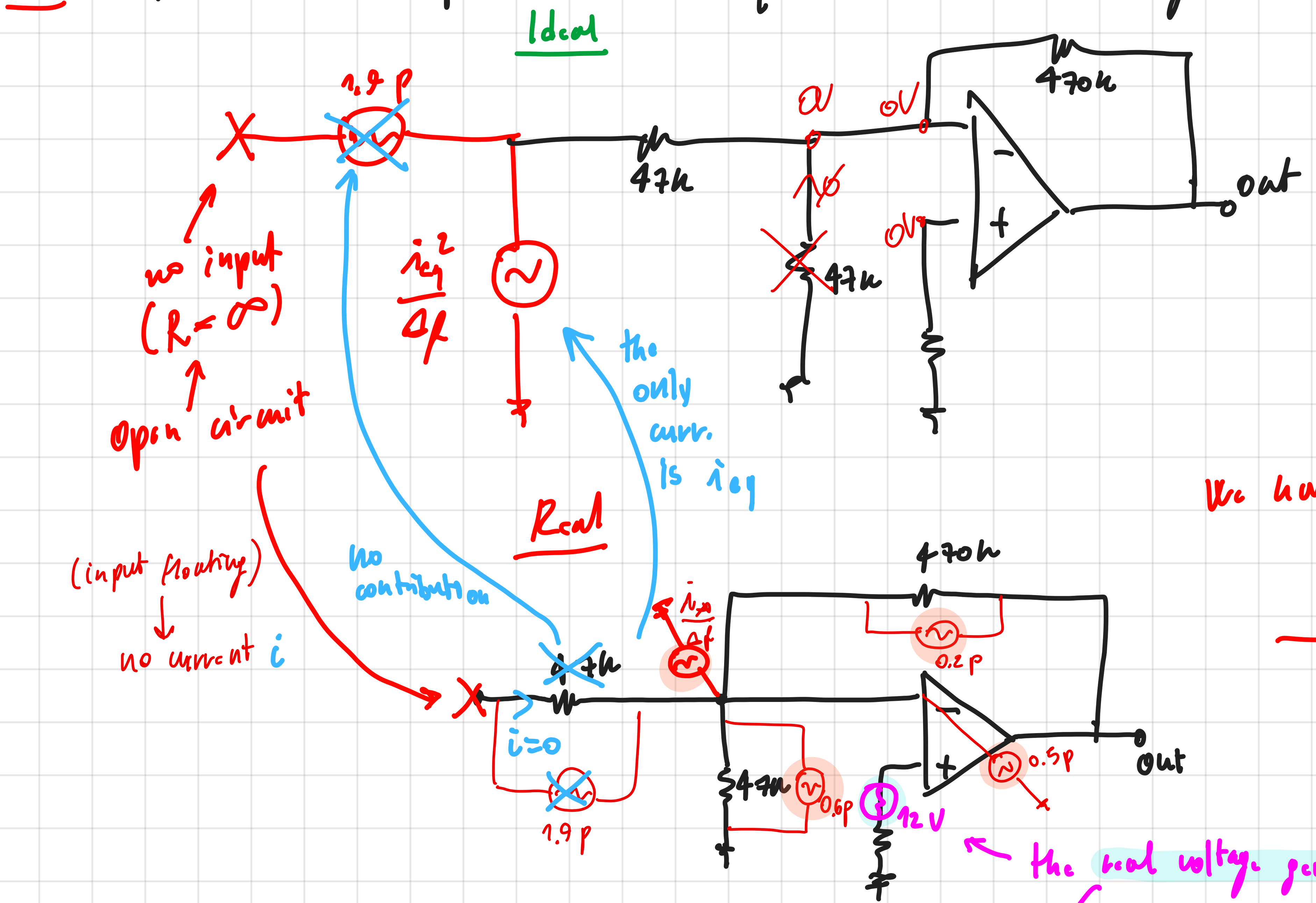
↳ We can now compute the equivalent gen. value for the ideal circuit



$$\frac{v_{eq}^2}{\Delta f}\cdot 100^2 = \left(\frac{1.6\mu V}{\sqrt{Hz}}\right)^2 \longrightarrow \frac{v_{eq}^2}{\Delta f} = \left(\frac{160 nV}{\sqrt{Hz}}\right)^2$$



2 • Now we compute the equivalent current generator



the real voltage gen. contributions are the same of before

Output current eq. spectral density:

$$\frac{\sigma^2_{out}}{\Delta f} = \frac{i_{eq}^2}{\Delta f}\cdot 470k^2$$

We have to recompute the real curr. gen. contributions (no 1.9p):

$$\frac{i_n^2}{\Delta f} = (0.2p)^2 + (0.6p)^2 + (0.5p)^2 = (0.8p)^2$$

⇒ Total noise (in voltage form):

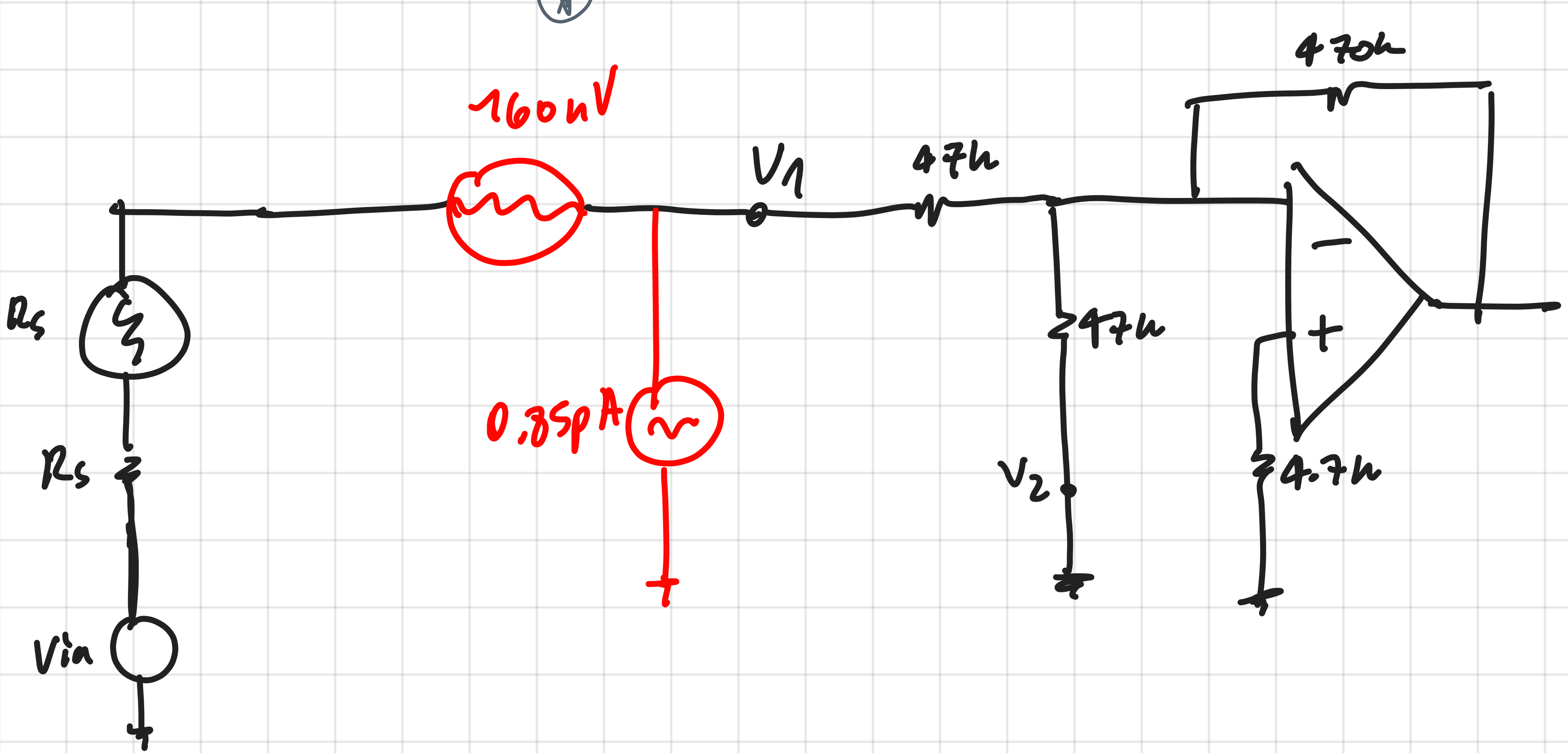
$$\frac{\sigma^2_{out}}{\Delta f} = \frac{i_n^2}{\Delta f}\cdot 470k^2 + (12n)^2\left(1+\frac{470k}{47k}\right)^2 = (\underbrace{0.8p\cdot 470k}_{376n})^2 + (132n)^2 = \left(\frac{400nV}{\sqrt{Hz}}\right)^2$$

divide for the equivalent bandwidth (*)

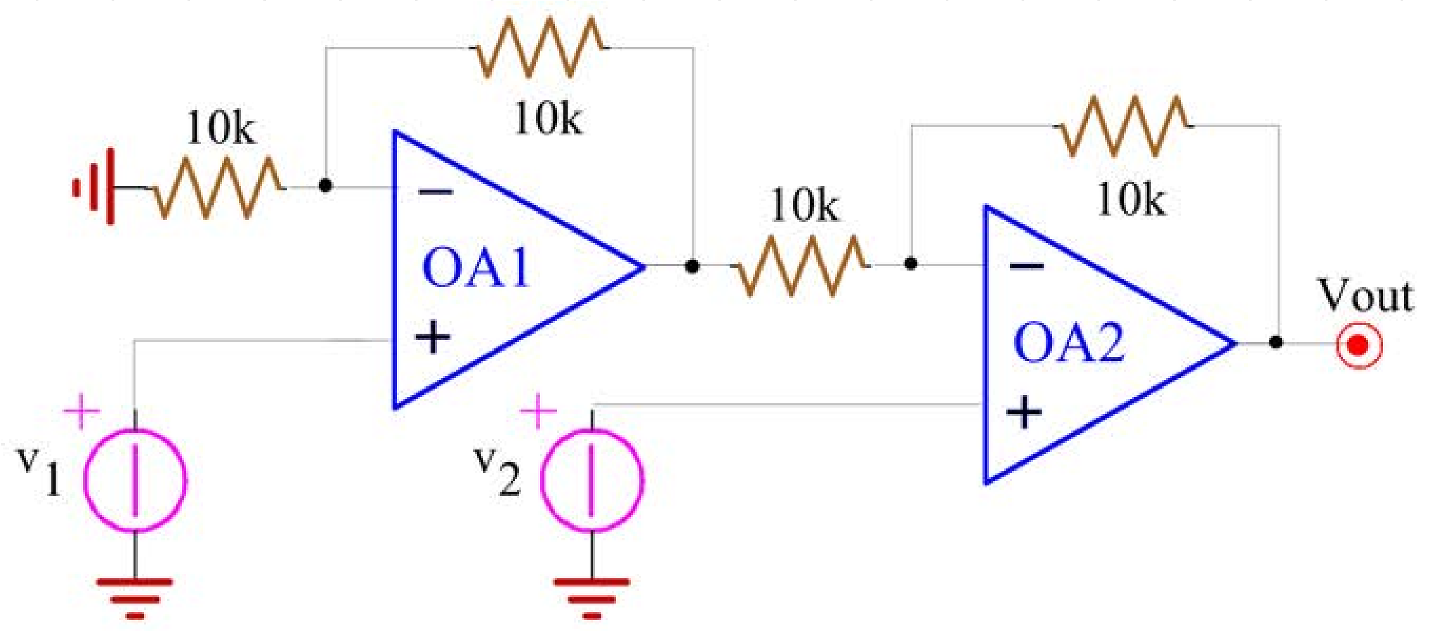
↳ The equivalent curr. noise:
$$\frac{i_{eq}^2}{\Delta f} = \left(\frac{\frac{400nV}{\sqrt{Hz}}}{470k}\right)^2 = \left(0.85\frac{pA}{\sqrt{Hz}}\right)^2$$
(*)

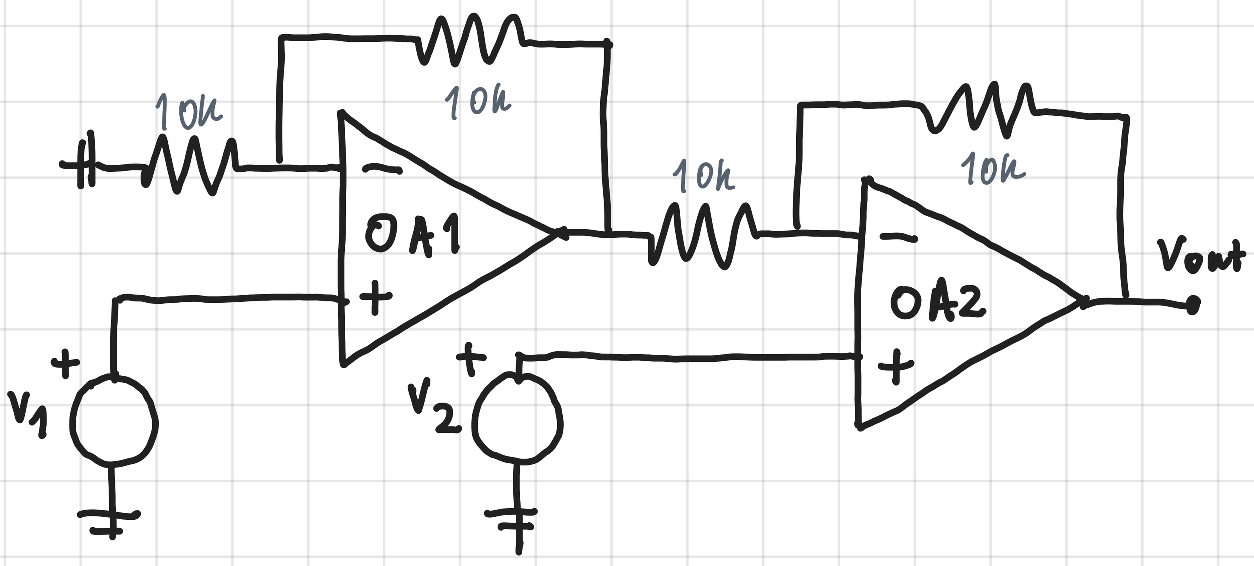
⟹ IDEAL CIRCUIT:

When we connect something we can compare the source noise 4kTRs with the rest of the noise with NF, SNR ....



(5)





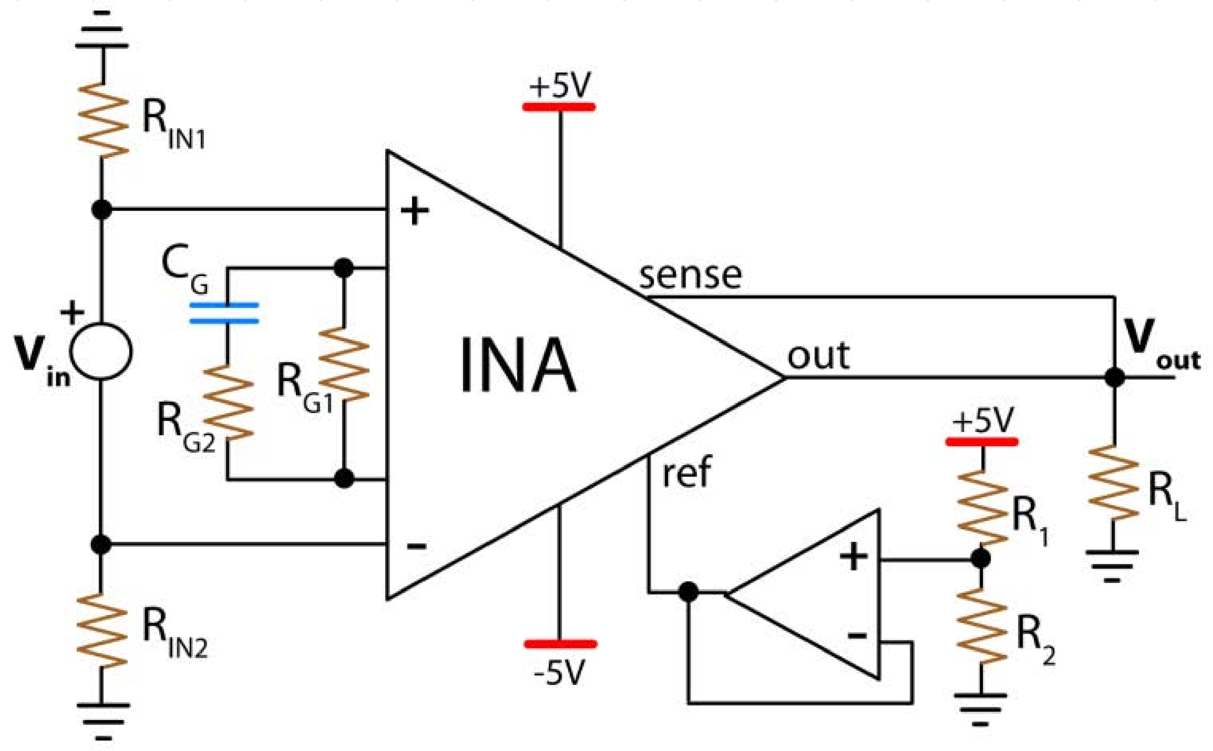
OpAmps: A_0=100dB, GBWP=10MHz, and 1nV/√Hz 1pA/√Hz noise

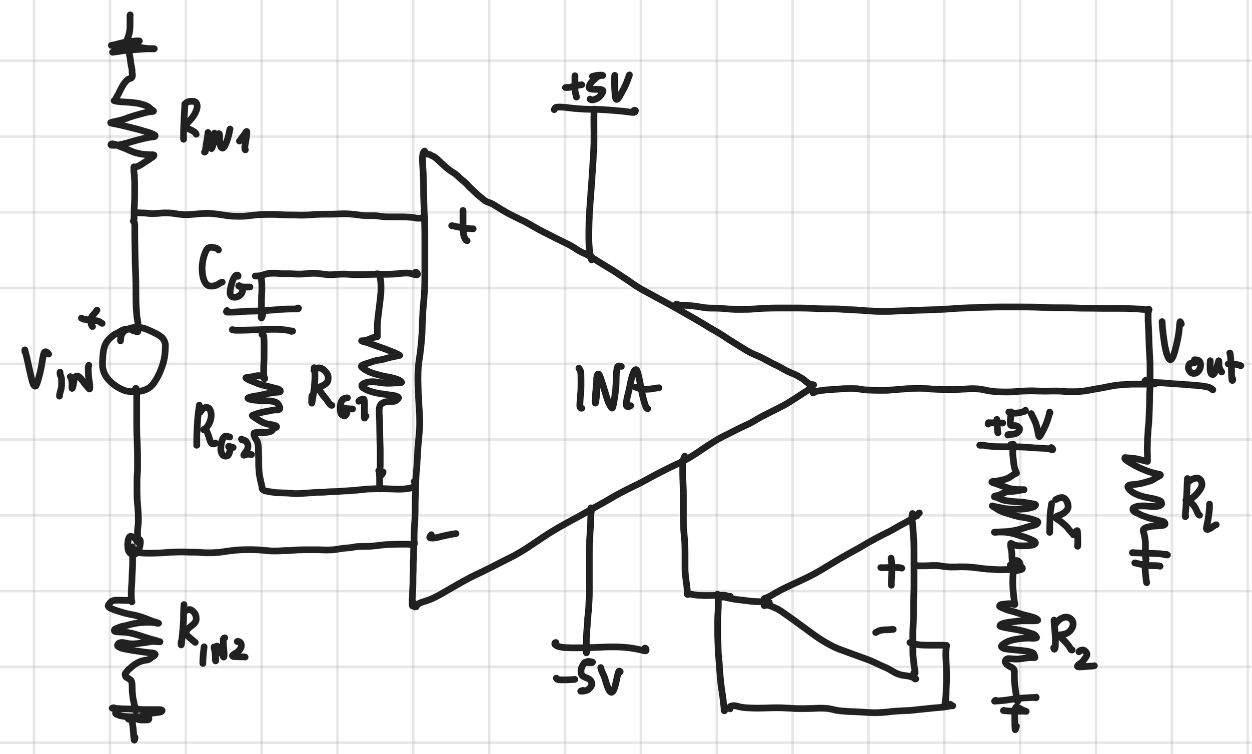
a) Compute output spectral density (neglect 4kTR contributions)

b) Comment on the negligibility of resistors' contributions

(skipped)

1 °





R_{IN1}=100kΩ R_{IN2}=100kΩ R_{G1}=10kΩ R_{G2}=1kΩ C_G=1.6nF R_1=3.3kΩ
R_2= 2.2kΩ R_L=1kΩ all resistors inside INA be 100kΩ

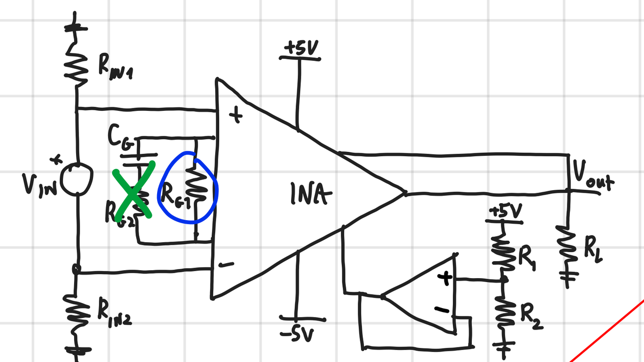
a) Compute V_{out} for V_{in} = 0V

b) Compute the ideal gain v_{out}/v_{in} at low and high frequency

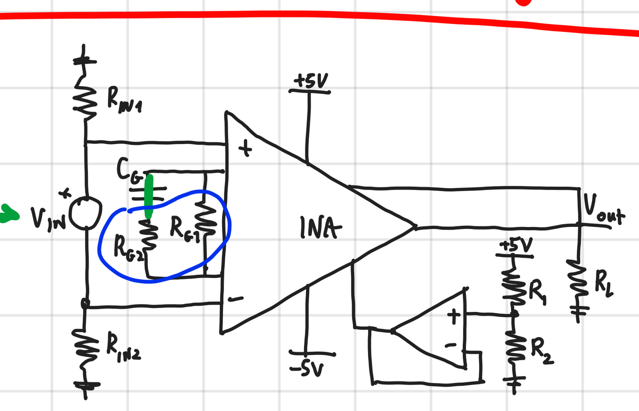
c) Compute poles and zeros

(a) b)

$R_G =$ @ DC → R_{G1} → $G_{INA} = 21$

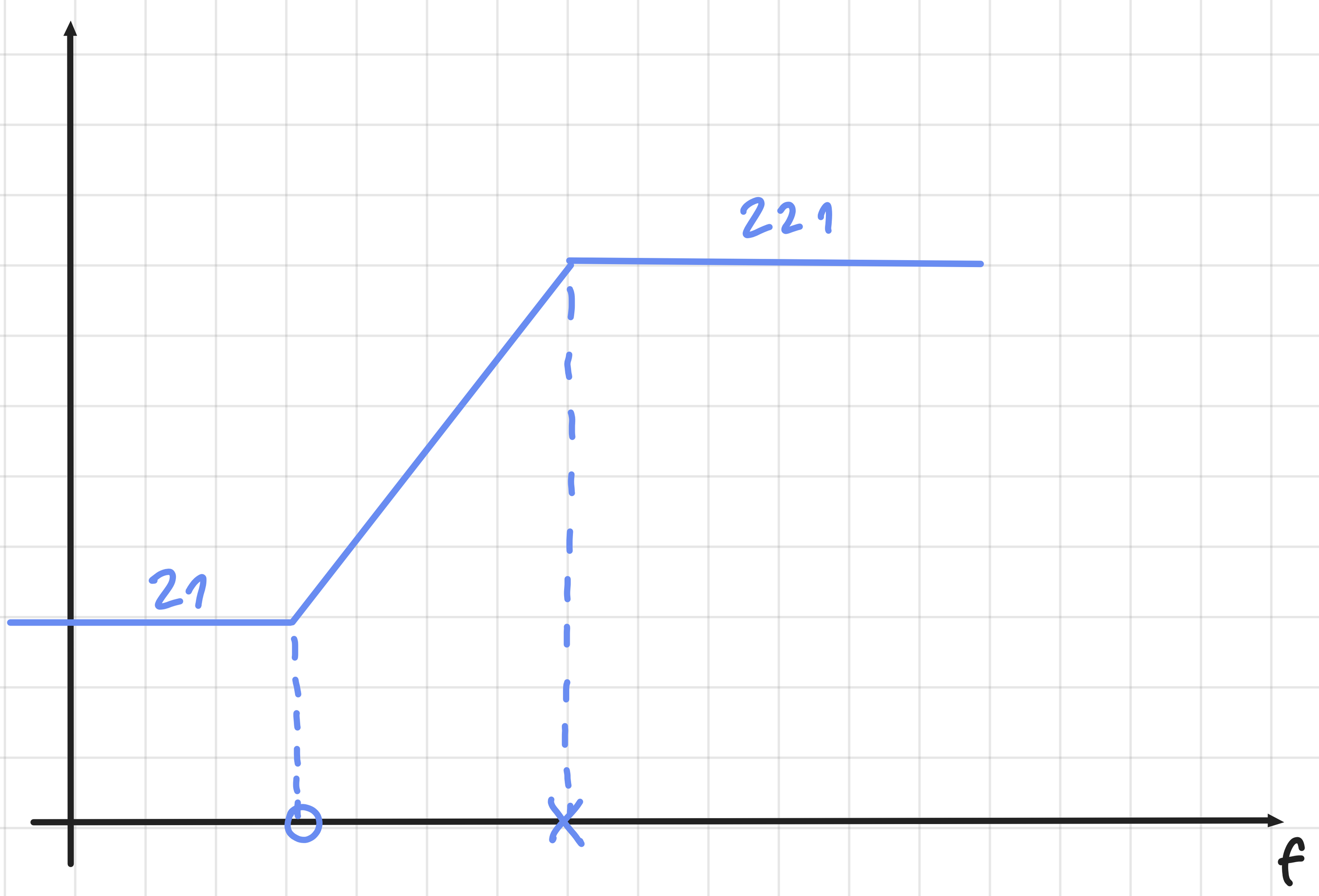


$R_G =$ @ AC → $R_{G1} \| R_{G2}$ → $G_{INA} = 221$



We know: $G_{INA} = 1 + \frac{2R_F}{R_G} = 1 + \frac{200k}{R_G}$

Bode



c) Poles and zeros:

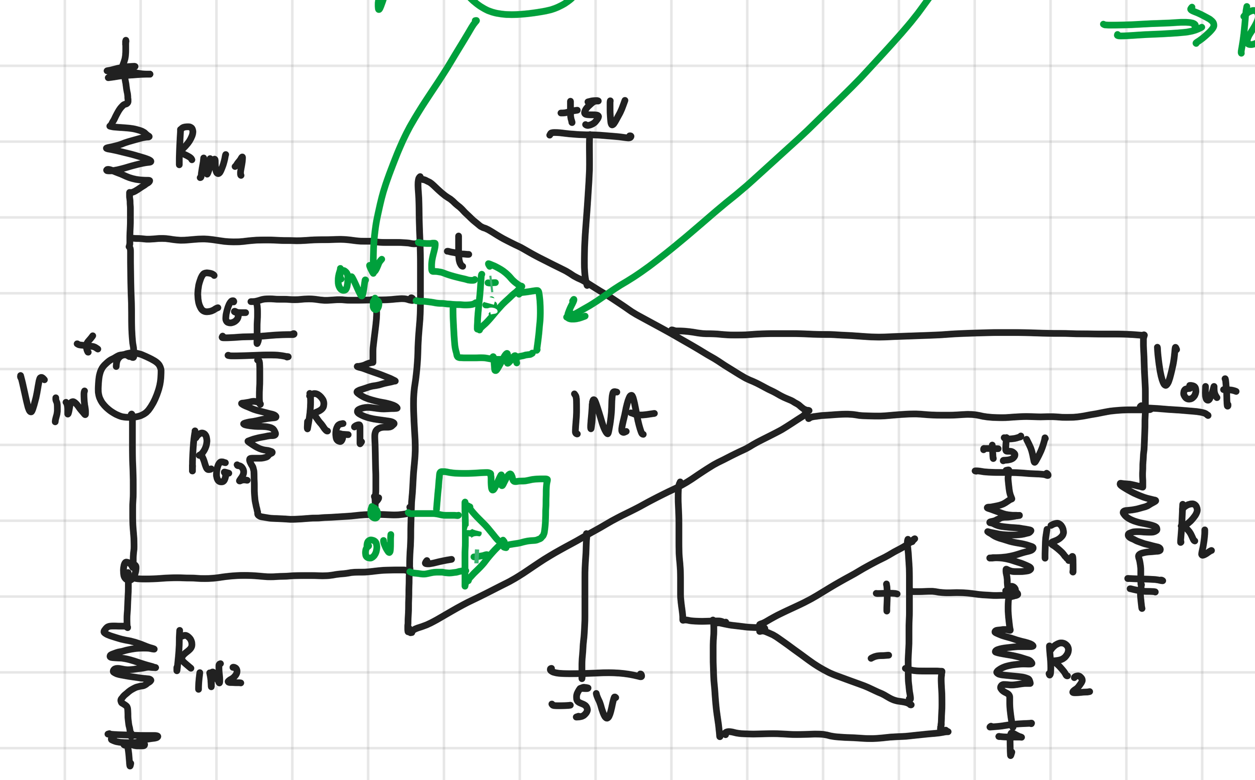
$$\text{pole} = \frac{1}{2\pi C_G R_{G2}}$$

$$\text{zero} = \frac{1}{2\pi C_G (R_{G1}+R_{G2})}$$

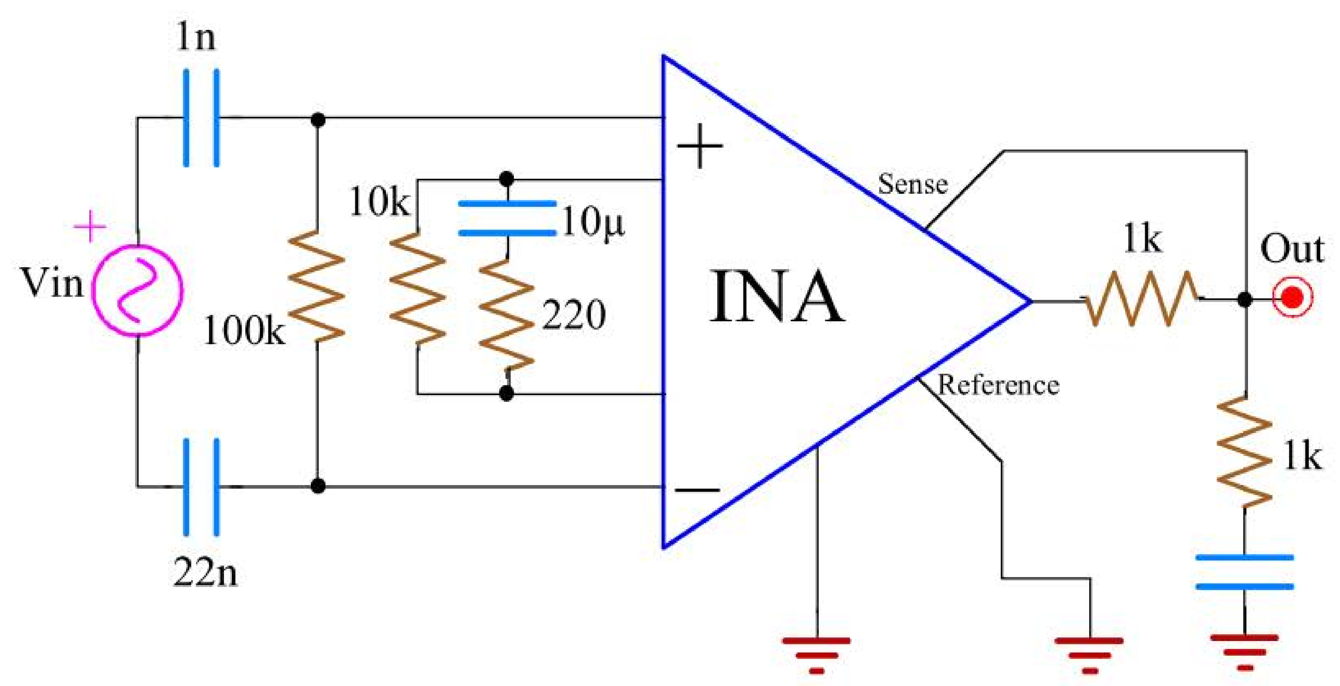
also can be computed graphically

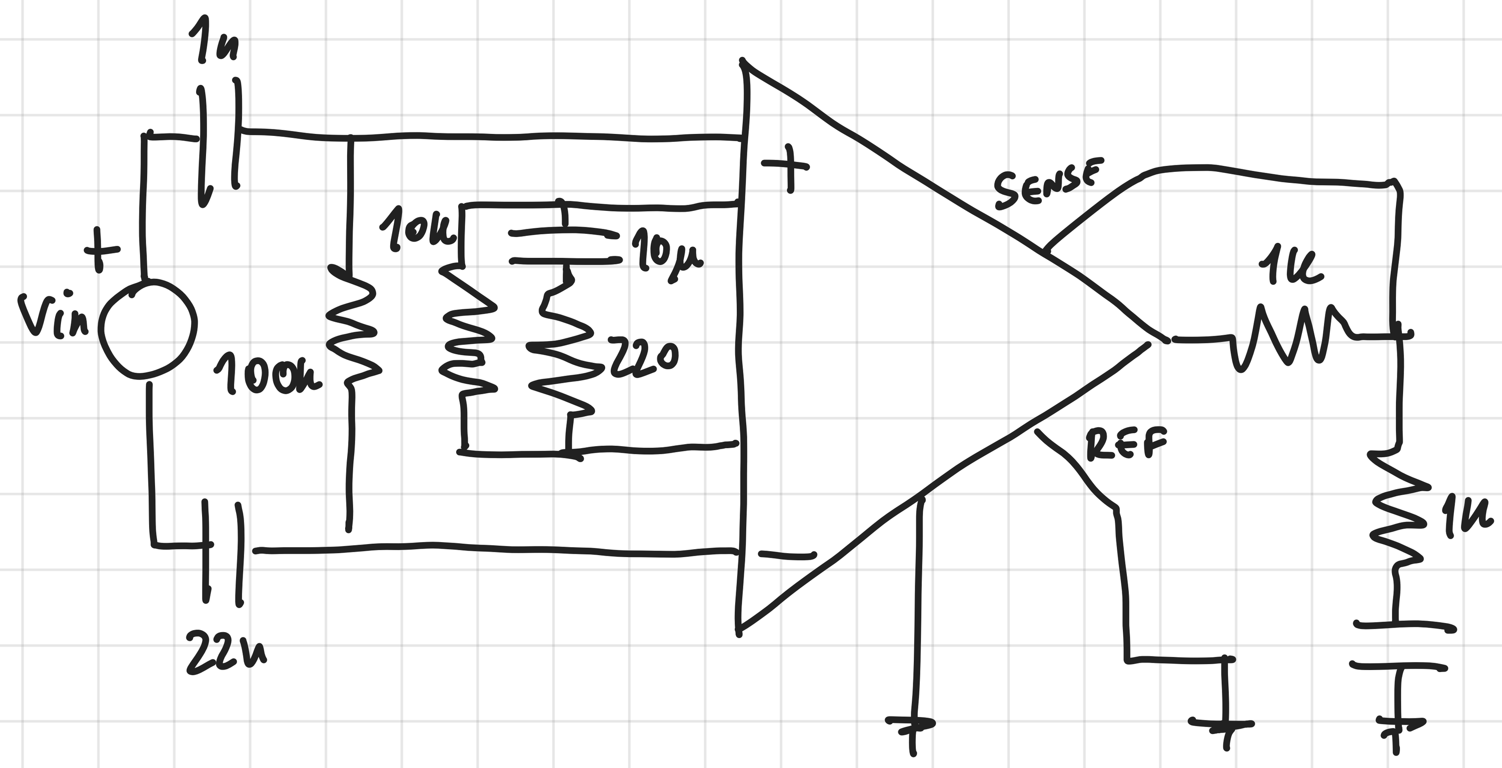
Remember that inside the INA we have these OpAmp → for the computation of the pole (R_{eq}) we have to consider the voltage here = 0

$\Longrightarrow R_{eq} = R_{G2}$



2

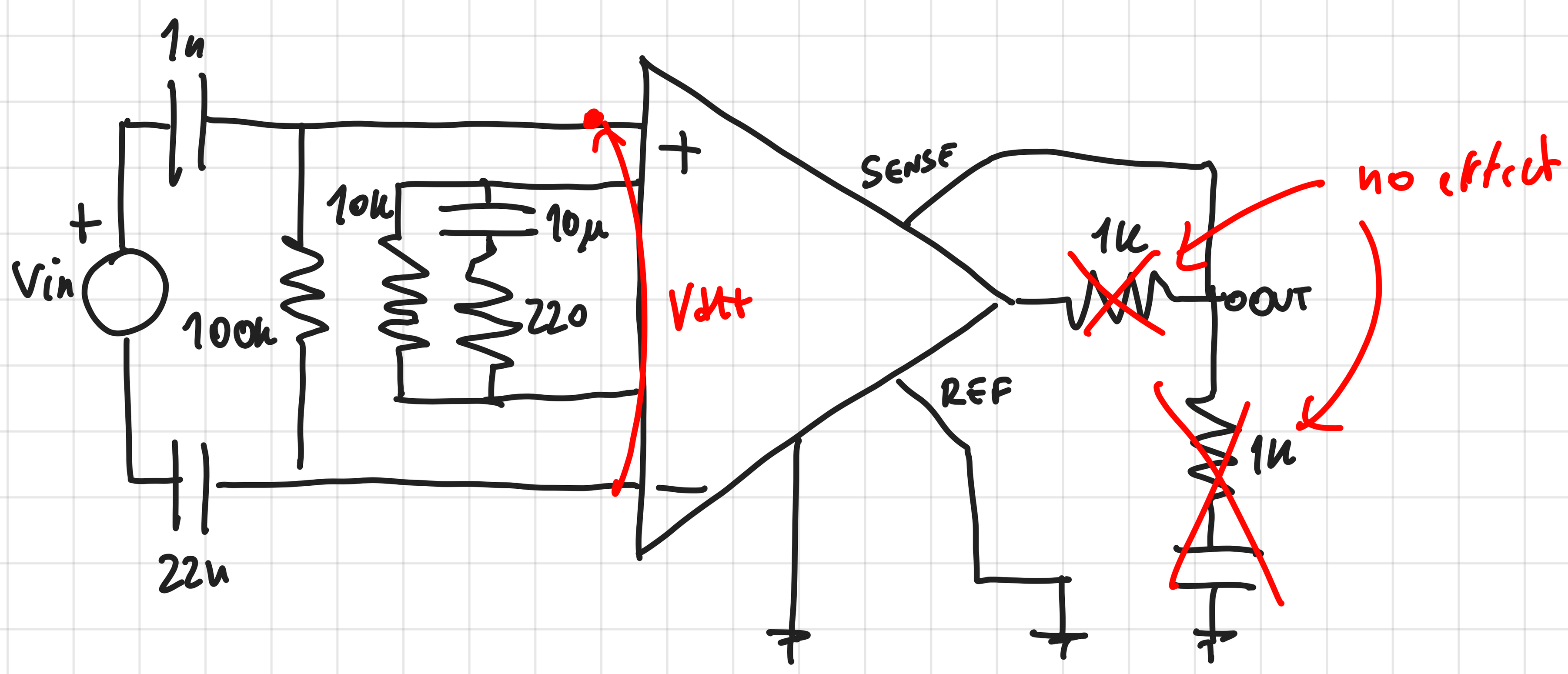




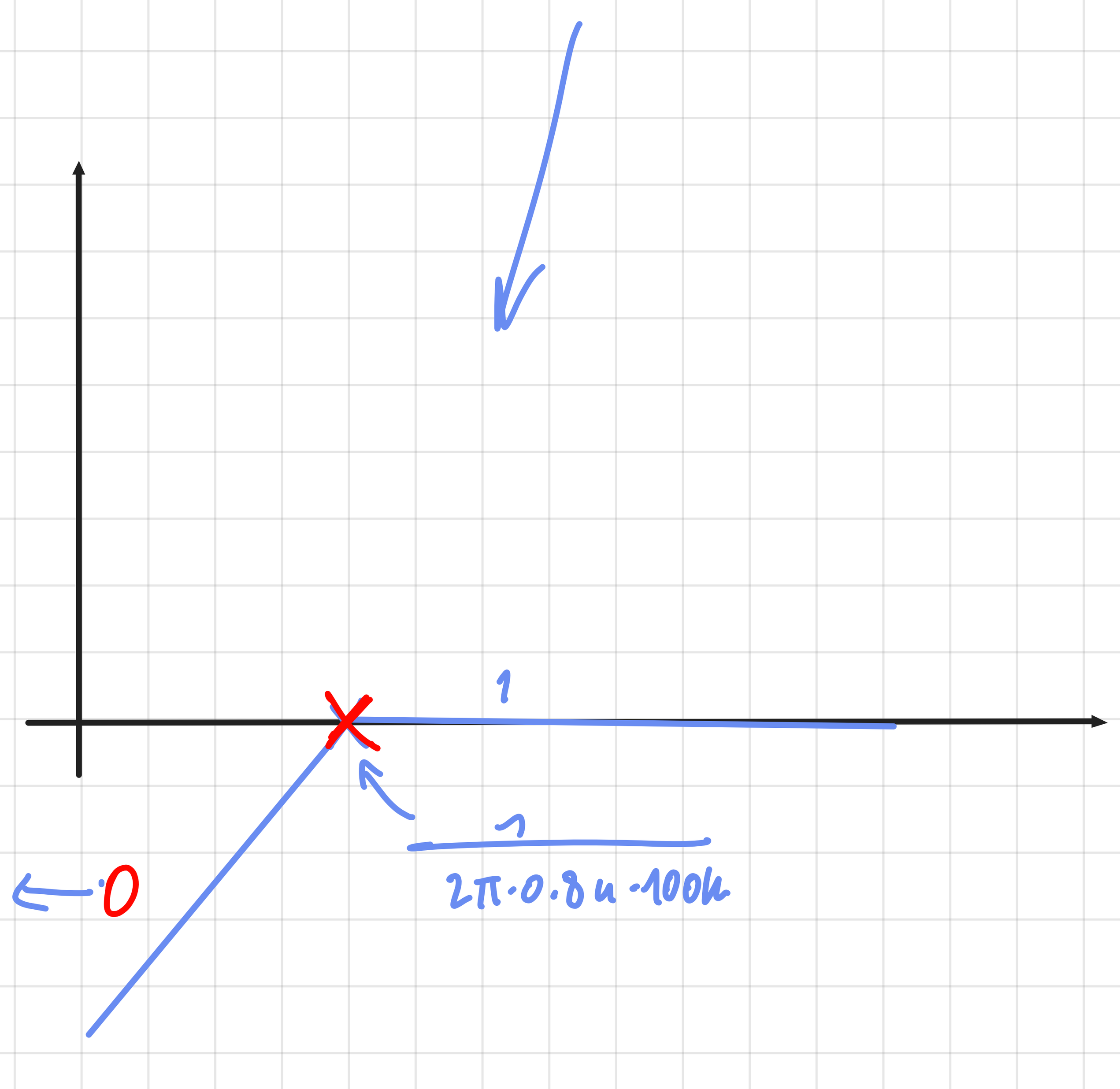
INA with R_f=100kΩ

a) Plot the Bode diagram for the $v_{out}(f)/v_{in}(f)$ **ideal** gain

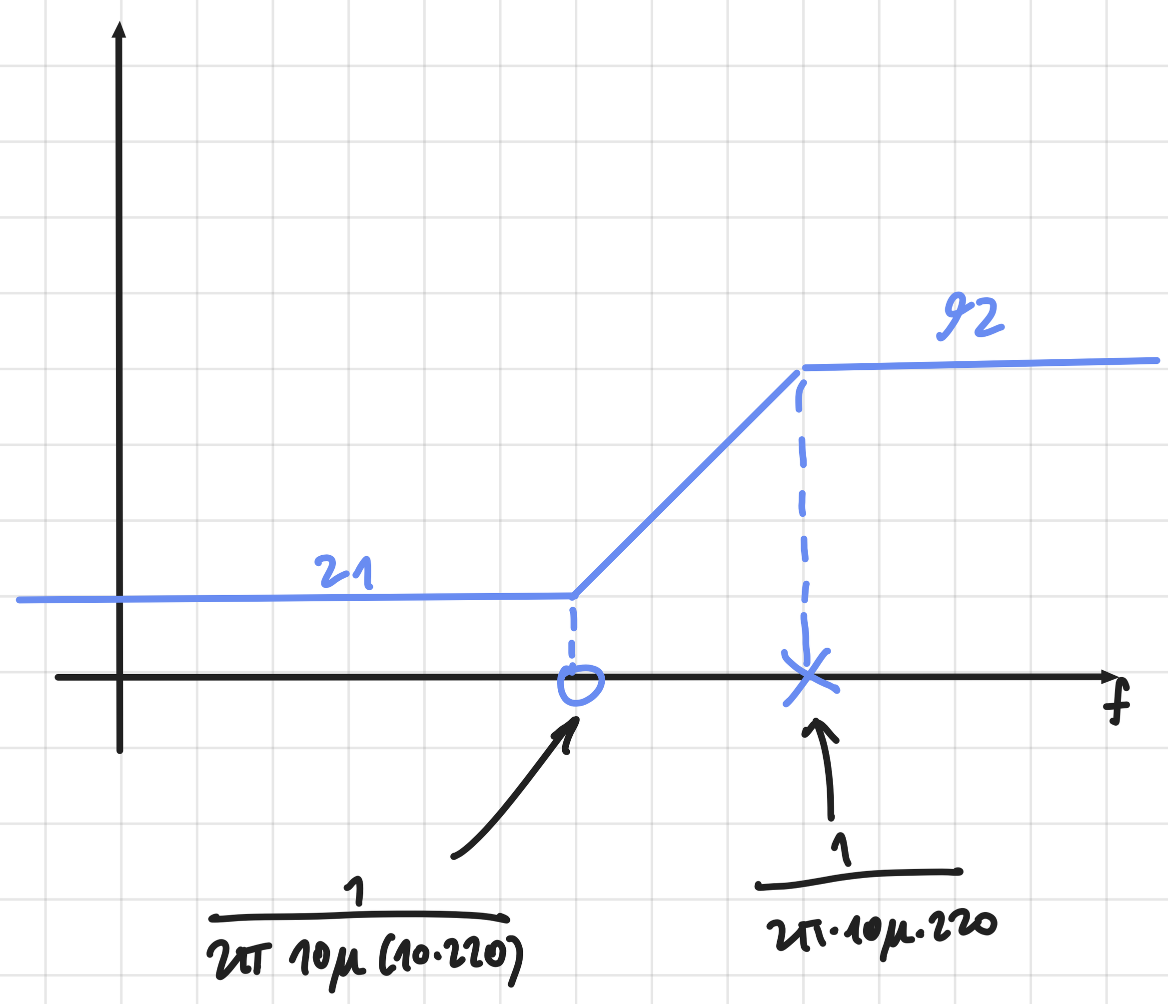
b) Modify the circuit to provide a DC gain of 1000 and a low-pass filtering action with 2 coincident poles at 100kHz



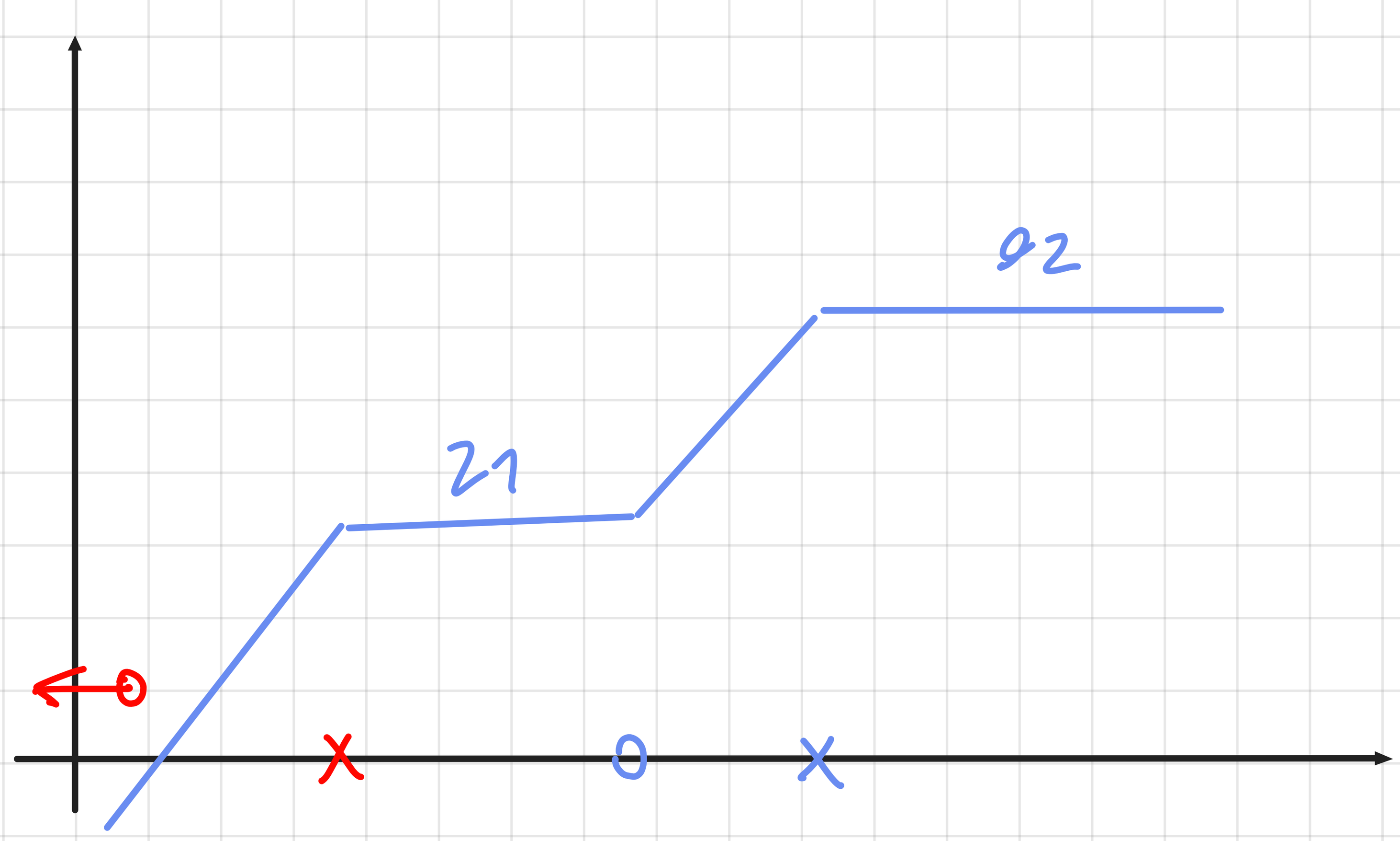
$$C_{in} = \frac{1}{\frac{1}{22n} + \frac{1}{1n}} = \frac{1n \cdot 22n}{1n + 22n} = 0.8\,nF$$



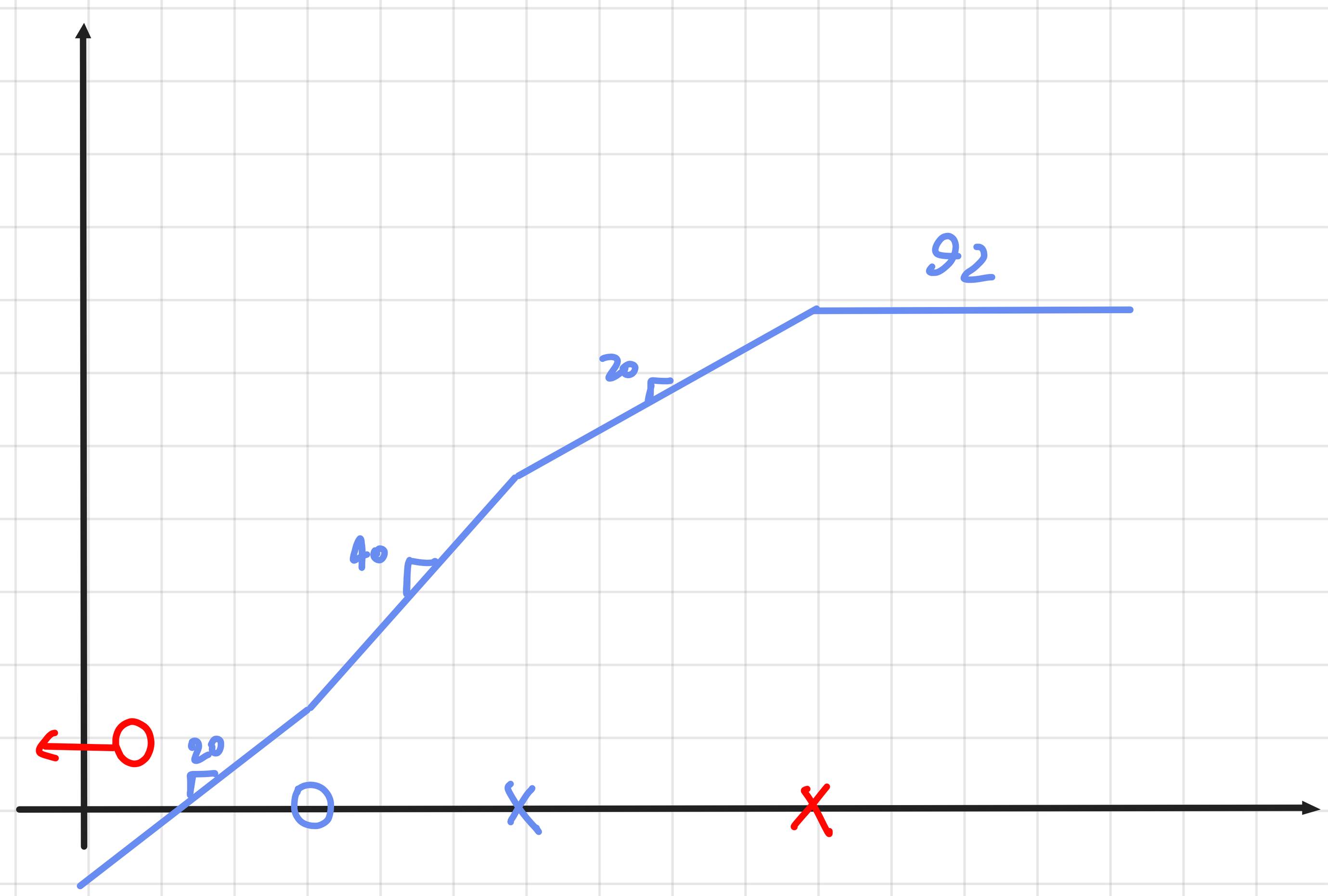
Bode INA



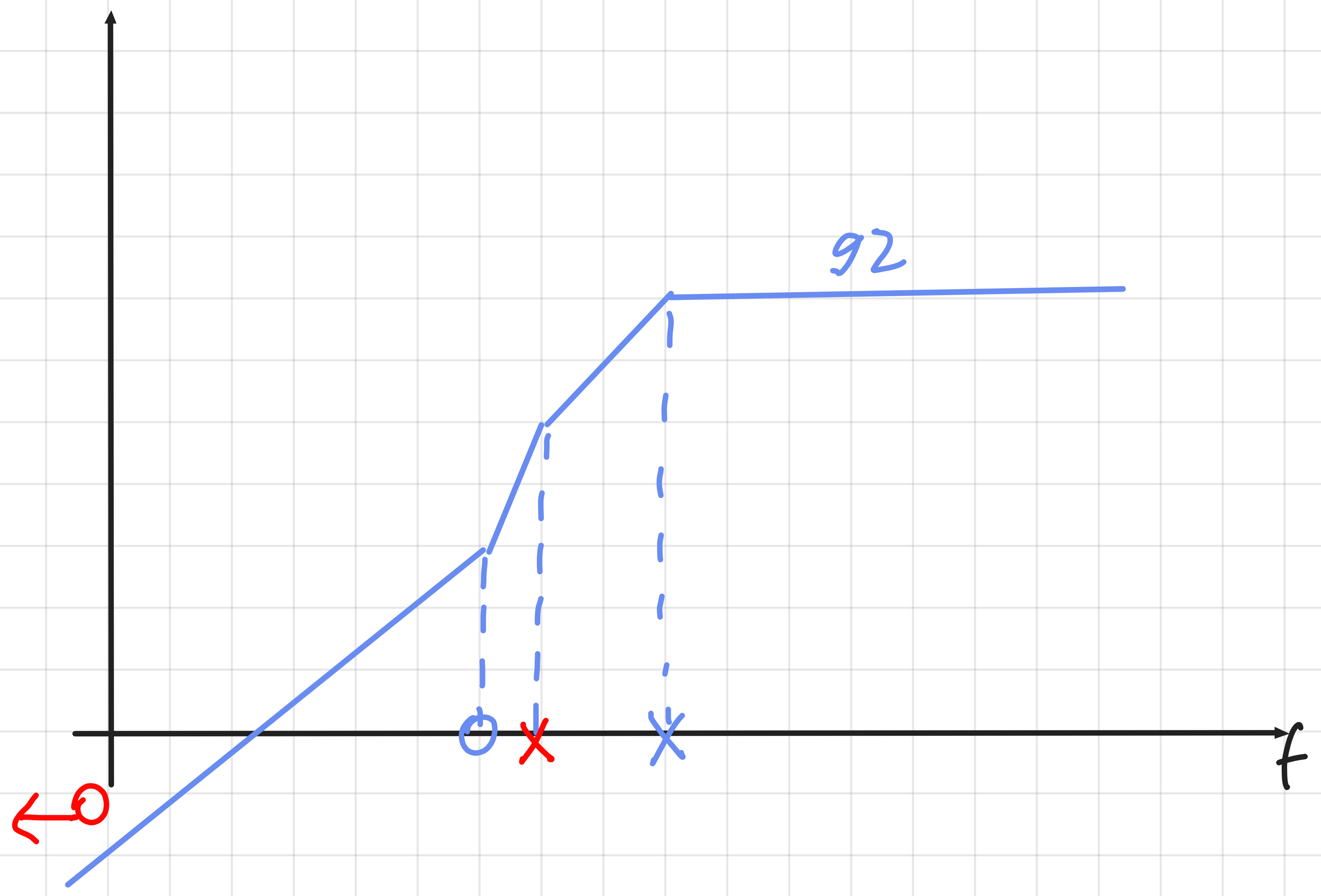
• If × < o



• If × > ×



• If O < X < x



10/11/2022

E02 - Burette

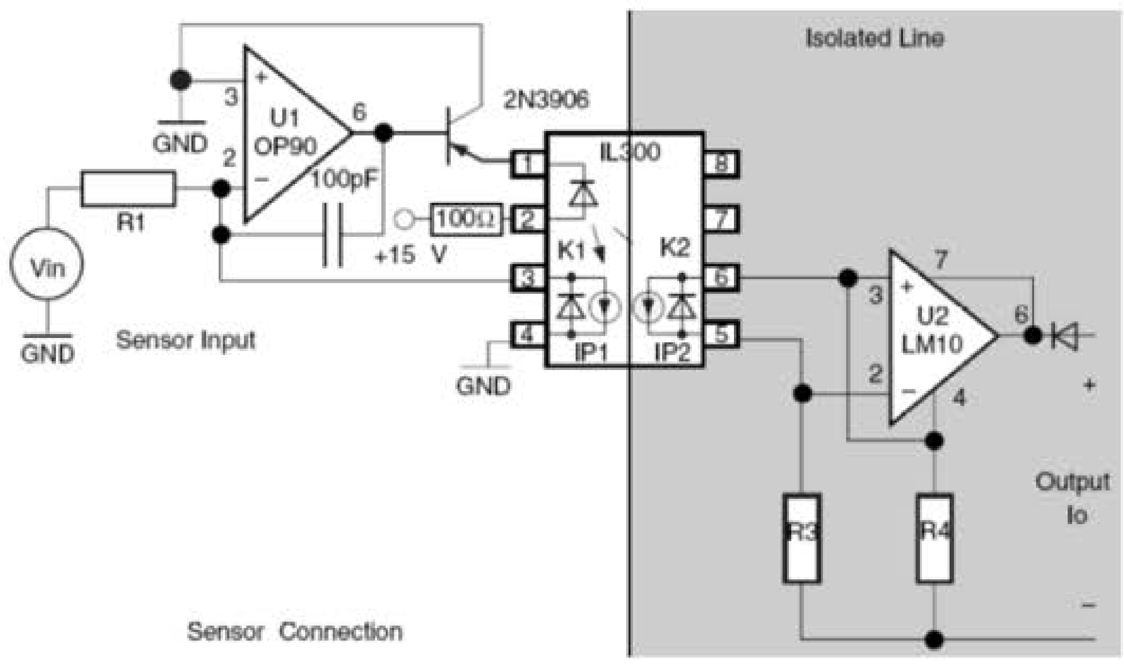
① Ex. 1

OpAmp: A_0=100dB, GBWP=10MHz, I_B=10nA, V_{OS}=5mV. Dual optocoupler with $K_1=K_2=I_{photodiode}/I_{LED}=0.012$. R1= 100 KΩ.

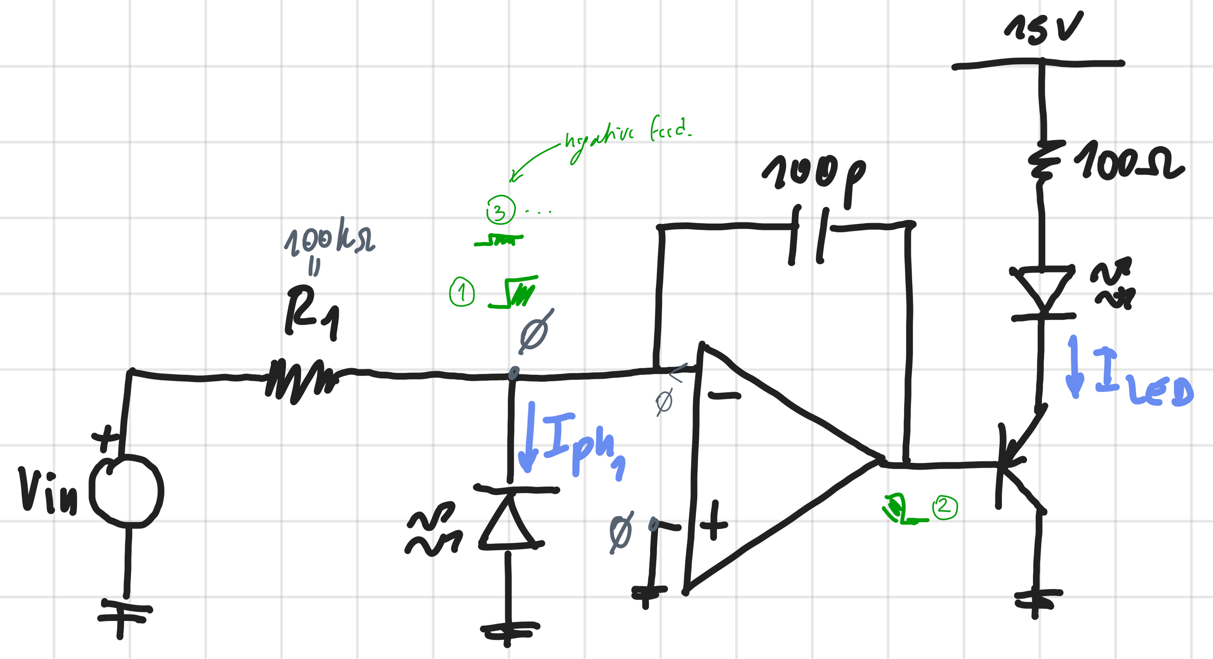
a) Compute the relationship I_{phot2} vs. V_{in}.

b) Study the role of C=100pF on stage stability.

c) Compute the relationship I_o vs. I_{phot2}.



↳ a) $\frac{I_{ph2}}{V_{in}}$?



(• Always check first is neg. feedback!)

• at DC: (C open)

$$\begin{cases} I_{ph1} = \frac{V_{in}}{100k} \\ I_{ph1} = I_{LED}\, k_1 \end{cases}$$

from the Opto coupling: $k_1 = k_2 = \frac{I_{ph\,i}}{I_{LED}} = 0.012$ (i = 1,2)

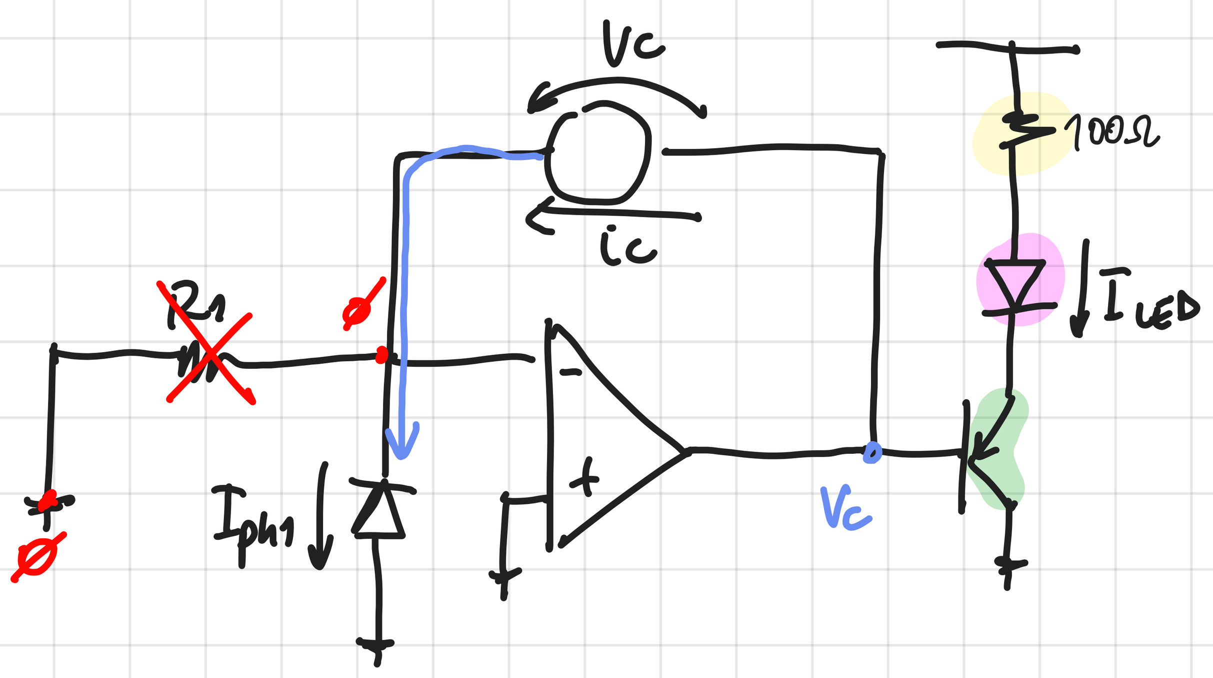
↳ $I_{LED} = \frac{V_{in}}{100k \cdot k_1}$ ⟶ $I_{ph2} = I_{LED} \cdot k_2 = \frac{k_2}{k_1} \boxed{\frac{1}{100k}} \cdot V_{in}$ (gain DC)

↳ $\left.\frac{I_{ph2}}{V_{in}}\right|_{DC} = \frac{1}{100k}$

• at HF: $I_{ph1} = I_{LED} = I_{ph2} = 0$

(C short) ⟹ transistor OFF → LED OFF → PHOTO-DIODES OFF

• pole



→ $i_c = I_{ph1} = k_1 I_{LED}$

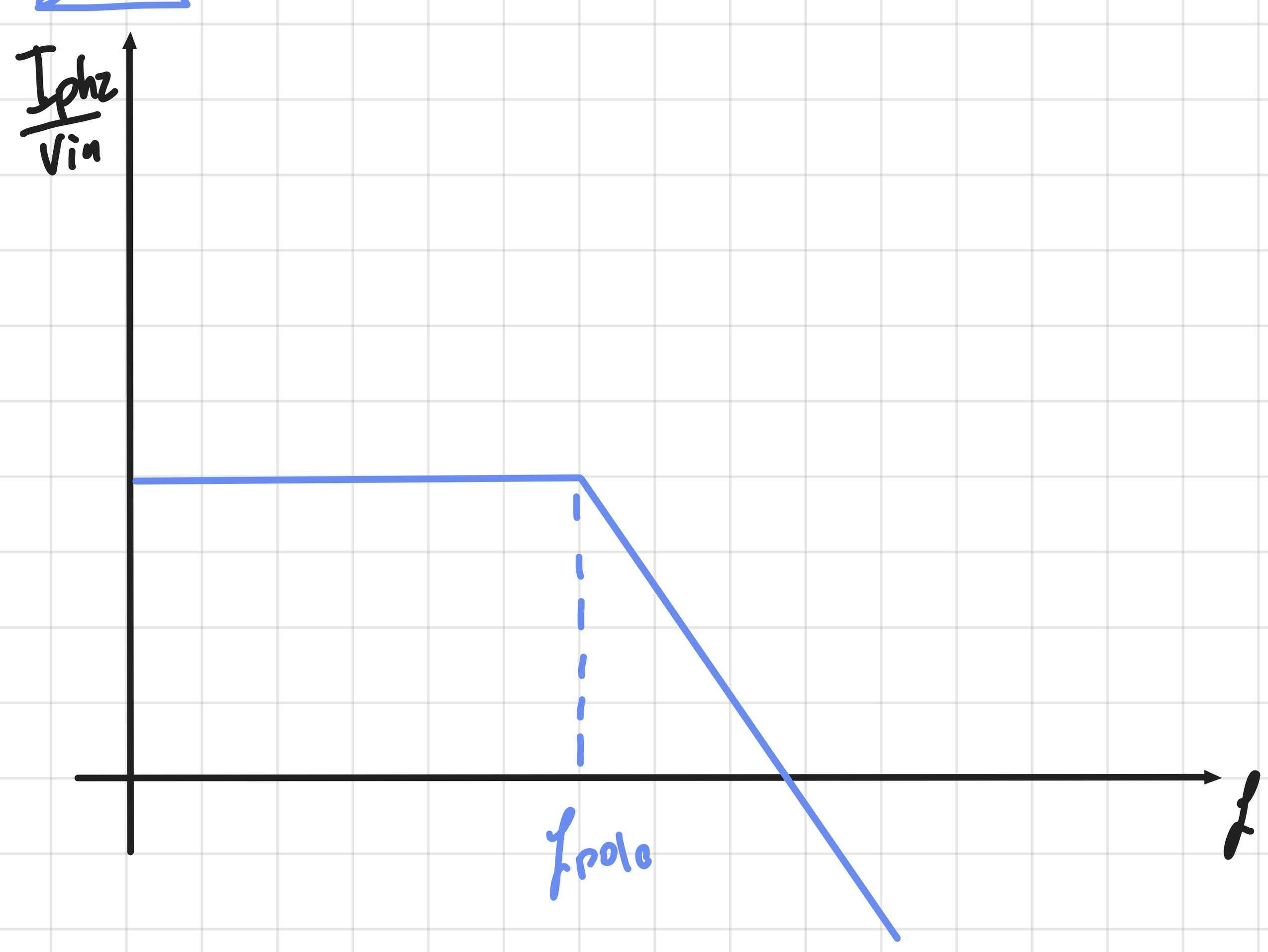
$I_{LED} = \frac{V_c}{\frac{1}{g_m} + R_{LED} + 100\Omega} \simeq \frac{V_c}{100\Omega}$

$i_c = \frac{k_1 V_c}{100\Omega}$

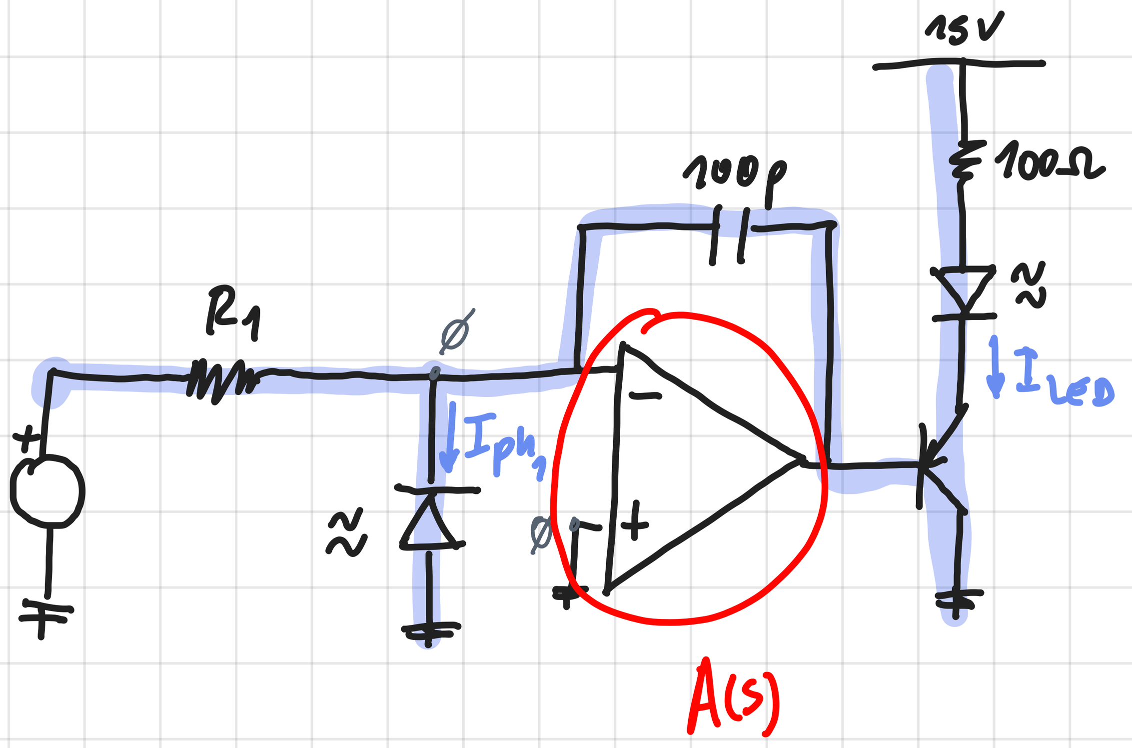
↳ $\frac{V_c}{i_c} \triangleq R_{eq} = \frac{100\Omega}{k_1}$

⟹ $f_{pole} = \frac{1}{2\pi C R_{eq}} = 191\ kHz$

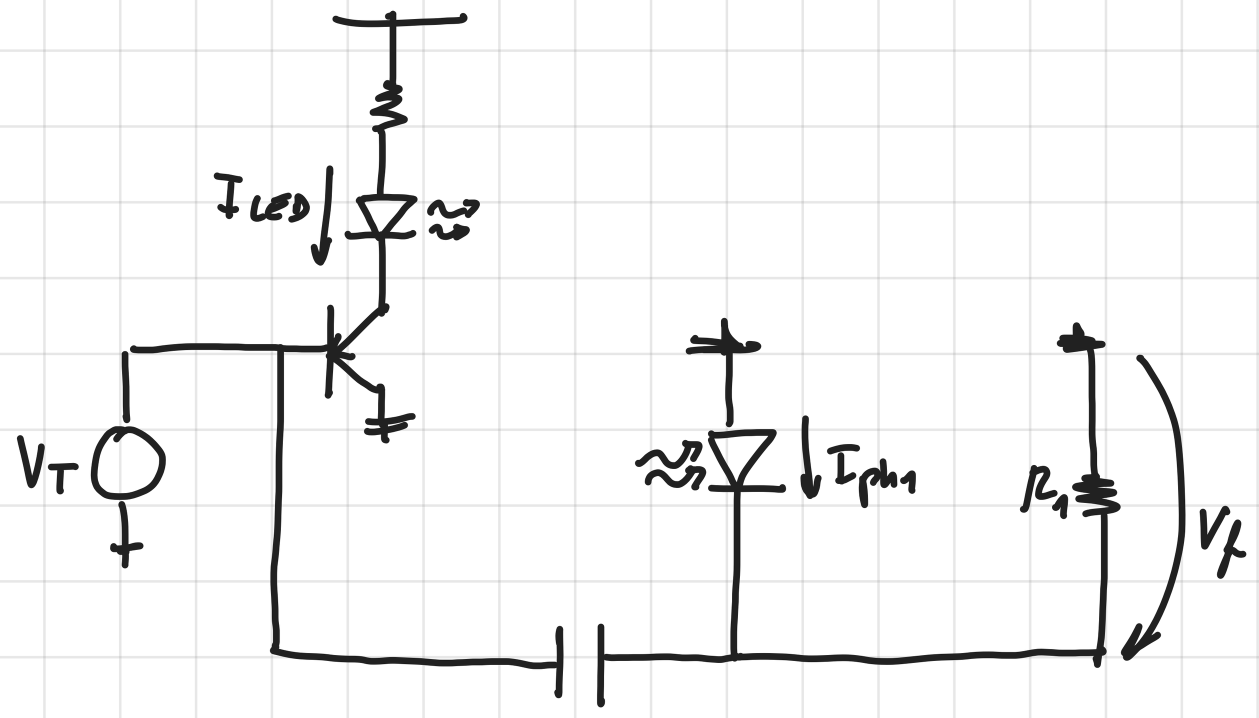
Bode:



b)



→ β(s):



• at DC: (c open)

$V_f = R_1 I_{ph1} = R_1 k_1 I_{LED}$ $\qquad I_{LED} = \dfrac{V_T}{\frac{1}{g_m} + R_{LED} + 100\Omega}$

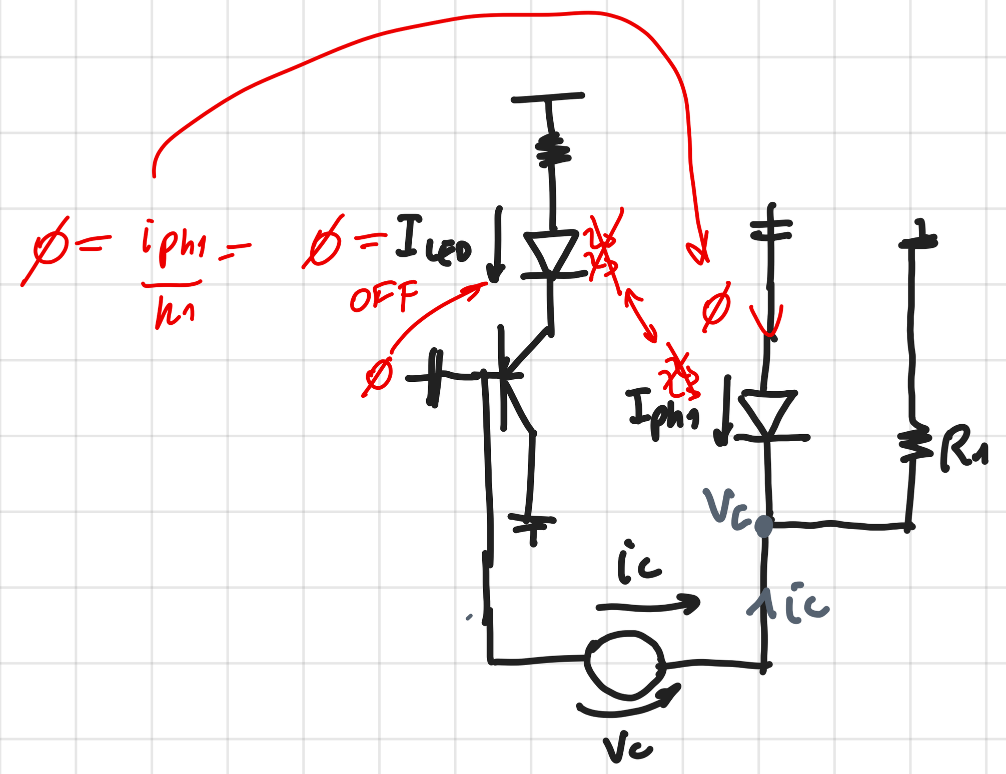
↳ $V_f = \dfrac{V_T}{\frac{1}{g_m} + R_{LED} + 100\Omega} k_1 R_1$

↳ $\beta_{DC} = \dfrac{V_f}{V_T} \simeq \dfrac{k_1 R_1}{100\Omega} \longrightarrow \dfrac{1}{\beta_{DC}} = \dfrac{1}{12}$

• at HF: (C short)

$V_f = V_T$

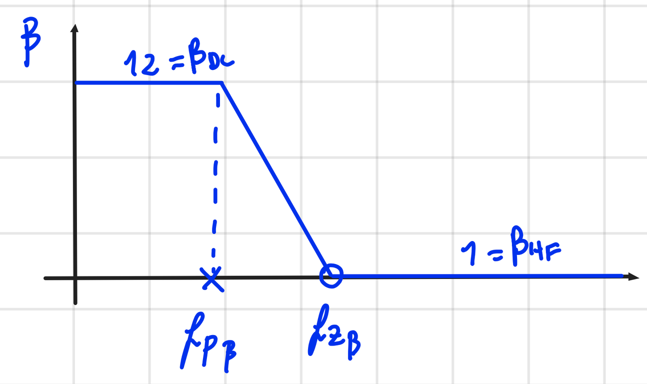
↳ $\beta_{HF} = 1 \longrightarrow \dfrac{1}{\beta_{HF}} = 1$



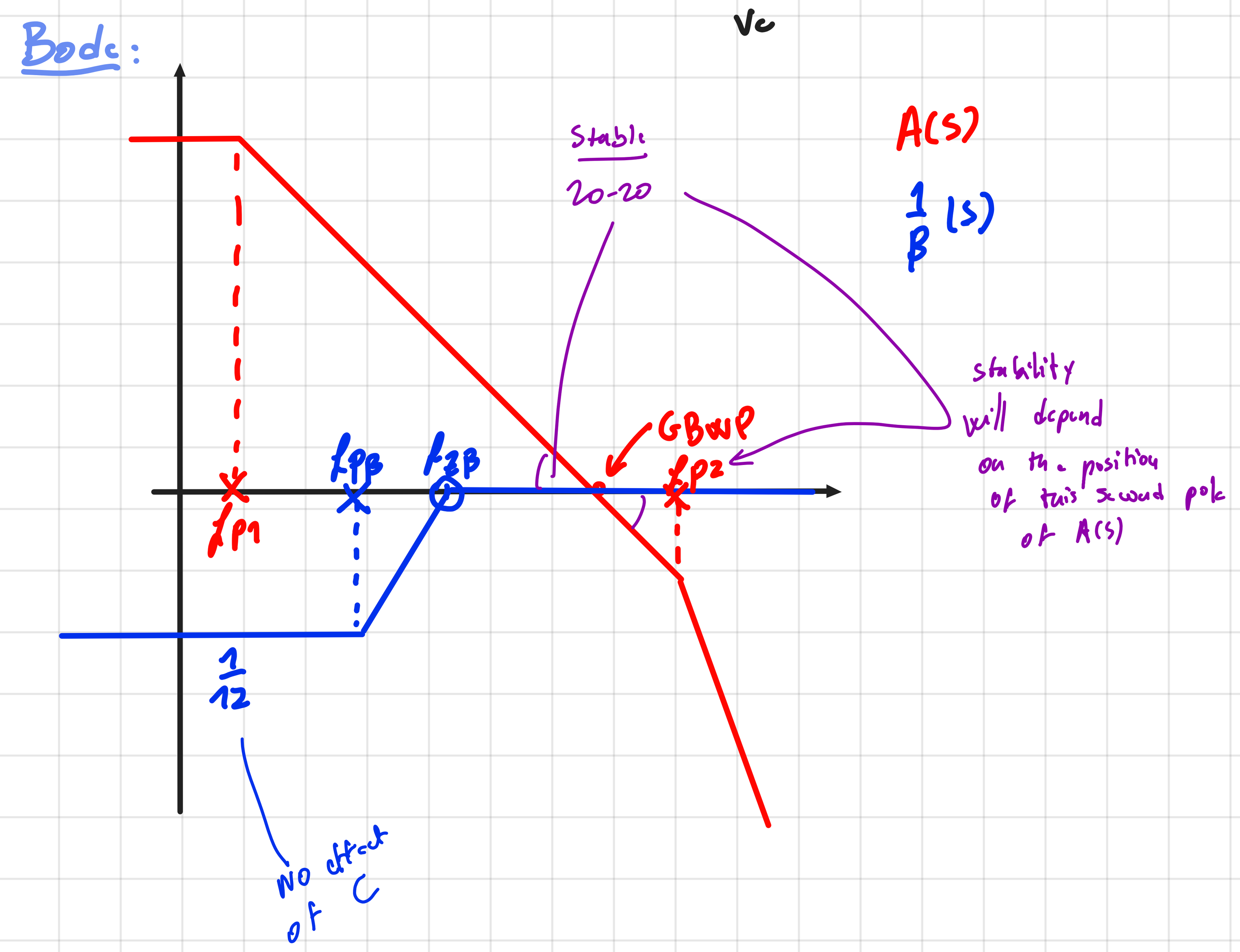
$\Rightarrow \dfrac{V_c}{i_c} = R_{eq} = R_1$

← • pole $\quad f_{p\beta} = \dfrac{1}{2\pi C R_1} = 15.9\,kHz$

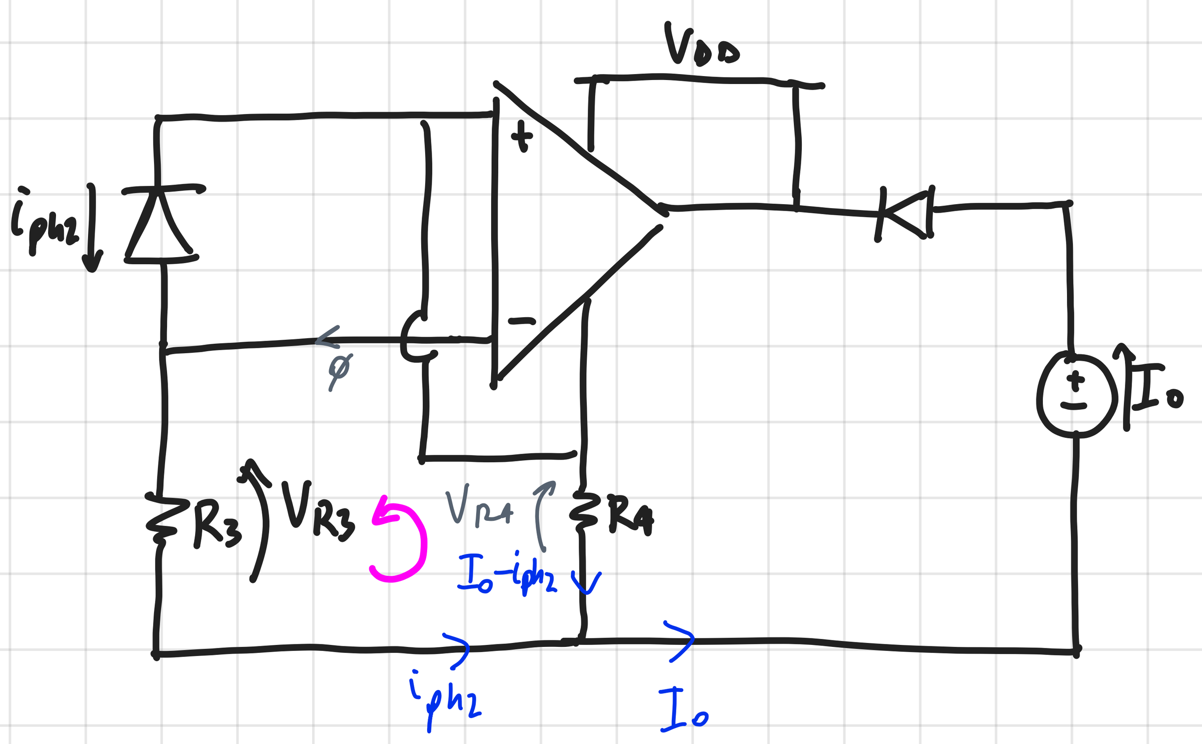
zero (graphically) $\quad f_{z\beta}\, \beta_{HF} = f_{p\beta}\, \beta_{DC} \Longrightarrow f_{z\beta} = 191\,kHz$



Bode:



c)



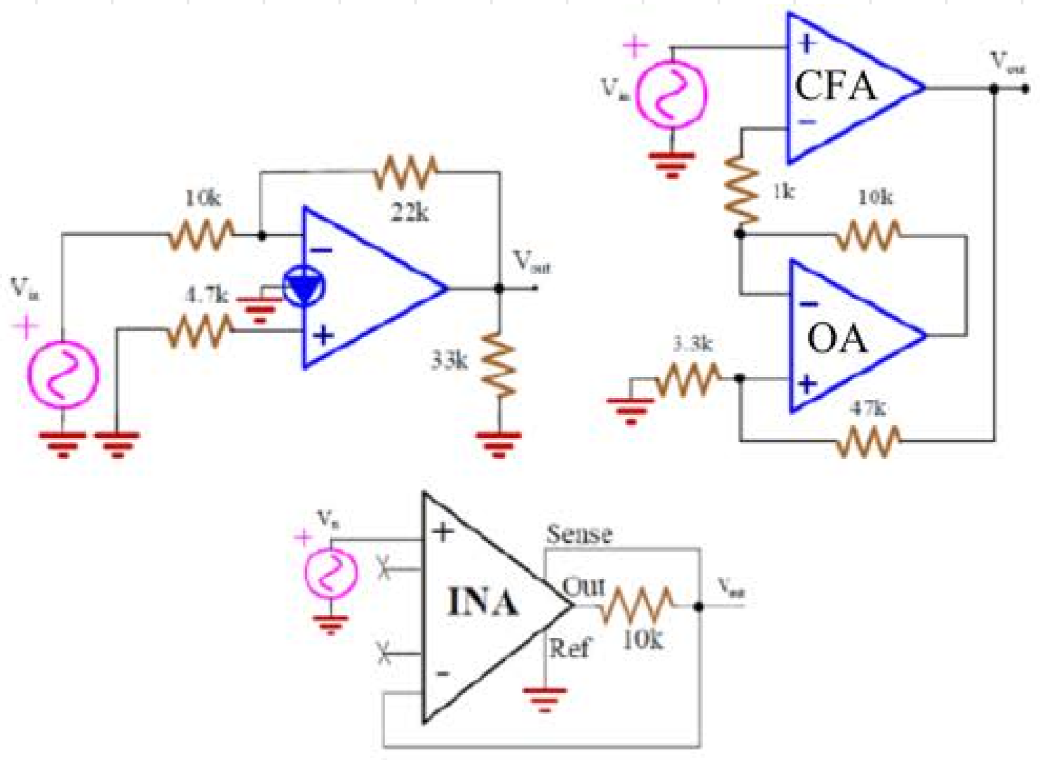
↻: $R_3 i_{ph2} = R_4 (I_o - i_{ph2})$

↳ $\dfrac{I_o}{I_{ph2}} = \underbrace{1 + \dfrac{R_3}{R_4}}_{gain}$

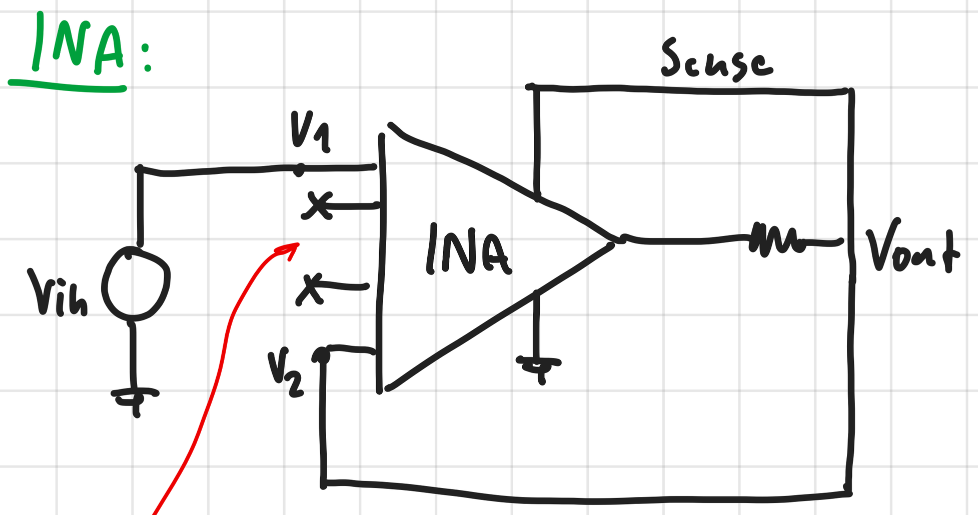
2

Ex. 2

The following blocks utilize INA, CFA and Norton amplifiers.
a) Compute the INA gain V_{out}/V_{in} and give an estimation of the output impedance
b) Compute the gain V_{out}/V_{in} of the Norton system, with $A_i=4$ and give an estimation of the input and output impedances
c) Compute the gain V_{out}/V_{in} of the CFA block.



a) INA:



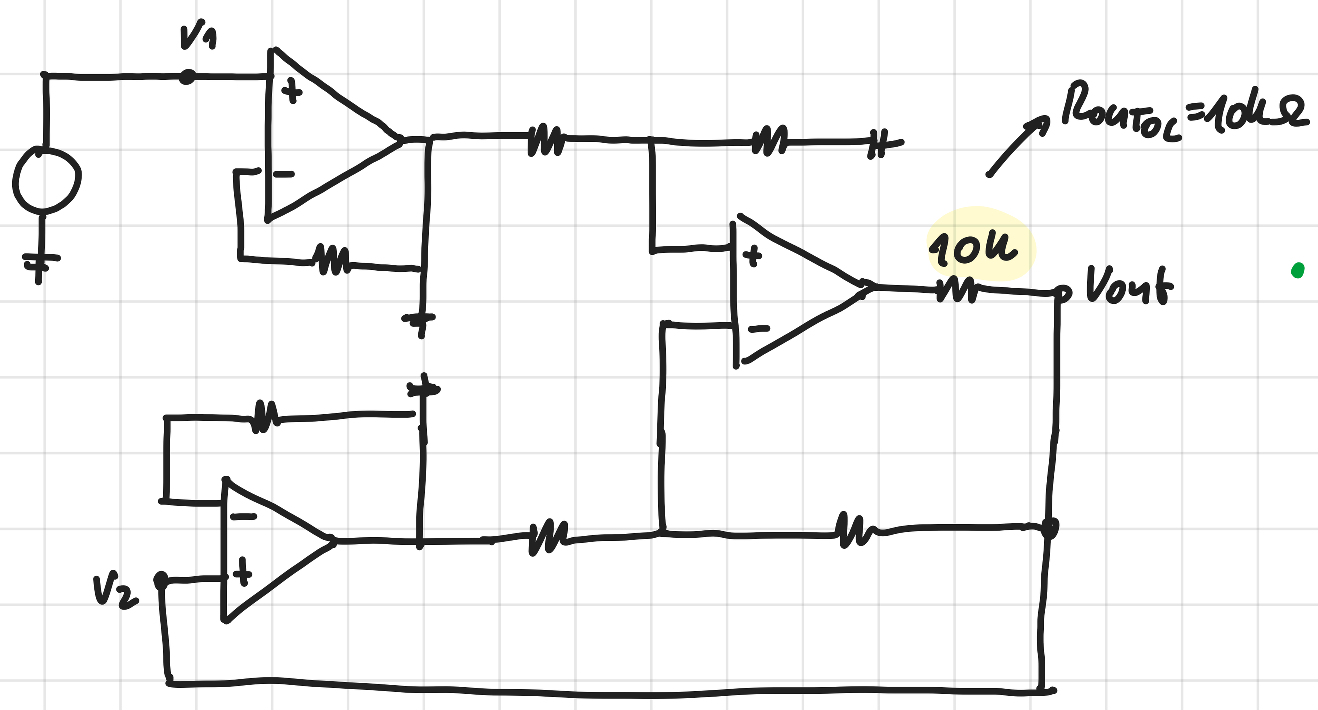
- $\frac{V_{out}}{V_{in}}$?
- Z_{out} ?

No R_G

$\hookrightarrow G_{diff}=1$ $\quad V_1 = V_{in}$, $\quad V_2 = V_{out}$

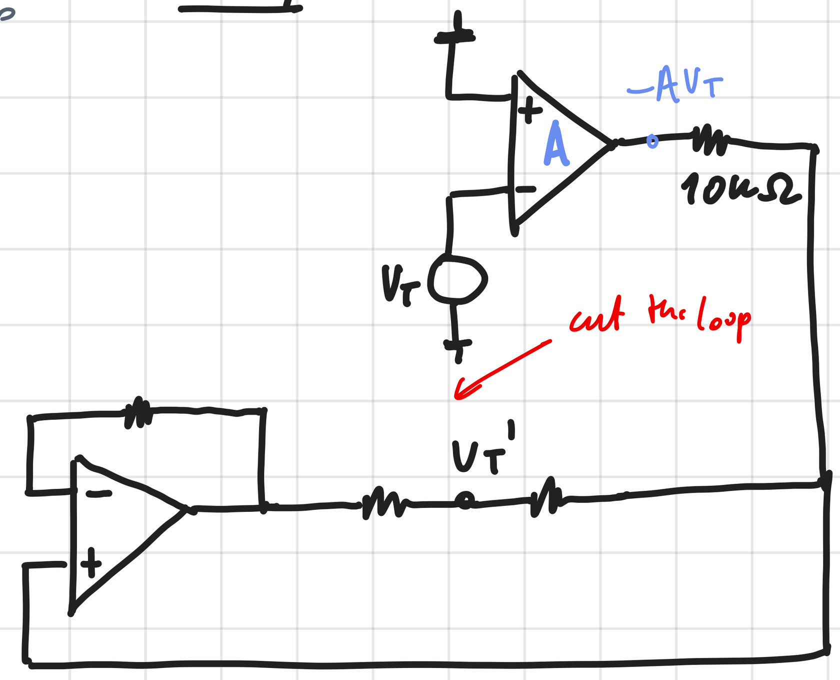
We know: $V_{out} = G_{diff}(V_1 - V_2) = 1\cdot(V_{in}-V_{out}) \rightarrow \frac{V_{out}}{V_{in}} = \frac{1}{2}$

$\hookrightarrow$ For the computation of Z_{out} we consider the internal stage



- $R_{OUT} = \frac{R_{OUT\,OL}}{1-G_{loop}}$ (open loop)

- G_{loop}:

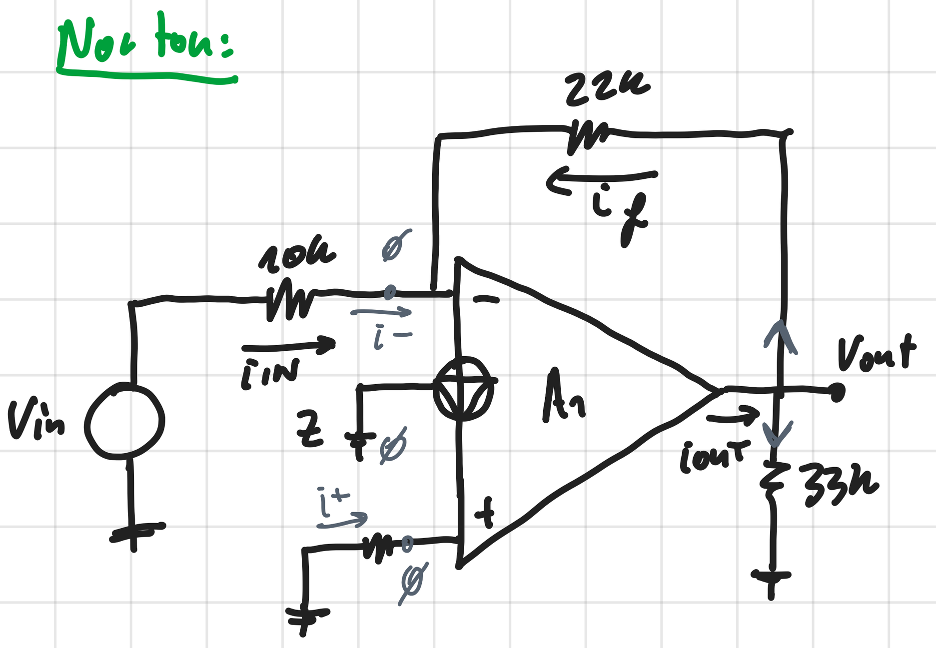


$V_T' = -AV_T$

$\frac{V_T'}{V_T} = -A = G_{loop}$

$\hookrightarrow R_{OUT} = \frac{10k}{1+A} \simeq 0$

b) Norton:



- $\frac{V_{out}}{V_{in}}$?

$A_1 = 4$

- $Z_{in} \cong$?
- $Z_{out} \cong$?

$i^+ = 0$

$i^- = i_{IN} + i_f = \frac{V_{in}}{10k} + i_f$

$i_f = V_{out}\,\frac{33k}{33k+22k}$ (current divider)

$\rightarrow i^- = \frac{V_{in}}{10k} + i_{OUT}\frac{33}{55}$

$i_{OUT} = A_i(i^+ - i^-) \rightarrow i_{OUT} = -A\left(\frac{V_{in}}{10k} + i_{OUT}\frac{33}{55}\right)$

$\hookrightarrow i_{OUT}\left(1 + A\frac{33}{55}\right) = -\frac{A}{10k}V_{in}$

$\Rightarrow i_{OUT} = -\frac{A}{10k}\,\frac{V_{in}}{\left(1+A\frac{33}{55}\right)}$ $\qquad V_{out} = i_{OUT}(33k//22k) = -1.55\,V_{in}$

$\boxed{\frac{V_{out}}{V_{in}} = -1.55}$

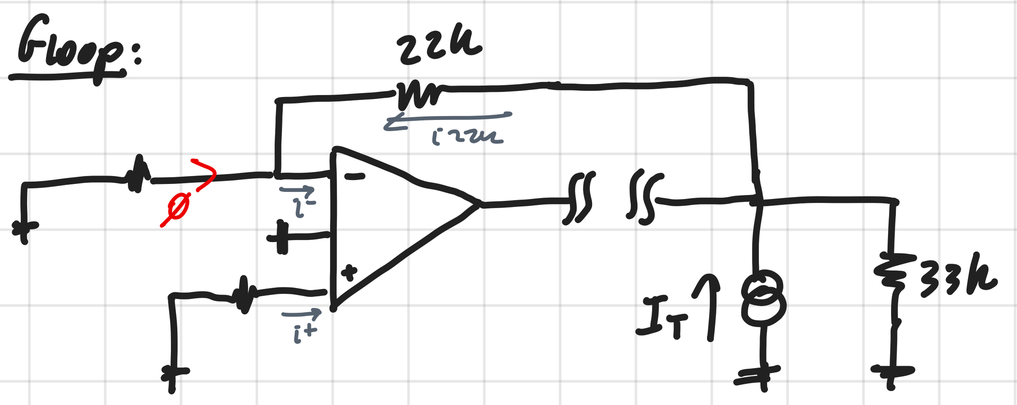
$\rightarrow Z_{in} = R_{in} = 10k\Omega$

$\rightarrow Z_{out} = R_{out} = \frac{R_{OUT\,OL}}{1-G_{loop}}$ (open loop)

$R_{OUT\,OL} = 22k//33k$

$Z_{OUT} = \frac{22k//33k}{1+2.4} = 3.88k\Omega$

- G_{loop}:



$i^+ = 0$

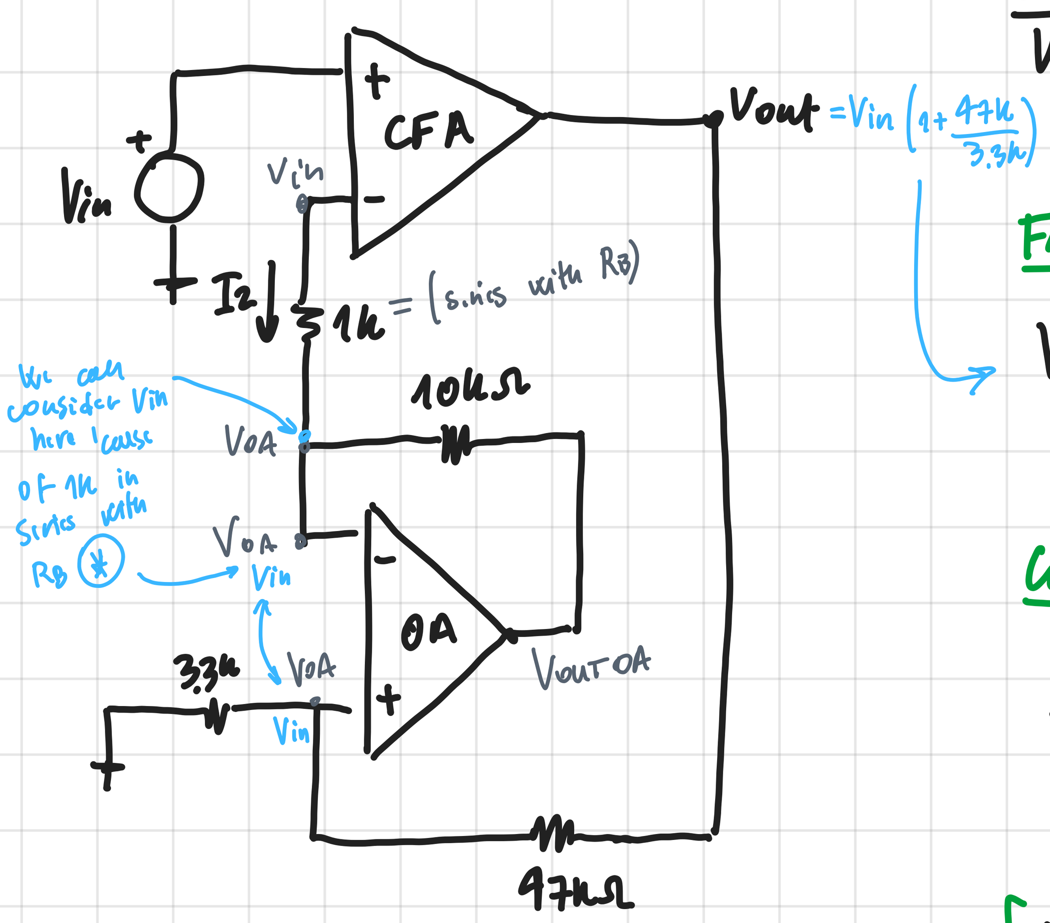
$i^- = i_{22k} = i_T\left(-\frac{33}{55}\right)$

name (subscript) of the curr, not multiplied for 22k

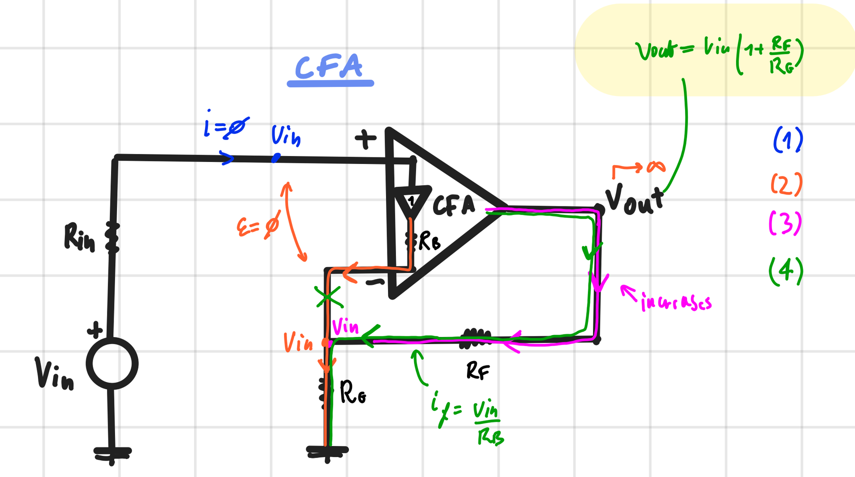
$I_{OUT} = A_1(i^+ - i^-) = -4\,\frac{33}{55}\,i_T$

$G_{loop} = \frac{I_{OUT}}{I_T} = -2.4$

c) CFA:



(*) from lesson notes_ ES07:



$$\frac{V_{out}}{V_{in}} = ?$$

Fast method → Annotations on circuit

$$V_{out} = V_{in}\left(1+\frac{47k}{3.3k}\right) \longrightarrow \frac{V_{out}}{V_{in}} = 15.24\ V$$

Computational method → Annotations

$$V_{OA}^{+} = V_{OA}^{-} = V_{OUT}\,\frac{3.3k\Omega}{47k\Omega+3.3k\Omega} \longrightarrow (*)$$

$$\begin{cases} V_{OUT\,OA} = V_{OA} + \underbrace{\dfrac{V_{OA}-V_{in}}{1k}}_{I_2}\,10k \\[2ex] \dfrac{V_{out\,OA}-V_{OA}}{10k} = \dfrac{V_{in}-V_{OA}}{1k} \qquad \text{KLC} \end{cases}$$

$$\longrightarrow V_{out\,OA} = 10k\left(\frac{V_{in}}{1k}\right) - V_{OA}\left(\frac{1}{1k}-\frac{1}{10k}\right)$$

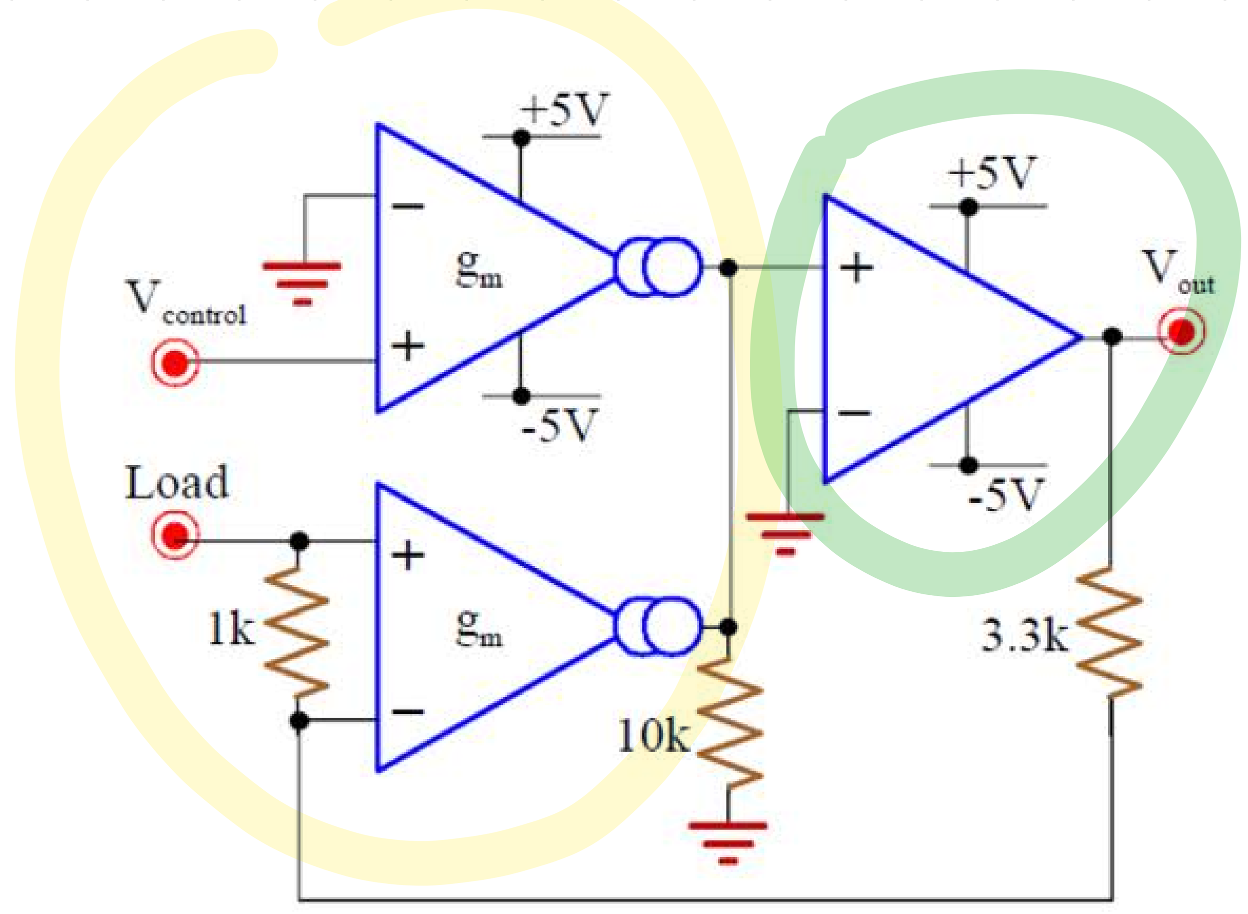
$$(*)\quad 10k\left(\frac{V_{in}}{1k}\right) - V_{out}\frac{3.3k}{47k+3.3k}\left(\frac{1}{1k}-\frac{1}{10k}\right) = V_{out}\,\frac{3.3k}{47k+3.3k} + \frac{V_{out}\frac{3.3k}{47k+3.3k} - V_{in}}{1k}\cdot 10k$$

$$\hookrightarrow \frac{V_{out}}{V_{in}} = 15.24\ V$$

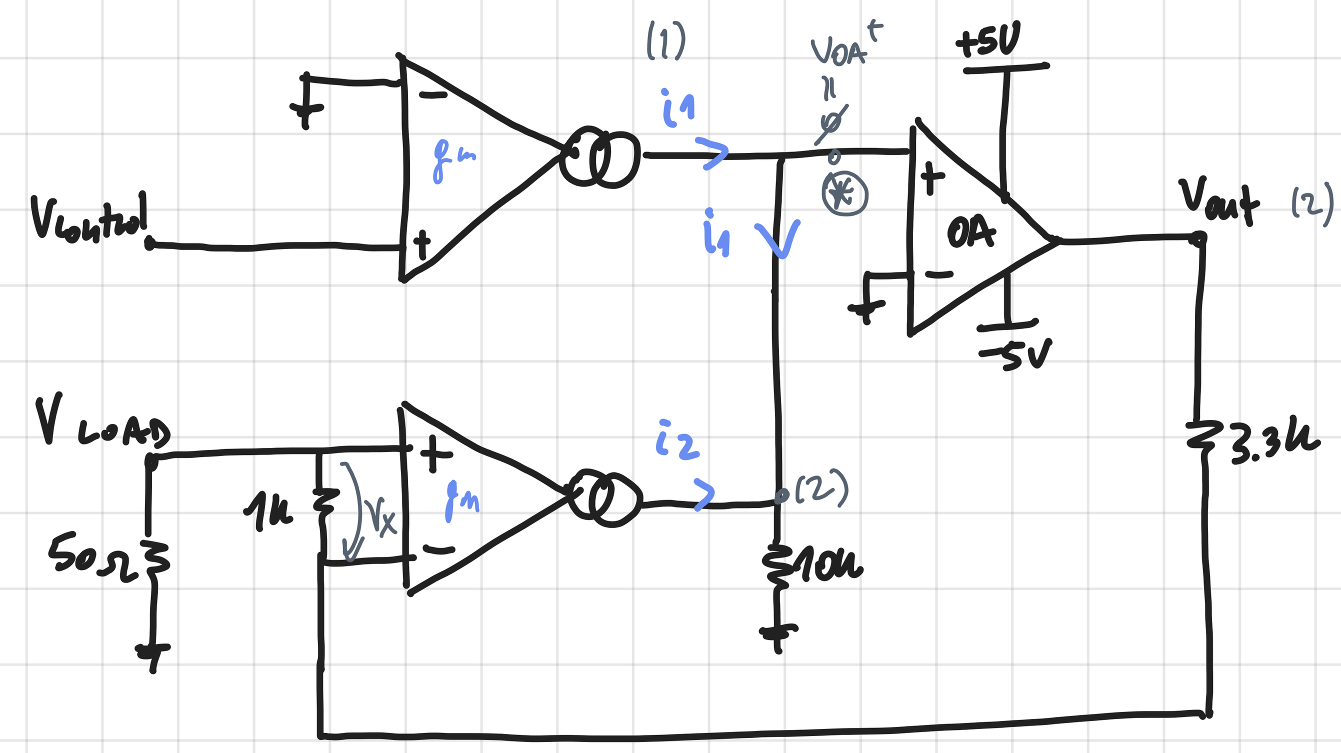
③

Ex. 3

OpAmp with A0=100dB, GBWP=20MHz, IB=10nA, VOS=0.5mV, output swing -3÷+3V.
OTAs with gm=10mS, output swing -4÷+4V.
Connect a 50Ω load at the Load output.
a) Compute VLoad/Vcontrol and Vout/Vcontrol and describe the function of the circuit.
b) Compute the error at the Load, caused by the IB of the OpAmp.



a)



(Always check NEG. feedback first)

- $\frac{V_{LOAD}}{V_{control}} = ?$
- $\frac{V_{OUT}}{V_{control}} = ?$

(1) increase i_1
(2) Voltage accross 10k ↑ , Vout ↑
(3) Feedback action ⇒ i_2↓ to decrease voltage across 10k

such that $i_1 + i_2 = i_R = 0$ (to have virtual ground)

We have that for OTAs:

$$\begin{cases} i_1 = V_{control} \cdot g_{m1} \\ i_2 = V_X \cdot g_{m2} = V_{out} \dfrac{1k}{50 + 1k + 3.3k} g_{m2} \end{cases}$$

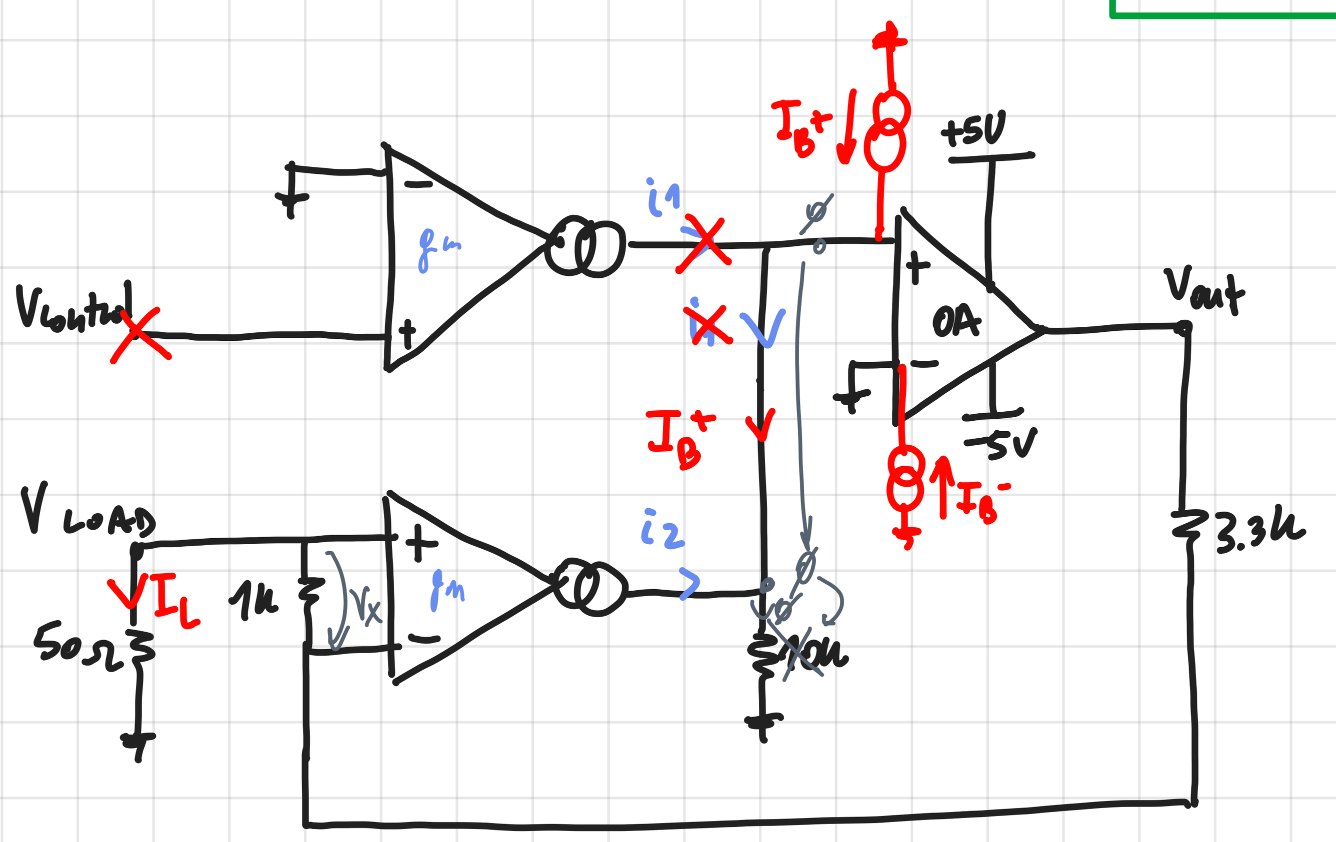
$i_1 + i_2 = i_R = 0$ $\quad i_1 = -i_2$ $\quad (V_{OA}^+ = 0V)$

$$V_{control}\, \cancel{g_{m1}} = V_{out} \frac{1k}{50 + 1k + 3.3k} \cancel{g_{m2}}$$

$$\boxed{\frac{V_{out}}{V_{control}} = \frac{50 + 1k + 3.3k}{1k} = 4.35}$$

$$V_{LOAD} = V_{out} \frac{50}{50 + 1k + 3.3k} \Rightarrow \boxed{\frac{V_{LOAD}}{V_{control}} = 0.05}$$

b)



$\varepsilon_{I_B^-} = 0$ (no error contribution from I_B^-)

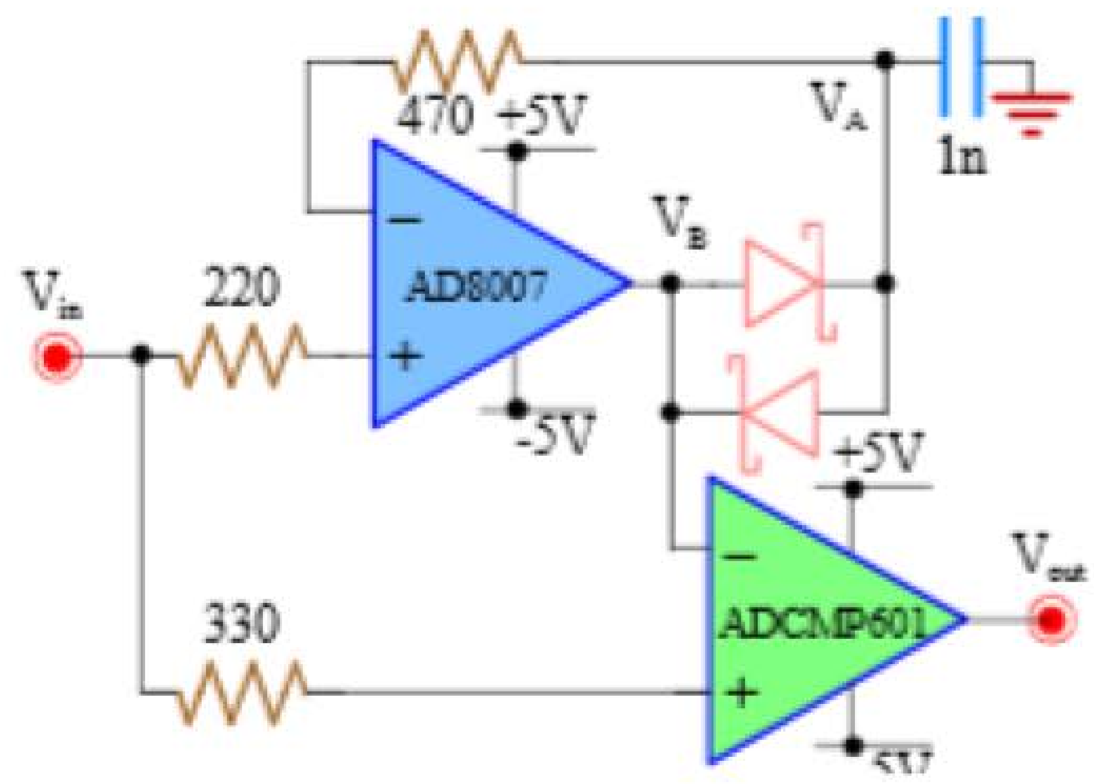
$$I_L = \frac{V_X}{1k} = \frac{i_2/g_m}{1k} = \frac{I_B^+/g_m}{1k} = 1\,nA$$

(error current on the load)

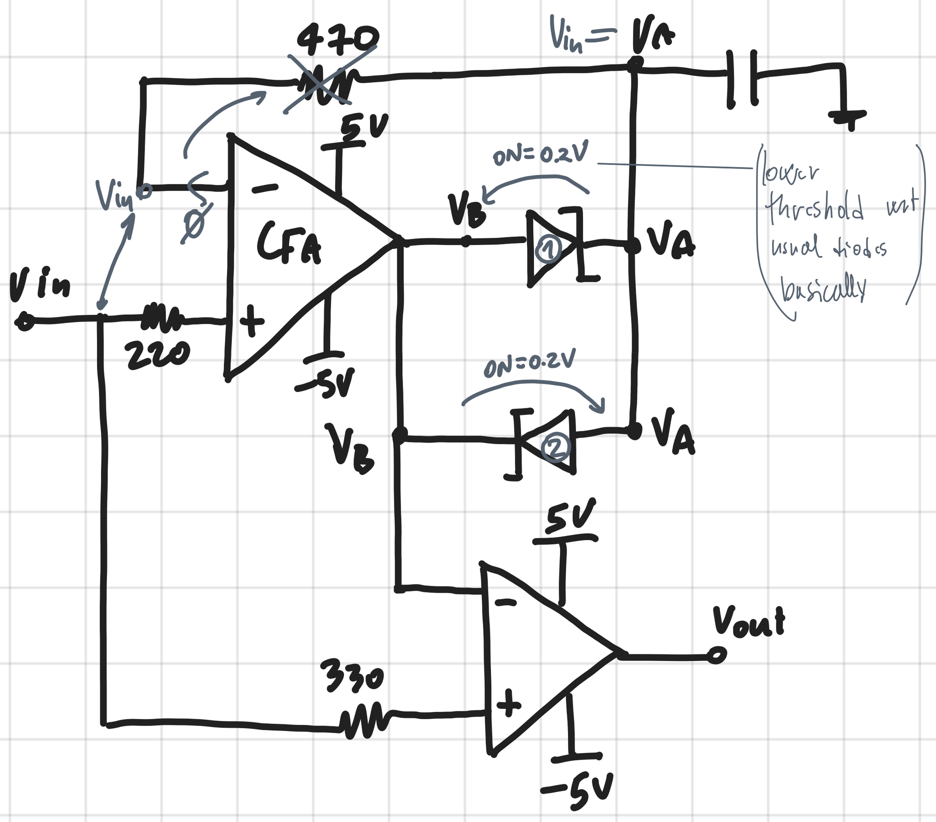
4

Ex. 4

The circuit employs a comparator, a CFA amplifier and two Schottky diodes. The Vin input is sinusoidal with 3V peak amplitude.
a) Plot the VA, VB and Vout waveforms and describe the function of the circuit.



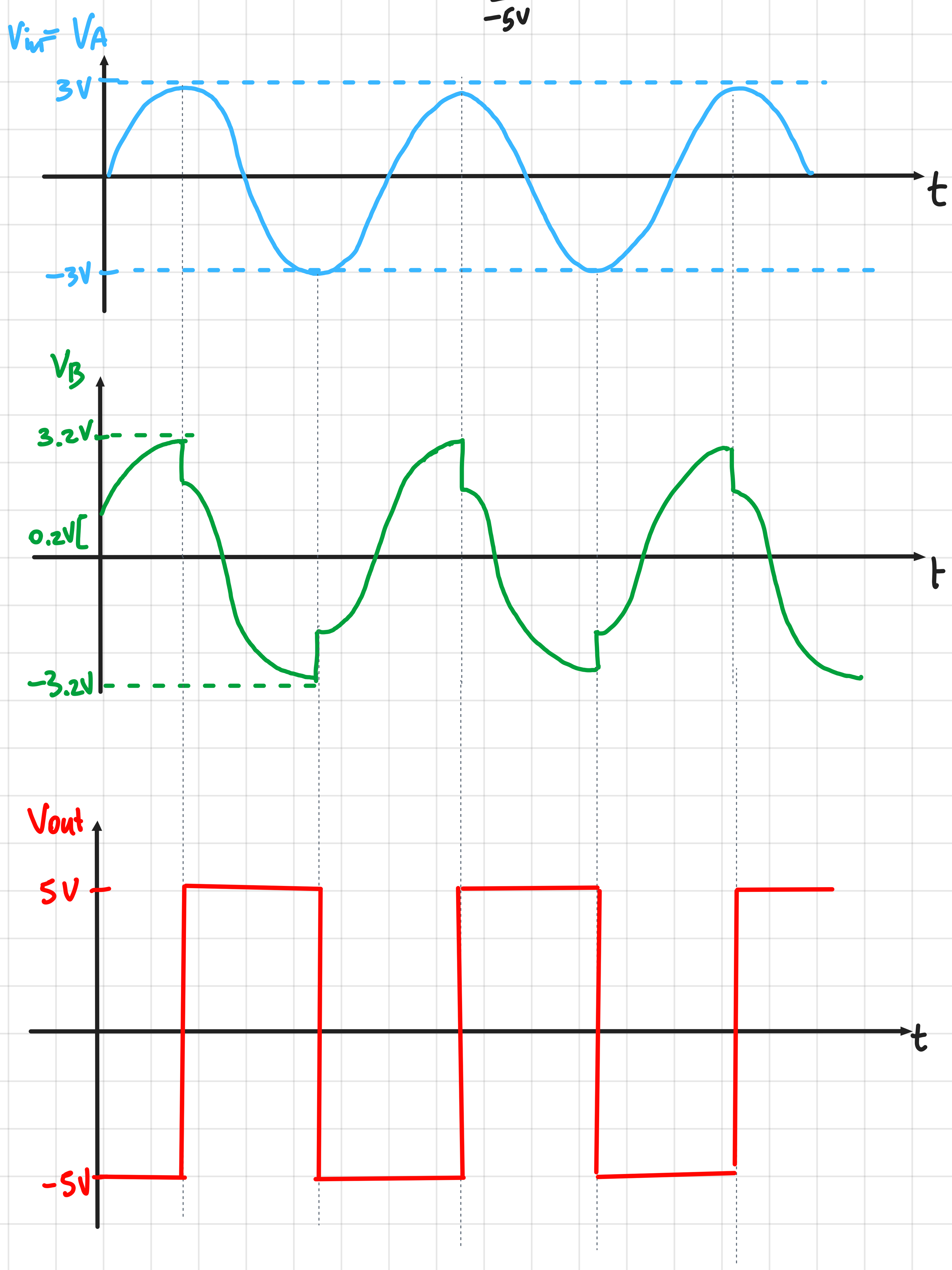
a)



Vin sine $3V_{peak}$

$V_A = V_{in}$

- If $V_{in} \uparrow \Rightarrow V_A \uparrow$ (Shottky ① is ON) $\Rightarrow V_B = V_A + 0.2V$
- If $V_{in} \downarrow \Rightarrow V_A \downarrow$ (Shottky ② is ON) $\rightarrow V_B = V_A - 0.2V$



→ every time the input Vin reaches a peak the comparator switches

so also acts like a PEAK DETECTOR circuit

24/11/2022

E03 (Beretta)

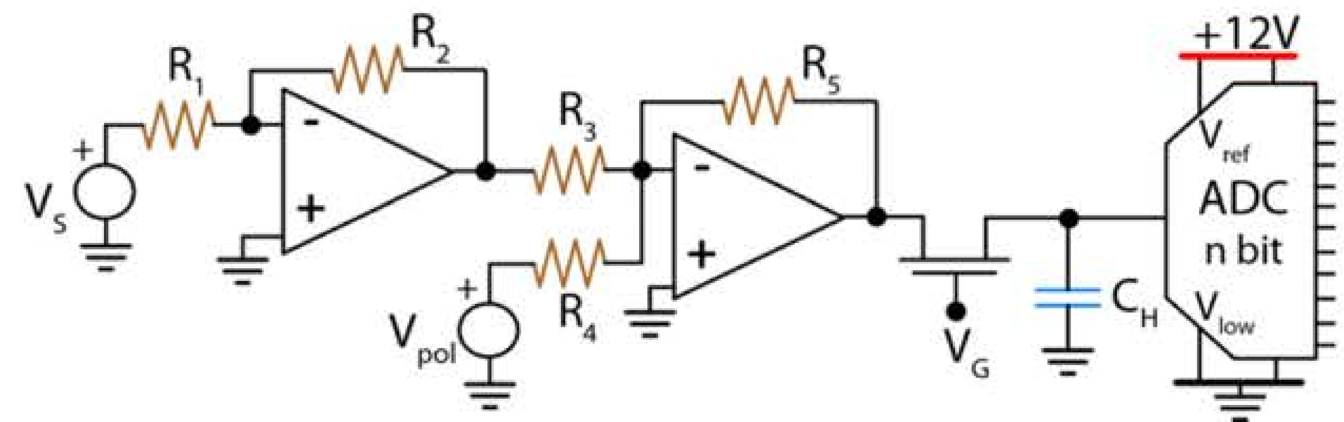
(1)

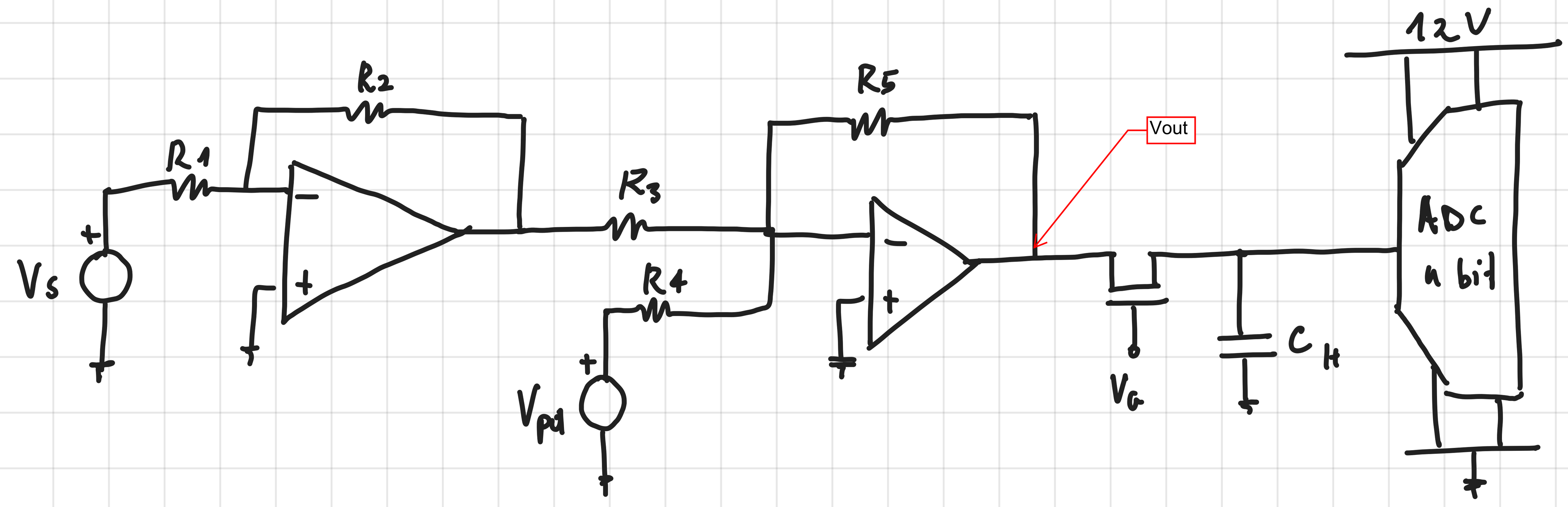
Ex. 1

Input signal from -15mV to +25mV with a 5kHz bandwidth. Required V_S input resolution of 10μV. ADC with T_{CONV}=90μs. R_1=4.7kΩ, R_3=3.3kΩ, R_4=15kΩ, R_5=47kΩ, C_H=100nF.

a) Size R_2, V_{POL} and n_{bit} to fully exploit the ADC input range.

b) Select R_{ON} to provide <1/2LSB error during sampling at Shannon limit.



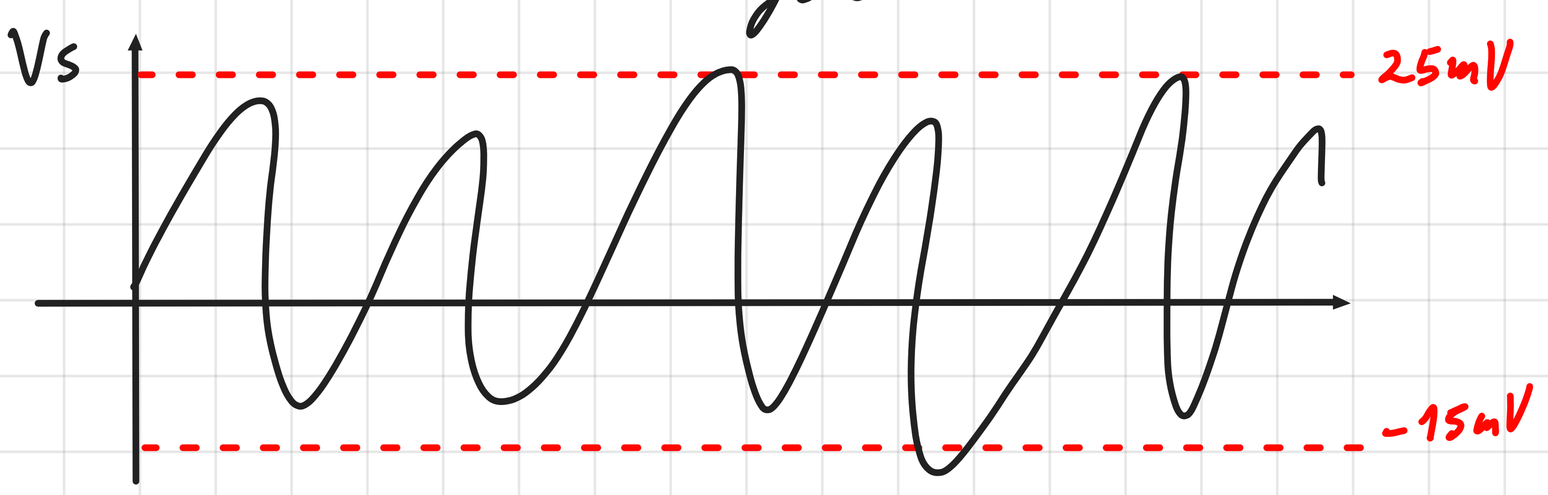


a) $R_2 = ?$ $\quad V_{pol} = ?$ $\quad n_{bit} = ?$ $\longrightarrow$ to exploit the full range of the ADC

→ from superimposition of effects:

$$V_{out} = V_S\left(-\frac{R_2}{R_1}\right)\left(-\frac{R_5}{R_3}\right) + V_{pol}\left(-\frac{R_5}{R_4}\right)$$

From data we know the range of Vs:



so:

- for $V_S|_{MAX}$ $\longrightarrow$ $V_{out} = 25mV\left(\frac{R_2}{R_1}\right)\left(\frac{R_5}{R_3}\right) - V_{pol}\left(\frac{R_5}{R_4}\right) = 12V$ ← MAX output of ADC
- for $V_S|_{MIN}$ $\longrightarrow$ $V_{out} = -15mV\left(\frac{R_2}{R_1}\right)\left(\frac{R_5}{R_3}\right) - V_{pol}\left(\frac{R_5}{R_4}\right) = 0V$ ← MIN output of ADC

ADC RANGE

$$+40mV\left(\frac{R_2}{R_1}\right)\left(\frac{R_5}{R_3}\right) = 12V \longrightarrow R_2 = \frac{12V}{40mV}\frac{R_3}{R_5}R_1 = 99k\Omega$$

$$V_{pol} = -15mV\left(\frac{R_2}{R_1}\right)\left(\frac{R_5}{R_3}\right)\frac{R_4}{R_5} = -1.44V$$

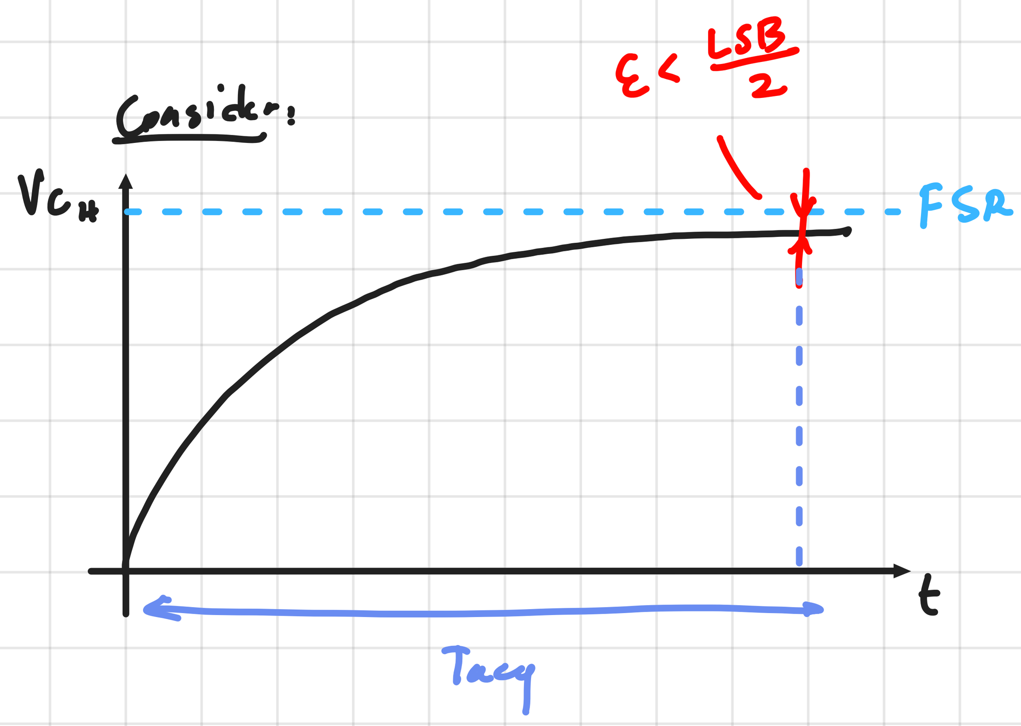
↳ we know that: $\quad LSB_{in} = 10\mu V \longrightarrow LSB_{out} = LSB_{in}\left(\frac{R_2}{R_1}\right)\left(\frac{R_5}{R_3}\right) = 3mV$

↳ $LSB_{out} = \frac{FSR}{2^{n\,bit}} \longrightarrow n_{bit} = \log_2\left(\frac{FSR}{LSB_{out}}\right) = 12\text{ bit}$

b) R_{ON} ? | $\varepsilon_{sampling} < \frac{LSB}{2}$ @ $f_{sampling} = 2f_{max} = 10kHz$ (Shannon limit)

$$T_{sampling} = \frac{1}{f_{sampling}} = 100\mu s \longrightarrow \underbrace{T_{sampling}}_{100\mu s} = \underbrace{T_{CONV}}_{90\mu s} + T_{acq} \longrightarrow T_{acq} = 10\mu s$$

Consider:



↳ $\varepsilon = FSR - FSR\left(1 - e^{-\frac{T_{acq}}{\tau}}\right) < \frac{LSB}{2} \longrightarrow FSR\, e^{-\frac{T_{acq}}{\tau}} < \frac{LSB}{2}$, with $\frac{LSB}{2} = \frac{FSR}{2^{n\,bit}}$

$\tau = R_{ON}C_H$

↳ $\frac{T_{acq}}{\tau} > \ln\left(2 \cdot 2^{n\,bit}\right) \longrightarrow R_{ON} < \frac{T_{acq}}{C_H \ln(2^{13})} = 11{,}11\,\Omega \longrightarrow$ e.g. $R_{ON} = 10\,\Omega$

2

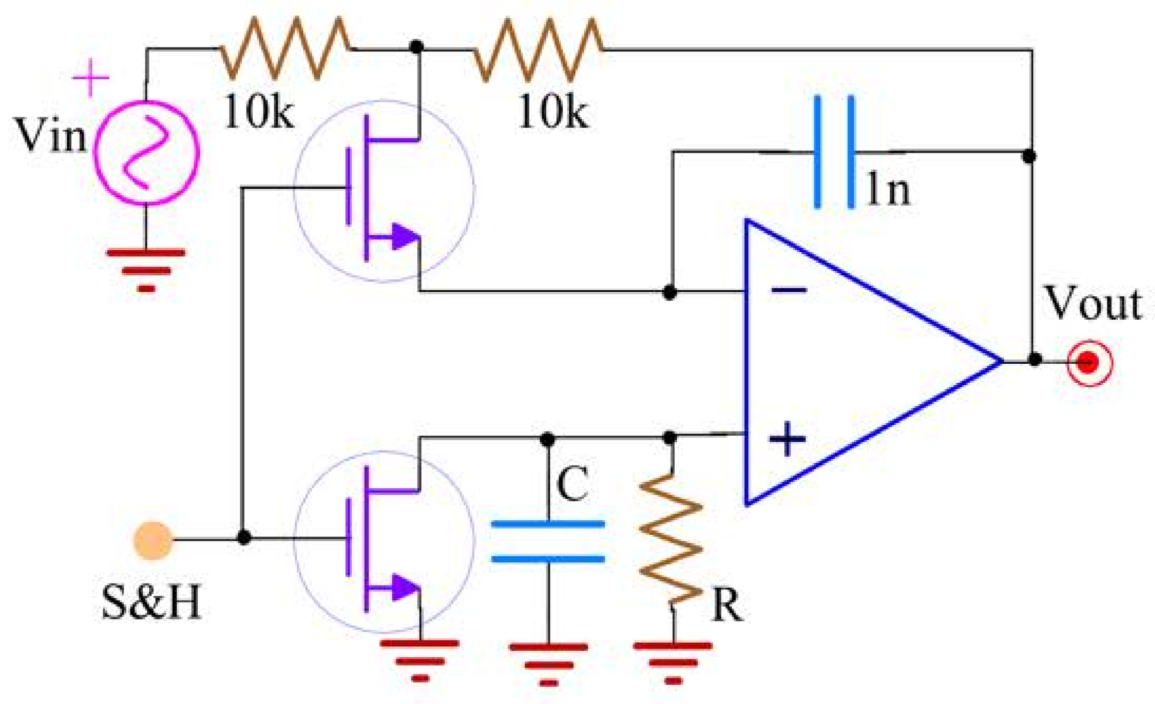
Ex. 2

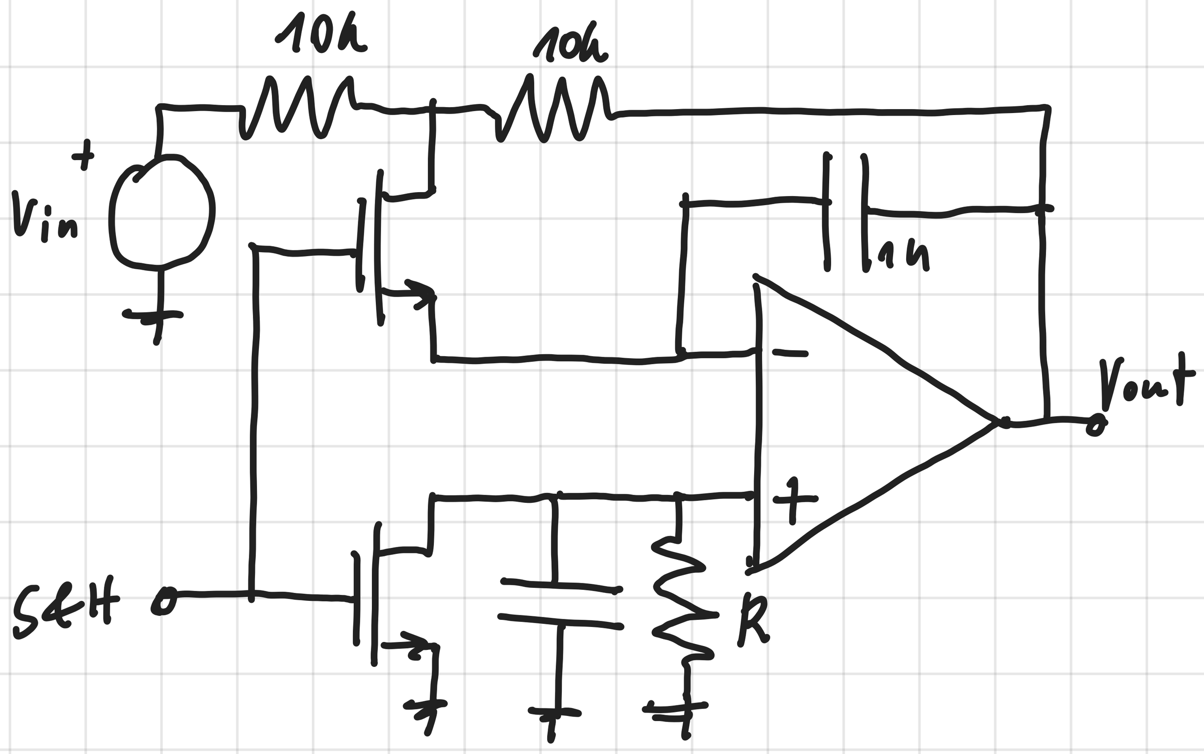
Uncompensated OpAmp with A_0=100dB, f_{high}=5MHz, A_{min}=20dB and I_B=200nA (inward going).

a) Compute the acquisition time for a 12 bit ADC.

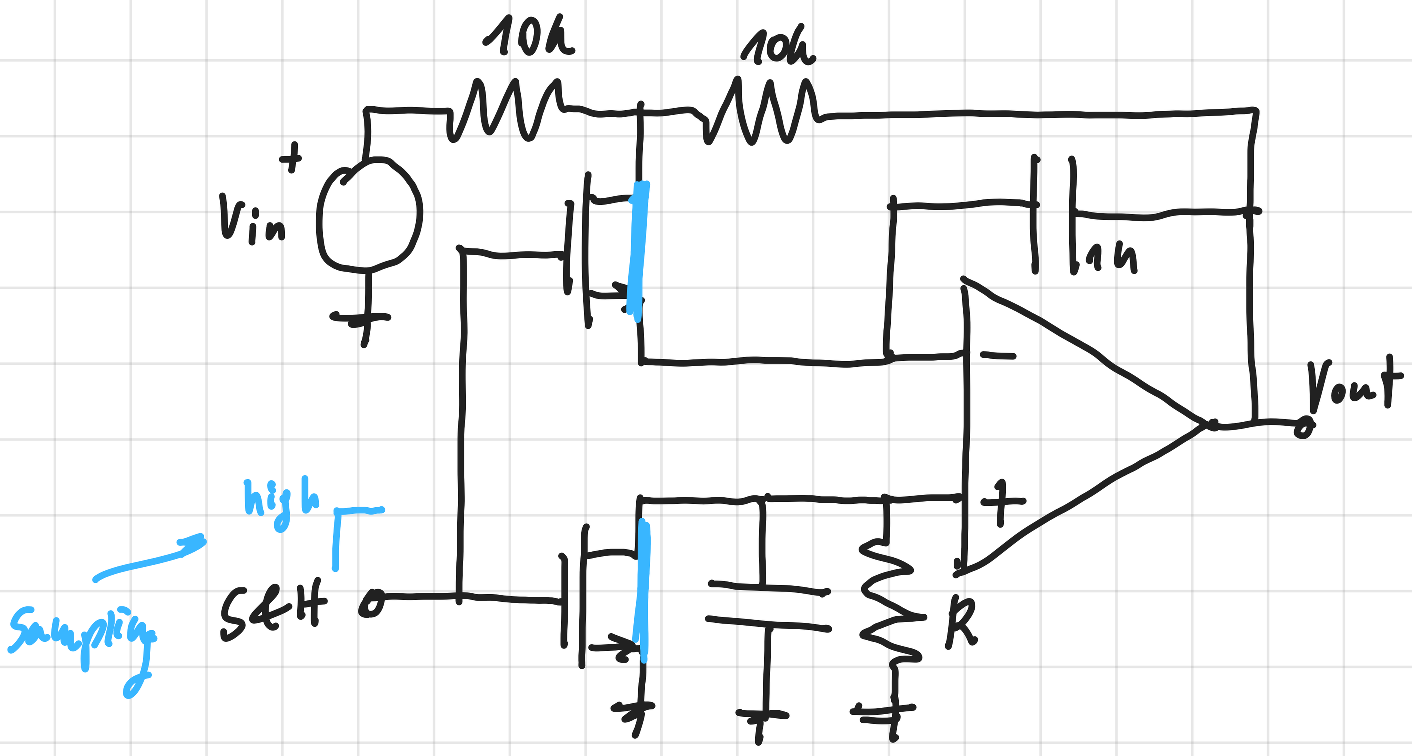
b) Consider V_{in}=+100mV, C=1nF and R=100kΩ, the plot the $V_{out}(t)$ waveform during the Hold phase, lasting 1ms.

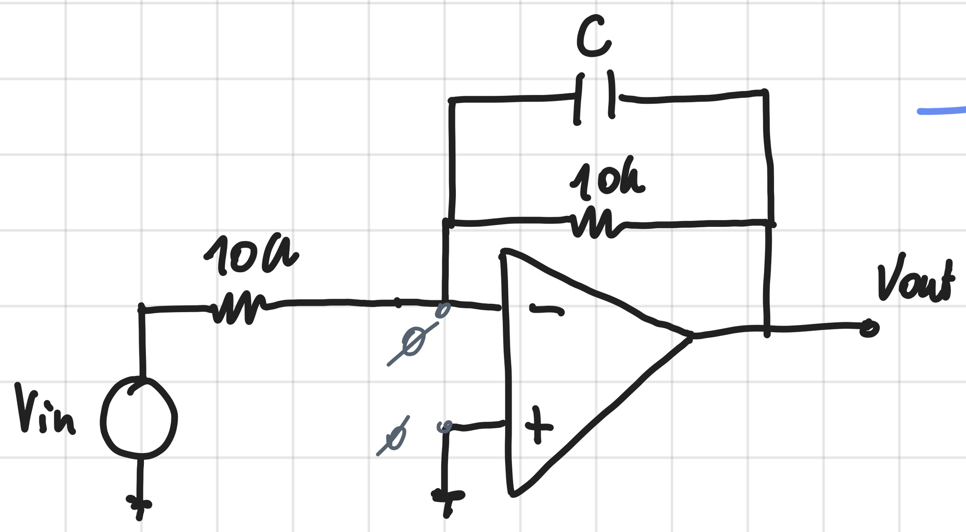
c) Properly modify and size the RC network in order to **compensate charge injection** and **bias currents.**





a) T_{acq} = ? (12 bit ADC)

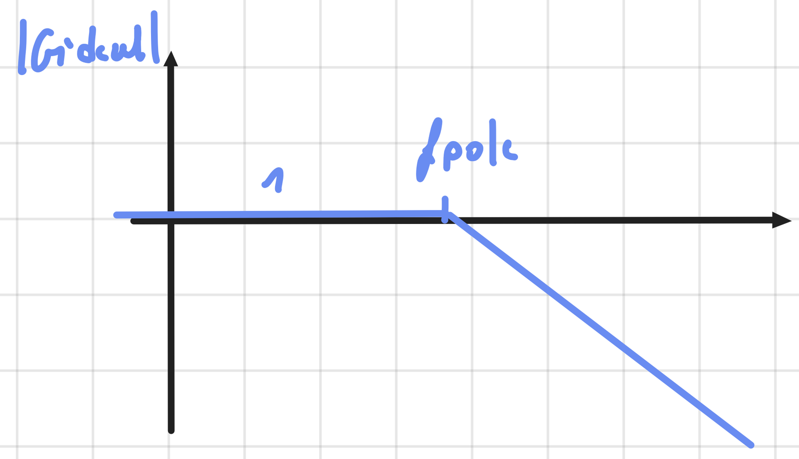




DC $G_{id} = -1$

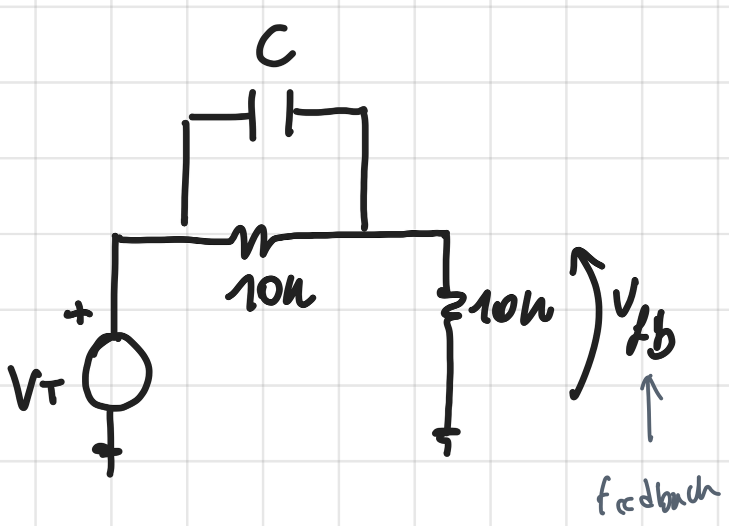
AC $G_{id} = 0$

pole $f_{pole} = \frac{1}{2\pi C\, 10k} = 15.9\,kHz$



→ Let's now study the real gain, consider:

$\beta(s)$

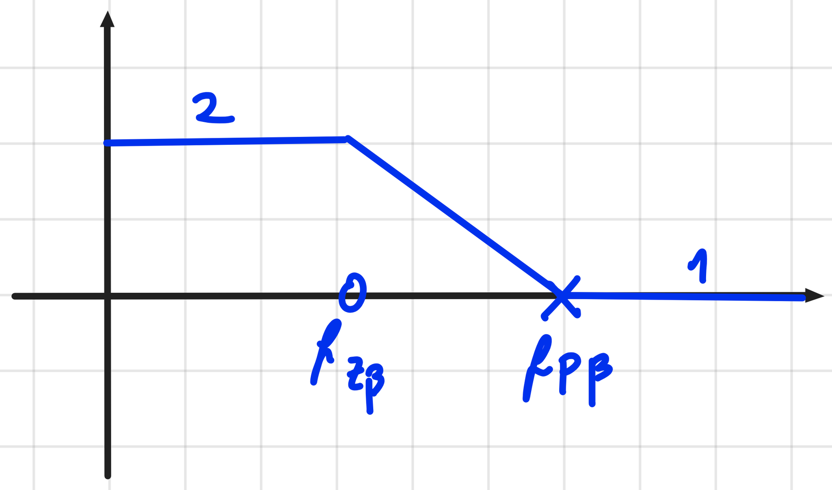


→ DC $\beta(s)|_{DC} = \frac{V_{fb}}{V_T} = \frac{10k}{10k + 10k} = \frac{1}{2}$

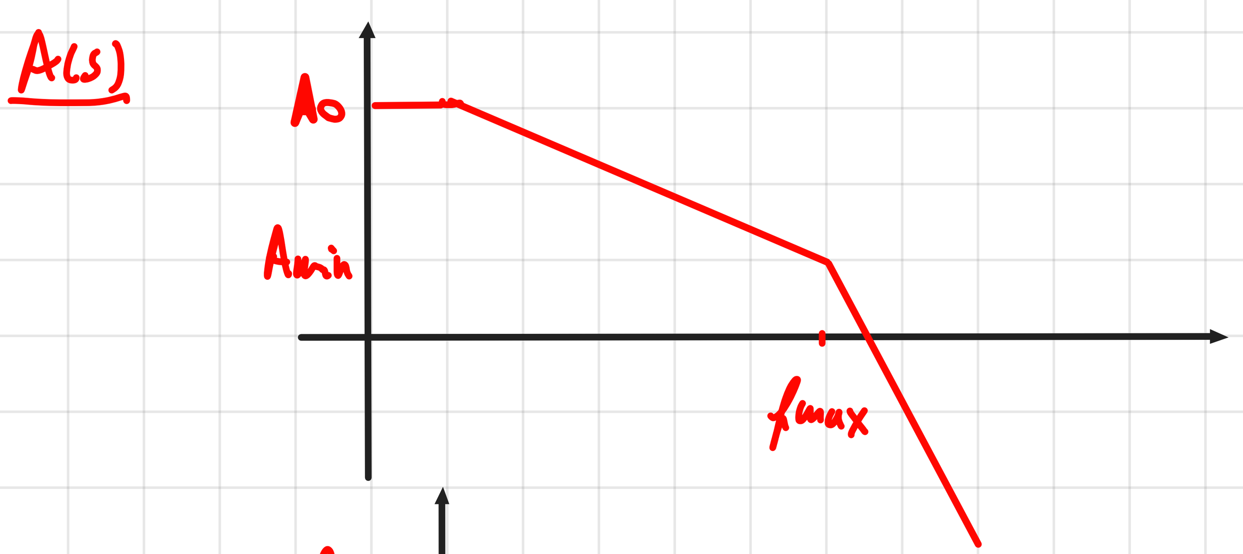
AC $\beta(s)|_{AC} = 1$

pole $f_{p\beta} = \frac{1}{2\pi C\,(10k\Omega // 10k\Omega)} = 31.8\,kHz$

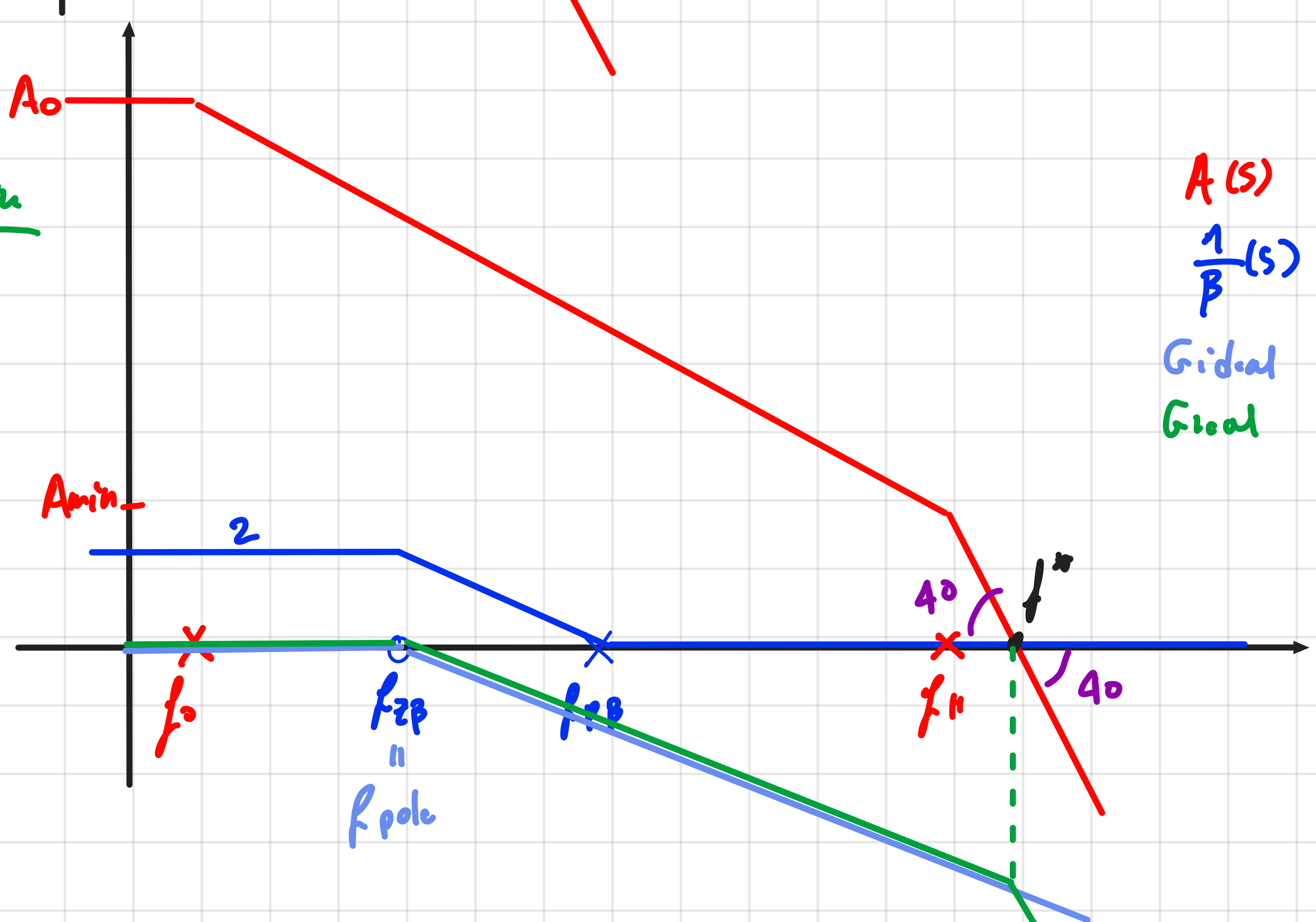
zero $f_{z\beta} = \frac{1}{2\pi C\, 10k\Omega} = 15.9\,kHz$



$A(s)$



→ Real gain



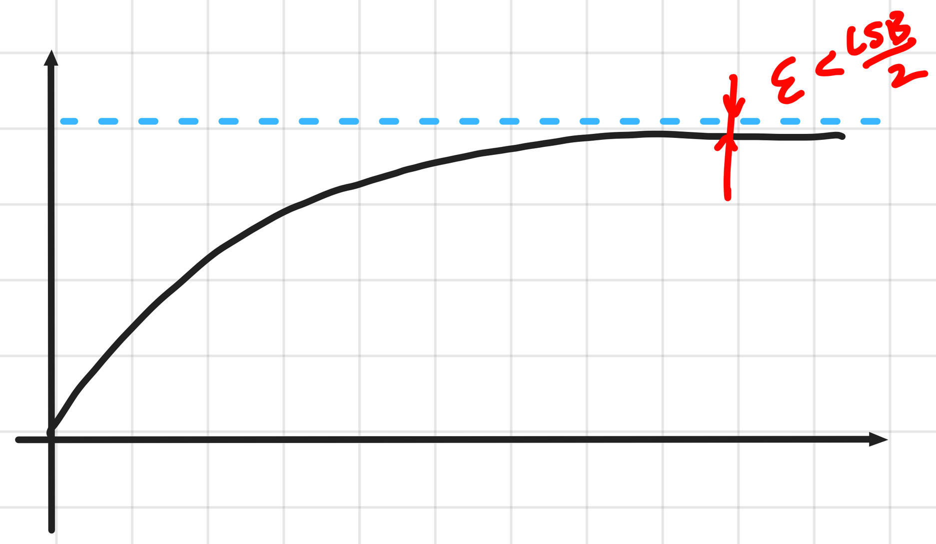
→ closure angle: 40 - 40 (UNSTABLE)

→ $f^* = \sqrt{A_{min} f_H} = 15.8\,MHz$

→ PHASE MARGIN:

$\phi_m = 180° - \arctan\left(\frac{f^*}{f_0}\right) + \arctan\left(\frac{f^*}{f_{z\beta}}\right) - \arctan\left(\frac{f^*}{f_{p\beta}}\right) - \arctan\left(\frac{f^*}{f_H}\right) = 17.56°$

So, now we consider the error:



$$\varepsilon = FSR\, e^{-\frac{T_{acq}}{\tau}} < \frac{LSB}{2}$$

$$T_{eq} = \tau \ln\left(\frac{\Delta V_{H\,max}}{\varepsilon_H}\right)$$

$$\frac{\Delta V_{H\,max}}{\varepsilon_H} = \frac{FSR}{\frac{LSB}{2}} = \frac{\cancel{FSR}}{\frac{\cancel{FSR}}{2^{nbit}}\cdot 2} = 2^{13}$$

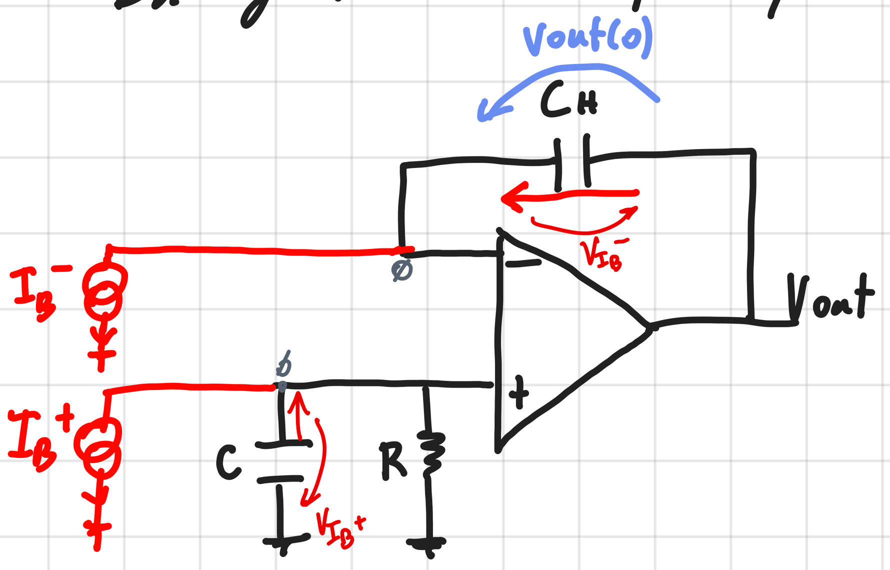
$\hookrightarrow \tau = \frac{1}{2\pi f_{pole}} = 10\,\mu s$

$f_{pole} = 15.9\,kHz$

$\Longrightarrow T_{acq} = 90.1\,\mu s$

b) $V_{in} = 100\,mV$ $\quad C = 1\,nF$ $\quad R = 100\,k\Omega$ $\longrightarrow V_{out_{HOLD}}(t) = ?$

During the HOLD phase, the circuit:



$\rightarrow V_{out}(0) = -100\,mV$

$\hookrightarrow$ now let's consider the effect of the bias currents:

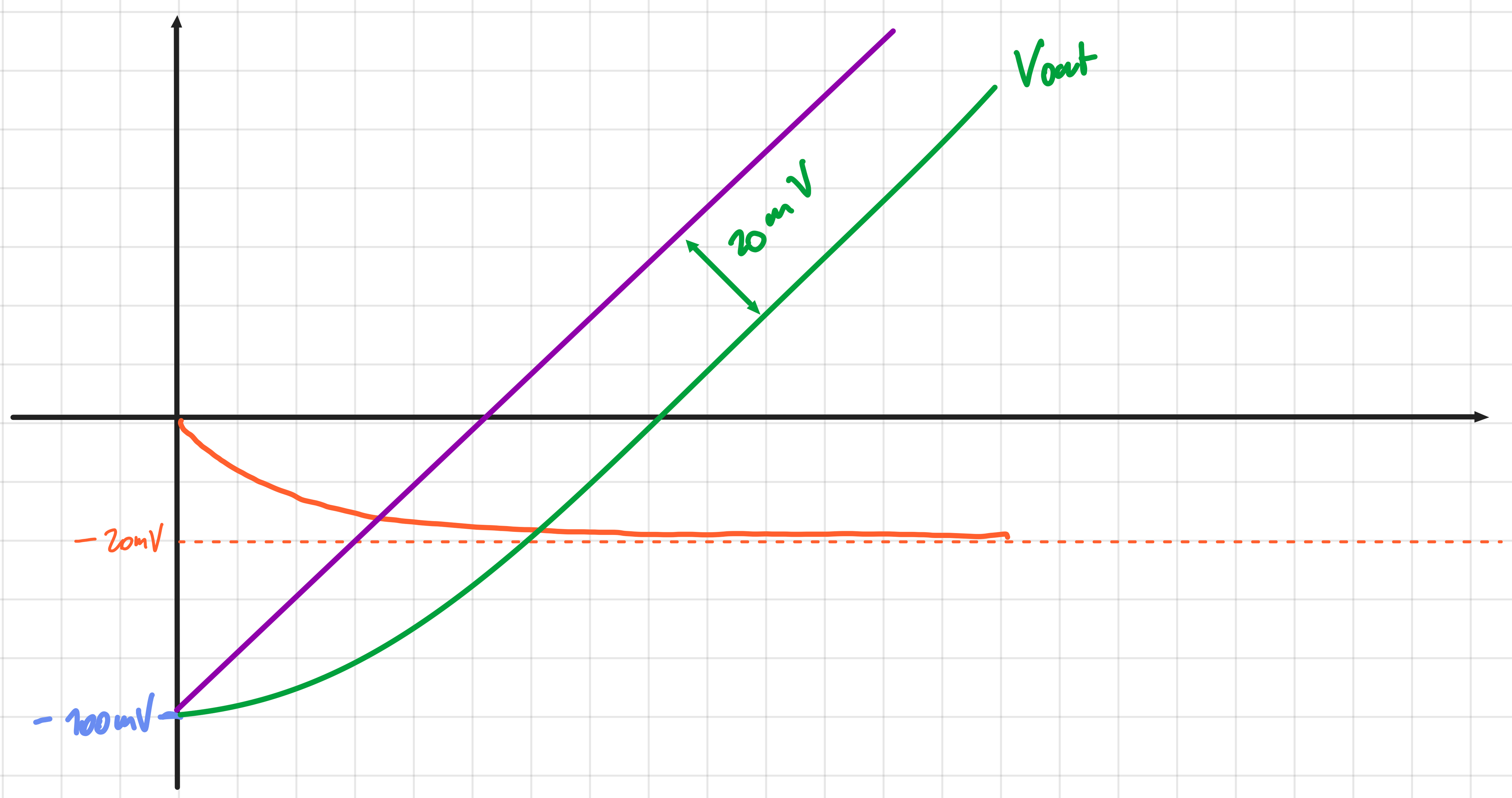
I_B^-: $\rightarrow$ will have a voltage drop $(V_{I_B^-})$ due to the current I_B^- going through C_H:

$$\frac{dV_{out}}{dt} = \frac{I_B}{C_H} = 200\,\frac{V}{s}$$

I_B^+: $\rightarrow$ we'll have a voltage drop $(V_{I_B^+})$ on C:

$$\hookrightarrow V^+ = \underbrace{I_B^+ R}_{20\,mV}\left(e^{-\frac{t}{\tau}} - 1\right)$$

$$\hookrightarrow V_{out}(t) = V_{out}(0) + \frac{dV_{out}}{dt}\cdot t + 20\,mV\left(e^{-\frac{t}{\tau}} - 1\right)$$

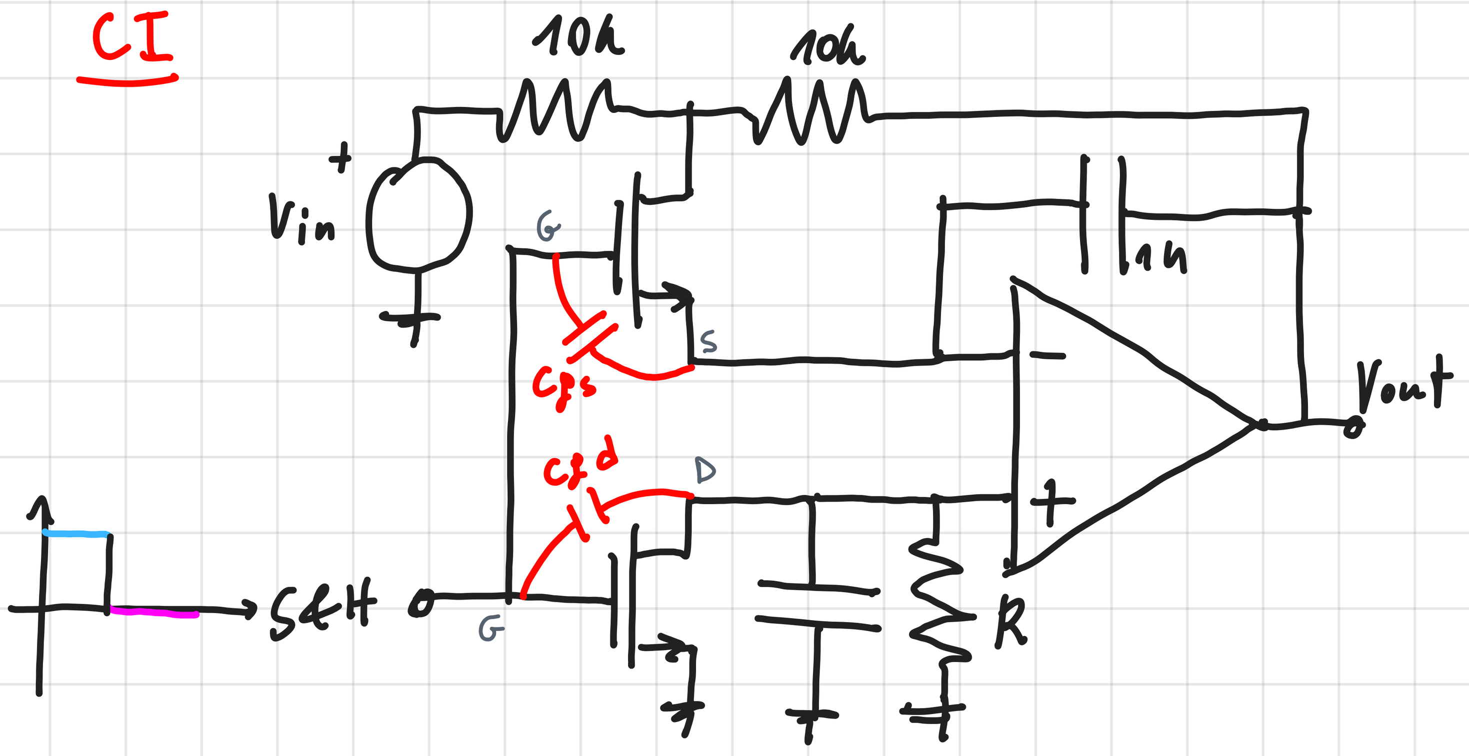


$\rightarrow$ then for $t = t_{HOLD} = 1\,ms$

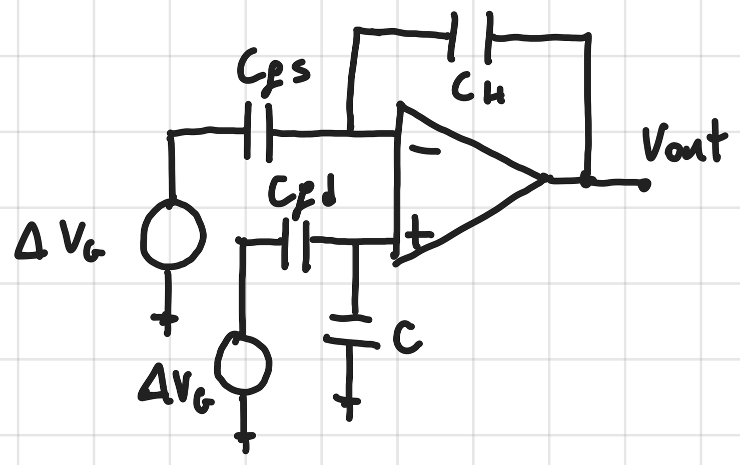
we can exactly compute $V_{out}(1\,ms)$

c) $R = ?$ $\quad C = ?$ | compensate charge injection (CI) & bias current (I_B)

CI



$\rightarrow$ we can simplify the circuit to consider this effect:



error coming from CI:

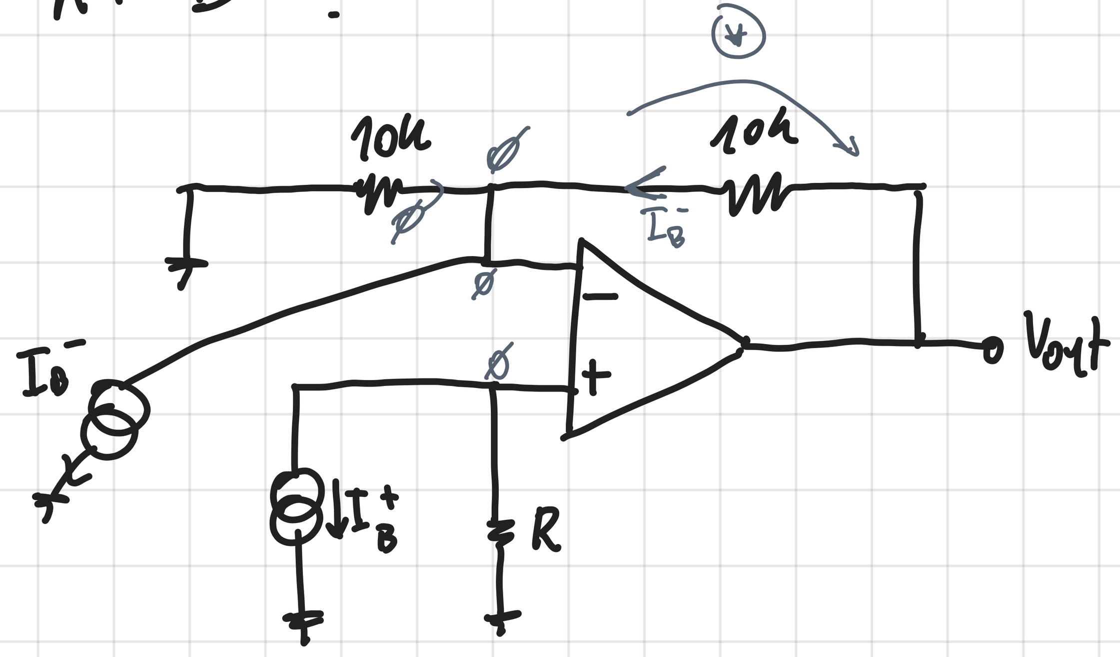
$$\varepsilon_{CI} = -\Delta V_G \frac{C_{gs}}{C_H} + \Delta V_G \frac{C_{gd}}{C_{gd}+C}\left(1 + \frac{C_{gs}}{C_H}\right)$$

$\hookrightarrow$ now let's consider $C_{gs} \simeq C_{gd}$ (Hp.) so this expression simplifies: (and $C = C_H$)

$$\varepsilon_{CI} = -\Delta V_G \frac{C_{gs}}{C_H} + \Delta V_G \frac{C_{gd}}{\cancel{C_{gd}+C}}\left(\frac{\cancel{C_H + C_{gs}}}{C_H}\right) = -\Delta V_G \frac{C_{gs}}{C_H} + \Delta V_G \frac{C_{gd}}{C_H} = 0$$

compensated ✓ if $C_{gd} = C_{gs}$ + $C = C_H$

I_B At DC:



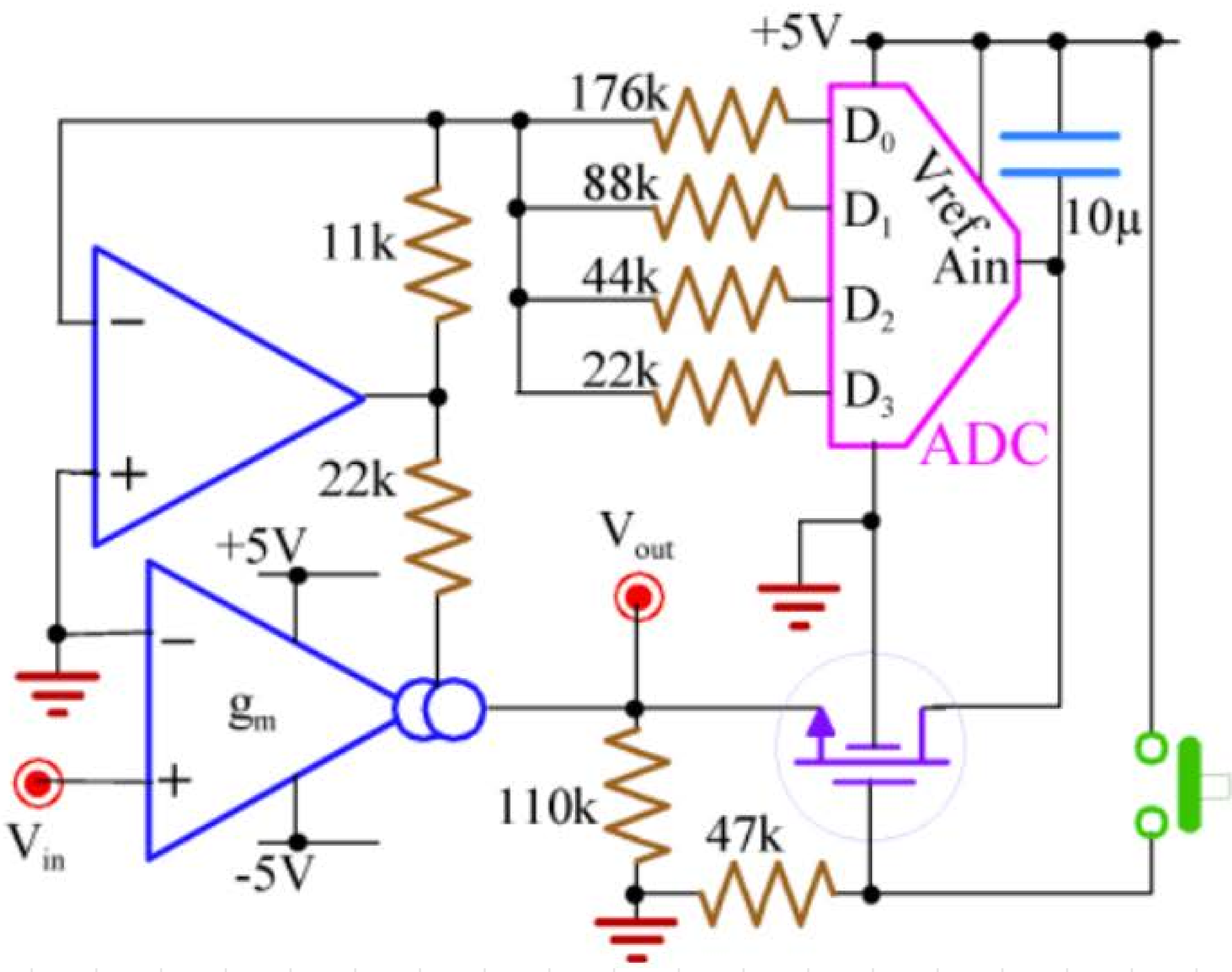
I_B^+ → no contribution on the out.

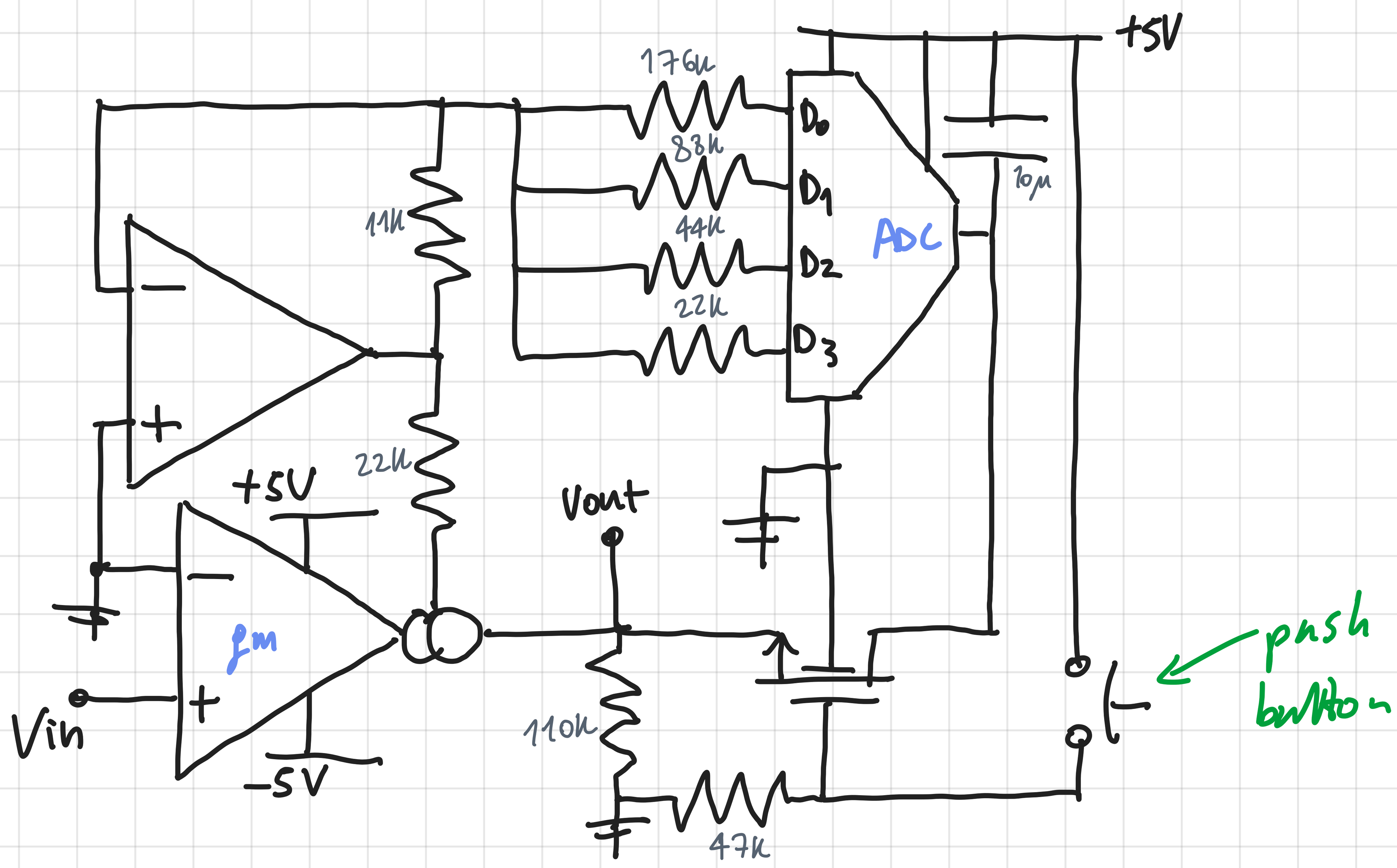
I_B^- → $\varepsilon = I_B^- \, 10k\Omega$

$$\varepsilon = I_B^- \, 10k\Omega - I_B^+ R \underbrace{\left(1 + \frac{10k}{10k}\right)}_{2} \longrightarrow \text{for } \varepsilon = 0 \Longrightarrow R = 5\ k\Omega$$

③ **Ex. 3**

4bit flash ADC. OpAmps with GBWP=100MHz. OTA with control pin (not output pin!) at -5V.
a) Compute the Vout/Vin relationship at DC, as a function of the Dout digital ADC code, when the pushbutton is off.
b) Describe what happens at each very short pulse applied to the pushbutton.
c) In case the pushbutton is kept pressed for long time, compute the Vout/Vin relationship at DC.

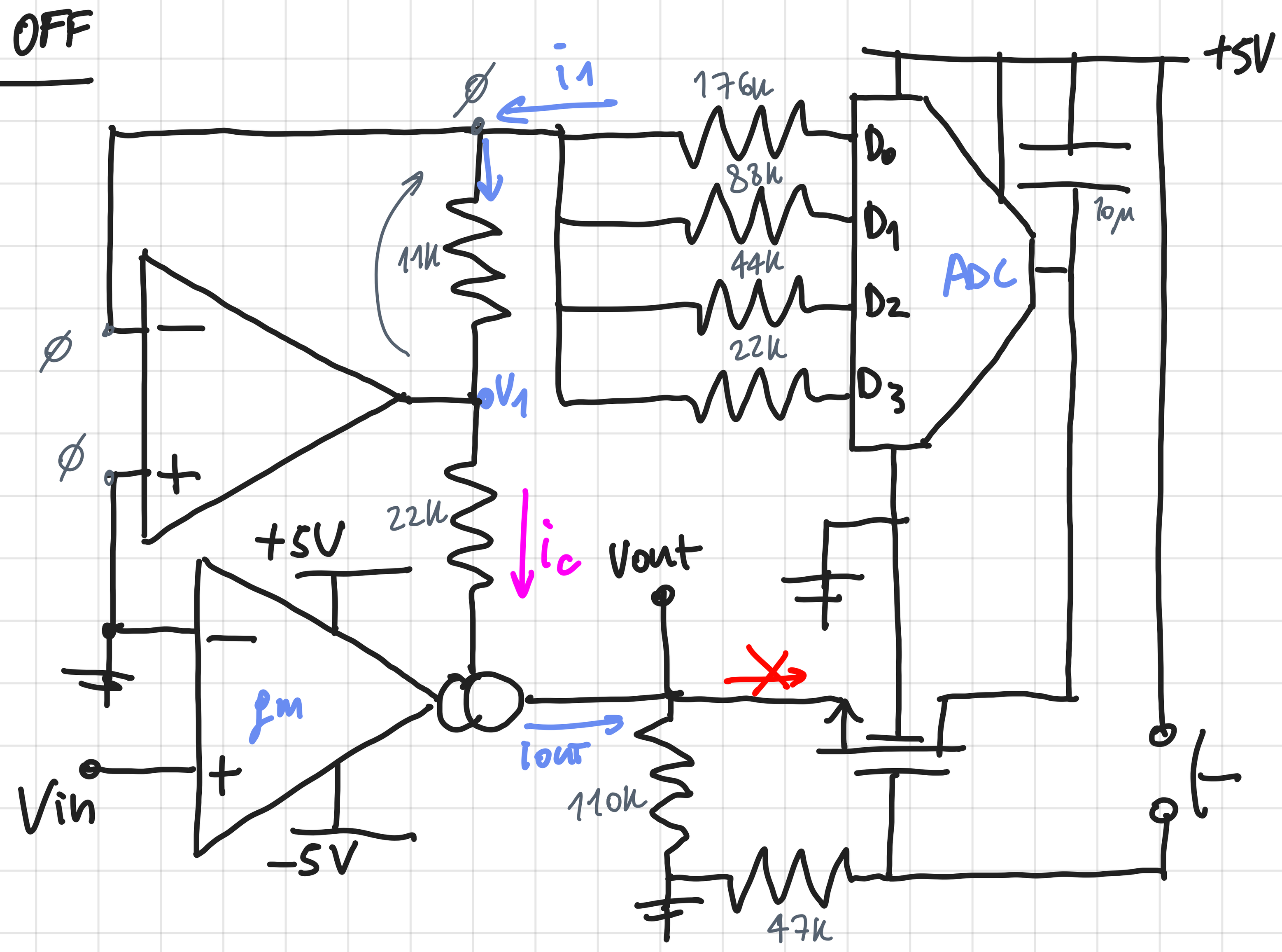




a)

Vout / Vin ?

- PUSH BUTTON OFF



- $V_{out} = 110k\Omega \cdot i_{OUT}$
- $i_{OUT} = V_{in} \cdot g_m$
- $V_1 = -i_1 \, 11k\Omega$
- $i_1 = \left(\frac{D_0}{176k} + \frac{D_1}{88k} + \frac{D_2}{44k} + \frac{D_3}{22k}\right) 5V$

from the ADC

the digital word can be written as:

$$D_{out} = D_0 \, 2^0 + D_1 \, 2^1 + D_2 \, 2^2 + D_3 \, 2^3$$

$$i_1 = \frac{1}{176k\Omega}\left(D_0 + D_1 \cdot 2 + D_2 \cdot 4 + D_3 \cdot 8\right) 5V$$

$$i_1 = \frac{D_{out}}{176k\Omega} 5V \implies V_1 = -\frac{D_{out} \, 5V}{176k\Omega} \cdot 11k\Omega$$

↳ control current: $i_c = \frac{V_1 - (-5V)}{22k\Omega}$

$$\hookrightarrow g_m = \frac{i_c}{V_{TH}} = \frac{-\frac{D_{out} \, 5V}{176k\Omega} \cdot 11k\Omega + 5V}{22k\Omega \quad V_{TH}} = g_m \overset{\text{Siemens}}{S}\left(1 - \frac{D_{out}}{16}\right)$$

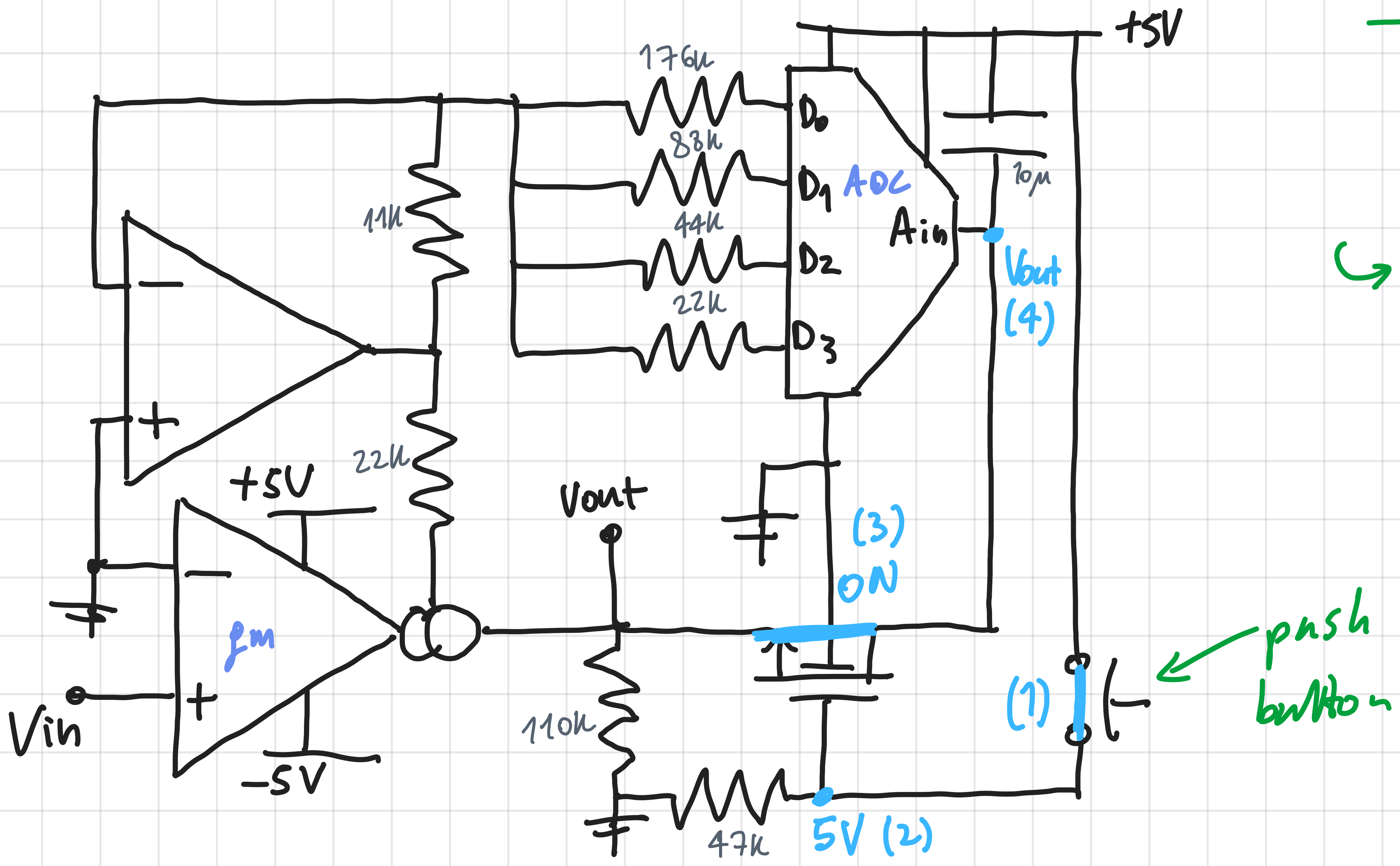
↳ $i_{OUT} = V_{in}\, g_m$

$$V_{out} = 110k\Omega\, g_m V_{in} = V_{in}\; 9mS\left(1 - \frac{D_{out}}{16}\right) 110k\Omega$$

$$\Rightarrow \frac{V_{out}}{V_{in}} = 1000\left(1 - \frac{D_{out}}{2^4}\right)$$

so the gain also depends on the ADC output digital word

b)



→ What happens if we press for a short amount of time the push-button?

↳ By pressing the button

(4): ADC will convert Vout voltage

↳ $A_{in} = V_{out}(0)$

→ We've seen that the gain $\frac{V_{out}}{V_{in}}$ is dependent on the digital output of the ADC

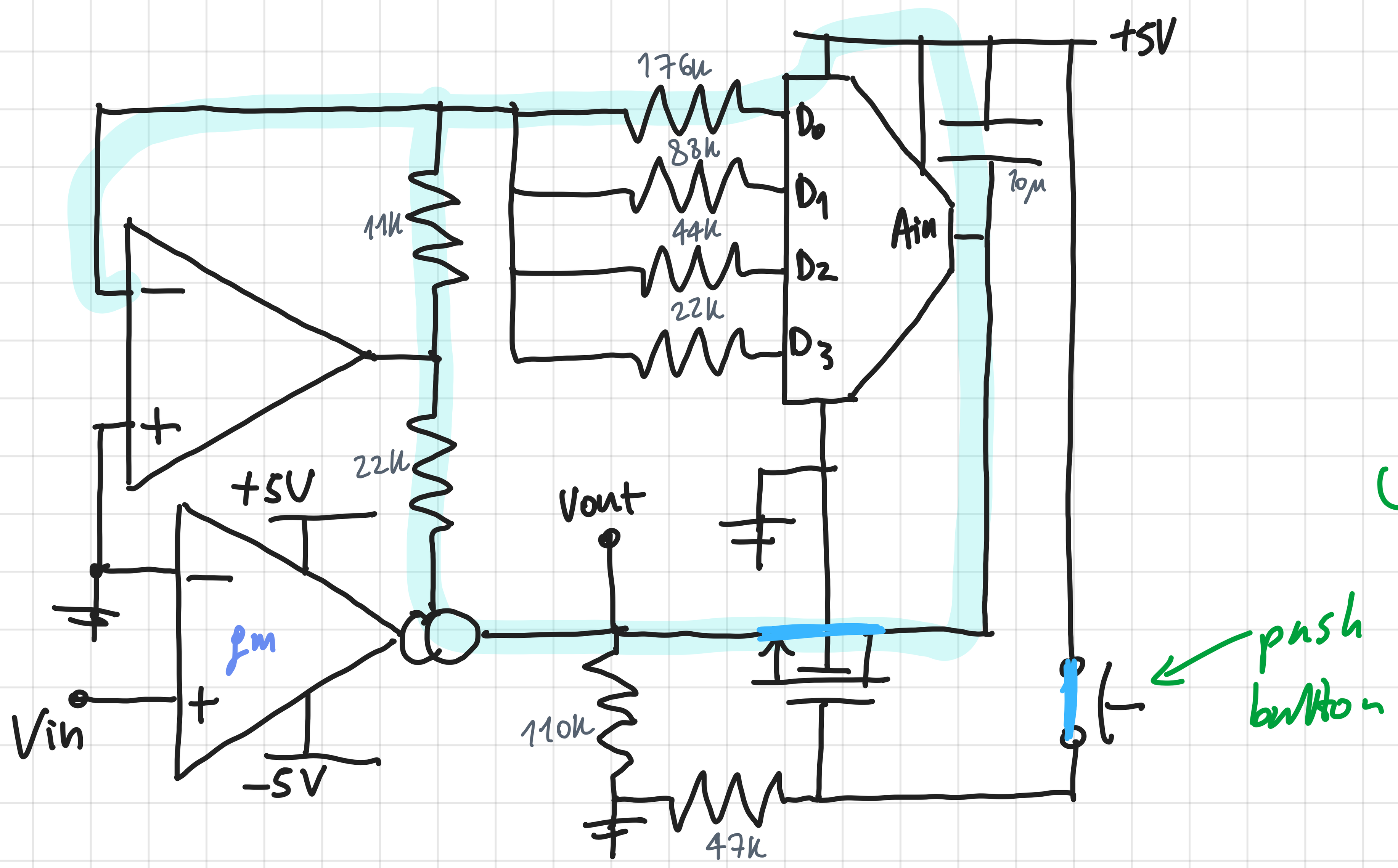
↳ So if we compute the digital output in this case:

$$D_{out} = \frac{A_{in}}{5V} 2^4 = \frac{V_{out}(0)}{5V} 2^4 \longrightarrow V_{out} = V_{in} \cdot 1000\left(1 - \frac{V_{out}(0)}{5V}\right)$$

↳ Vout depends on Vout(0)

⟹ By pressing instantaneously the button we're modifying the T.F. btw in and out

c) Push-button is kept press for a long time ⟹ it's like we're closing the feedback)



PUSH-BUTTON ON ⟹ neg. feedback

(Ain = Vout always, not just for some instant)

$$D_{out} = \frac{A_{in}}{5V} \cdot 2^4$$

↳ $V_{out} = V_{in} \cdot 1000\left(1 - \frac{V_{out}}{5V}\right)$

↳ $V_{out} = V_{in}\, 1000 - V_{out}\, V_{in} \frac{1000}{5}$

T.F. (gain): $V_{out} = \frac{V_{in}\, 1000}{1 + V_{in}\, 200}$

4

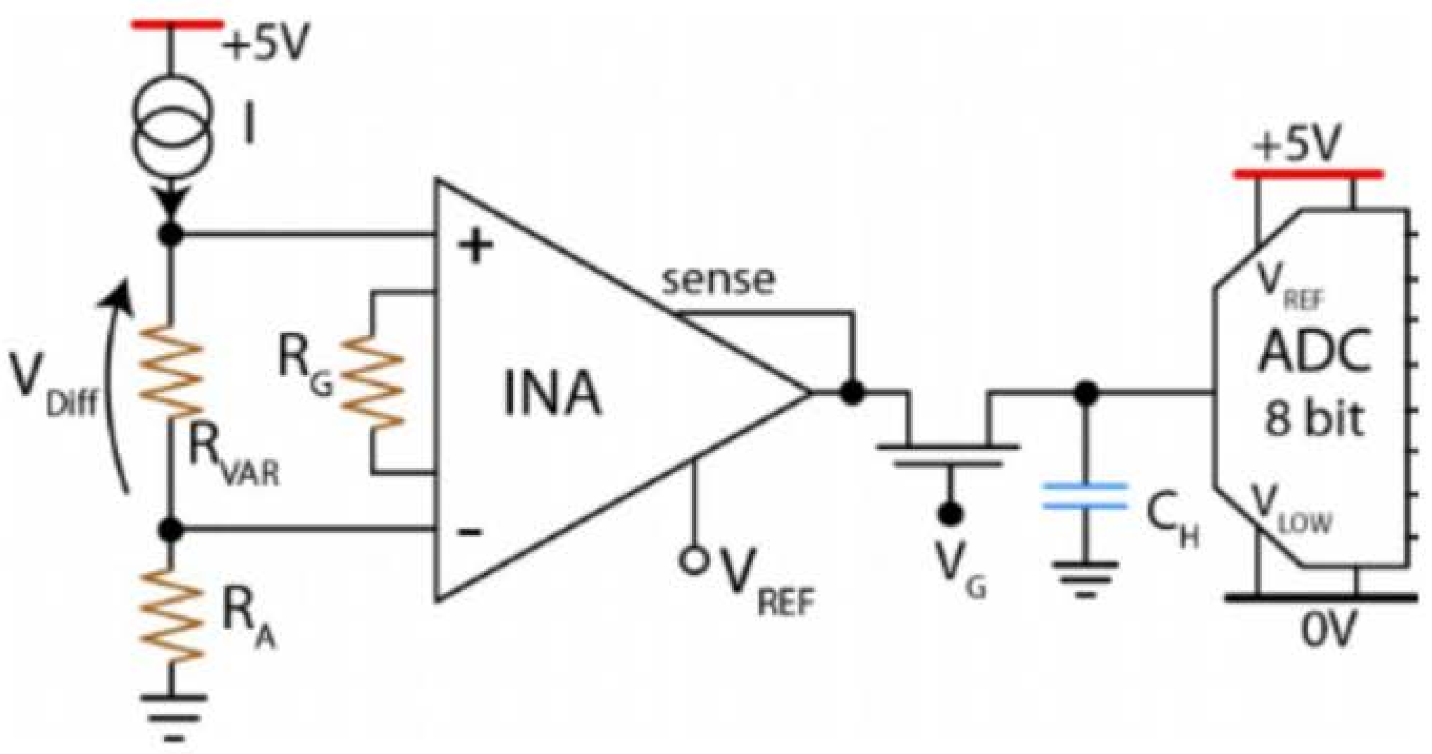
Ex. 4

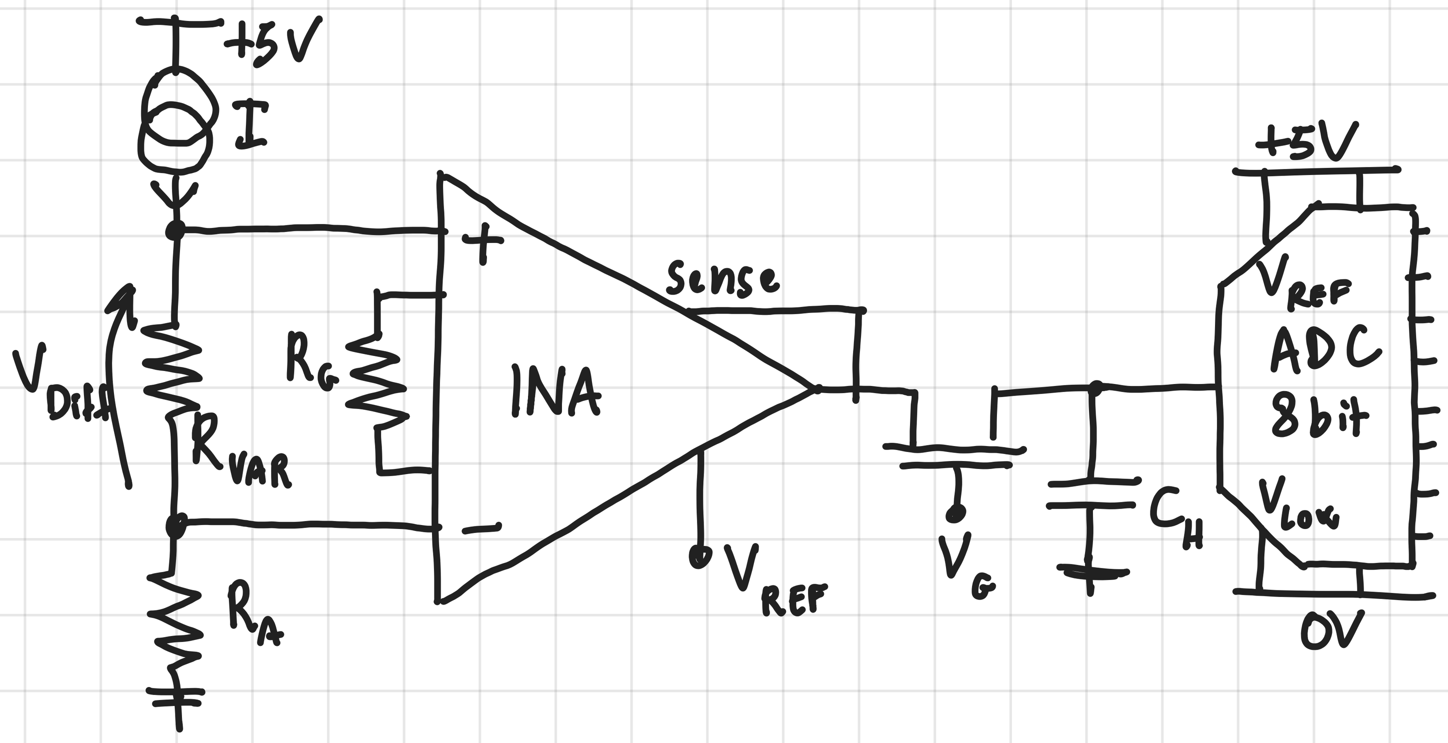
A breath sensor measures the chest extension through an R_{VAR}=10kΩ·(1+α·d), where α=0.02mm^{-1} and d is in the 0-50 mm range. R_A=10kΩ, I=100μA, C_H=10nF. INA's internal resistors are Rf=10kΩ. The SAR ADC has 50nA input leakage.

a) Size R_G and V_{REF} for exploiting the whole ADC's FSR.

b) With V_G swinging between 0V and 10V and an n-MOSFET with V_T=1V and Cgs=100pF, compute aperture charge-induced error range over R_{VAR}.

c) Select Tconv and Tclock to achieve a precision better than ½LSB





$R_{VAR} = 10k(1+\alpha d)$ $\quad \alpha = 0.02\,mm^{-1}$ $\quad d = 0 \div 50mm$

a) $R_G = ?$ $V_{REF} = ?$ | exploits FSR of ADC

$R_{VAR}|_{MIN} = 10k\,(1+0.02\,mm^{-1}\cdot 0) = 10k\Omega$

$R_{VAR}|_{MAX} = 10k\,(1+0.02\,mm^{-1}\cdot 50\,mm) = 20k\Omega$

we can now compute Vdiff min & max

$V_{diff\,min} = R_{VAR}|_{MIN}\, I = 1\,V$

$V_{diff\,max} = R_{VAR}|_{MAX}\, I = 2\,V$

$\Delta V_{diff} = V_{diff_{max}} - V_{diff_{min}} = 1V$

Variations of the INPUT

At the output we'll have a variation:

$\Delta V_{out} = FSR = 5V$

From the INA formulas:

$\Delta V_{out} = \left(1+\frac{2R_f}{R_G}\right)\Delta V_{diff} = 5V \longrightarrow R_G = 5k\Omega$

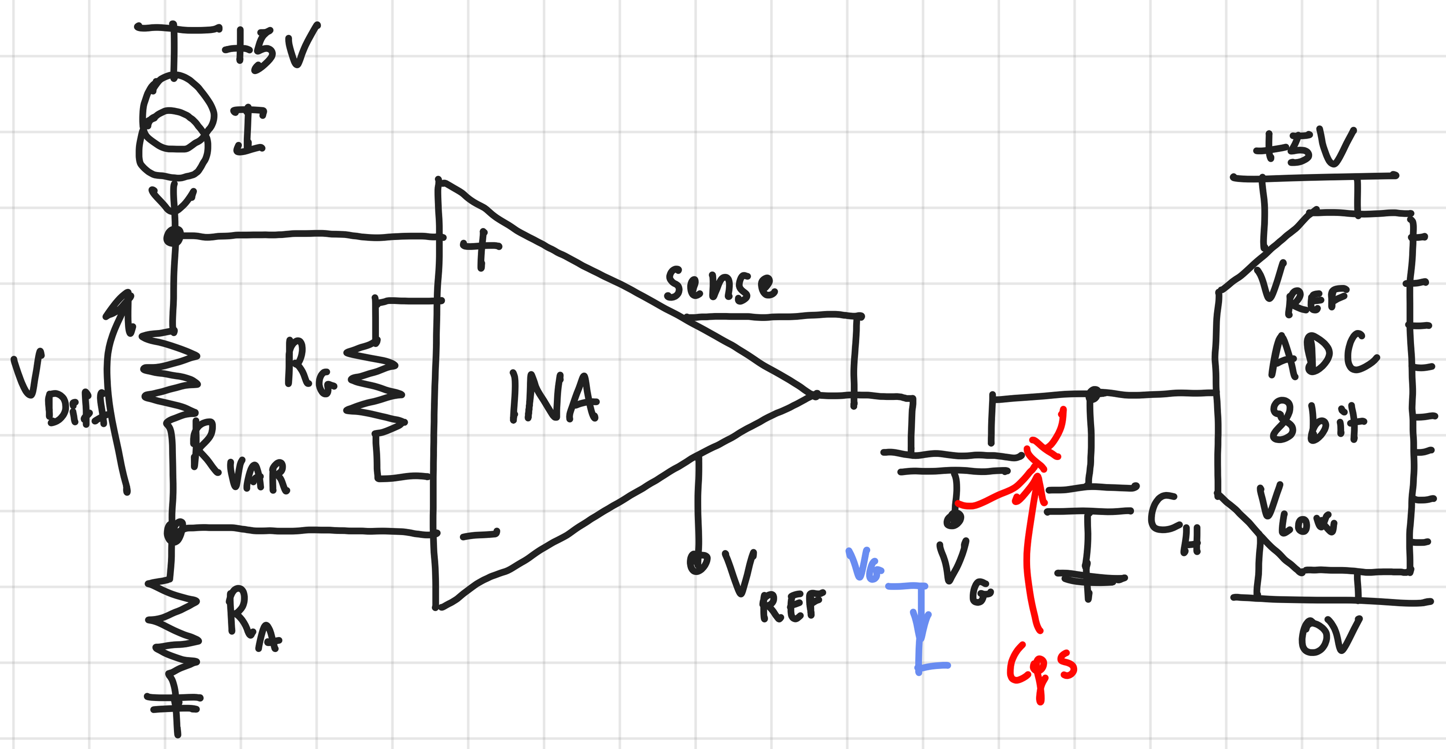
Now we have to fix the bias such that when we use $R_{VAR}|_{min} \longrightarrow V_{out} = 0$

$R_{VAR}|_{max} \longrightarrow V_{out} = 5V$

We can do it by choosing V_{REF}:

$V_{out} = V_{diff\,min}\cdot G_{INA} + V_{ref} = 0 \longrightarrow V_{ref} = -5\,V$

b)



Vg during sampling phase depnds on the out of the ina Vo+Vt

In HOLD phase

ε_{CI}

$\Delta V_G = V_o + V_T - V_{GH}$

0V

• BEST CASE $V_{out} = 0V \Longrightarrow \Delta V_G = +1V$

$\hookrightarrow \varepsilon_{CI\,out} = \Delta V_G \frac{C_{gs}}{C_{gs}+C_H} = 10\,mV \longrightarrow \varepsilon_{RVAR} = \frac{\varepsilon_{CI\,out}}{G_{INA}} = 2\,mV$

• WORST CASE $\Delta V_G = 6\,V$

Vo=+5V

$\hookrightarrow \varepsilon_{CI\,out} = 60\,mV \longrightarrow \varepsilon_{RVAR} = 12\,mV$

c) $T_{conv} = ?$ $\quad T_{ck} = ?$ | precision $< \frac{LSB}{2}$

$$LSB = \frac{FSR}{2^{nbit}} = \frac{5V}{2^8} = 19.5\,mV$$

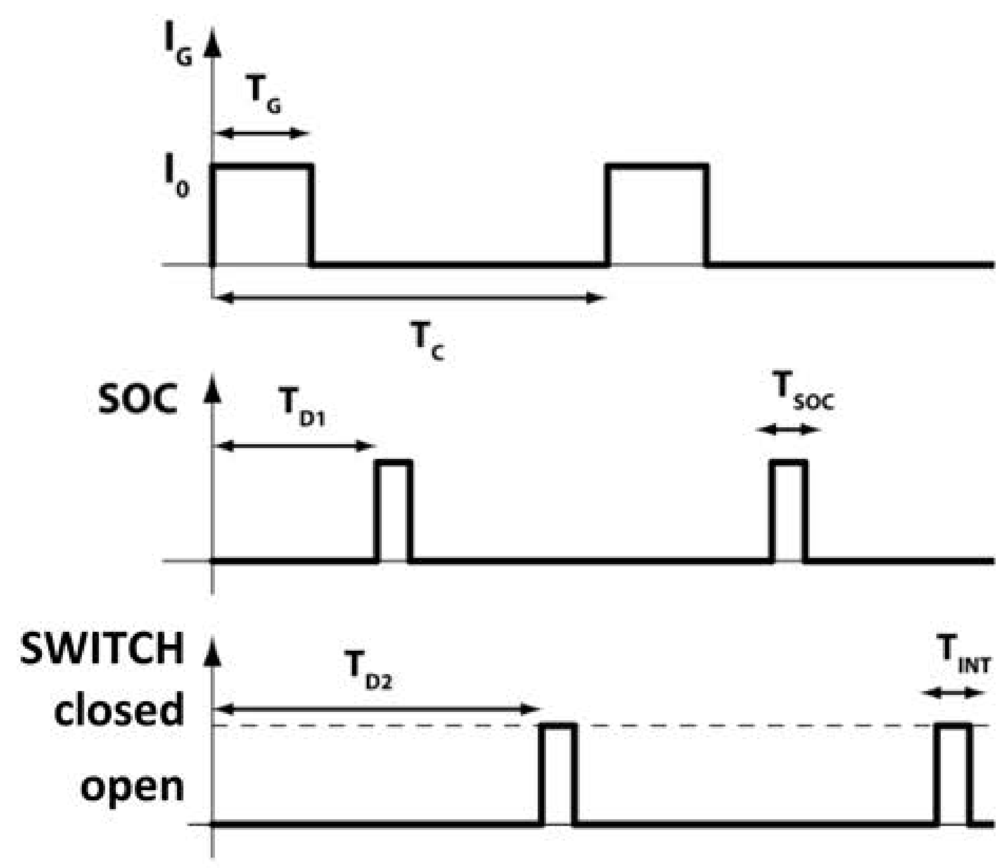
$$T_{conv} = \frac{\frac{LSB}{2} C_H}{I_{leakage}} = 1.95\,ms$$

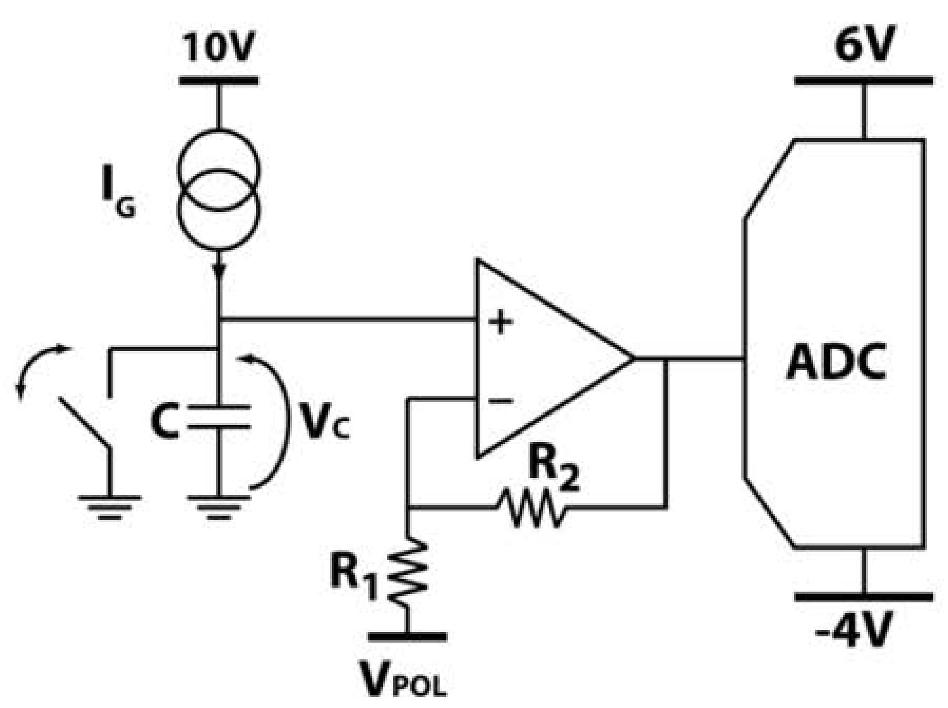
$$\left[T_{conv} = (n+1)\,T_{ck}\right] \Longrightarrow T_{ck} = \frac{T_{conv}}{9} = 216.6\,\mu s$$

5 ex on Prof solutions

Ex. 5

Let us measure the C value with the timings shown in figure. The ADC conversion is triggered by the SOC rising-edge and lasts $T_{CONV}=1\mu s$.
$R_1=4.7k\Omega$, $R_2=100k\Omega$, $V_{POL}=0.25V$, $T_{D1}=2\mu s$, $T_{D2}=4\mu s$, $T_{SOC}=0.2\mu s$, $T_{INT}=0.2\mu s$.
The $I_G=0.5mA$ current generator is pulsed with duration $T_G=1.2\mu s$ and period $T_C=5\mu s$. OpAmp biased at $\pm10V$.
a) Plot $V_C(t)$ for $C=2nF$ (be $V_C(0)=0V$ for $t=0s$).
b) Determine the range of measurable C values.





15/12/2022

E04 (Buretta)

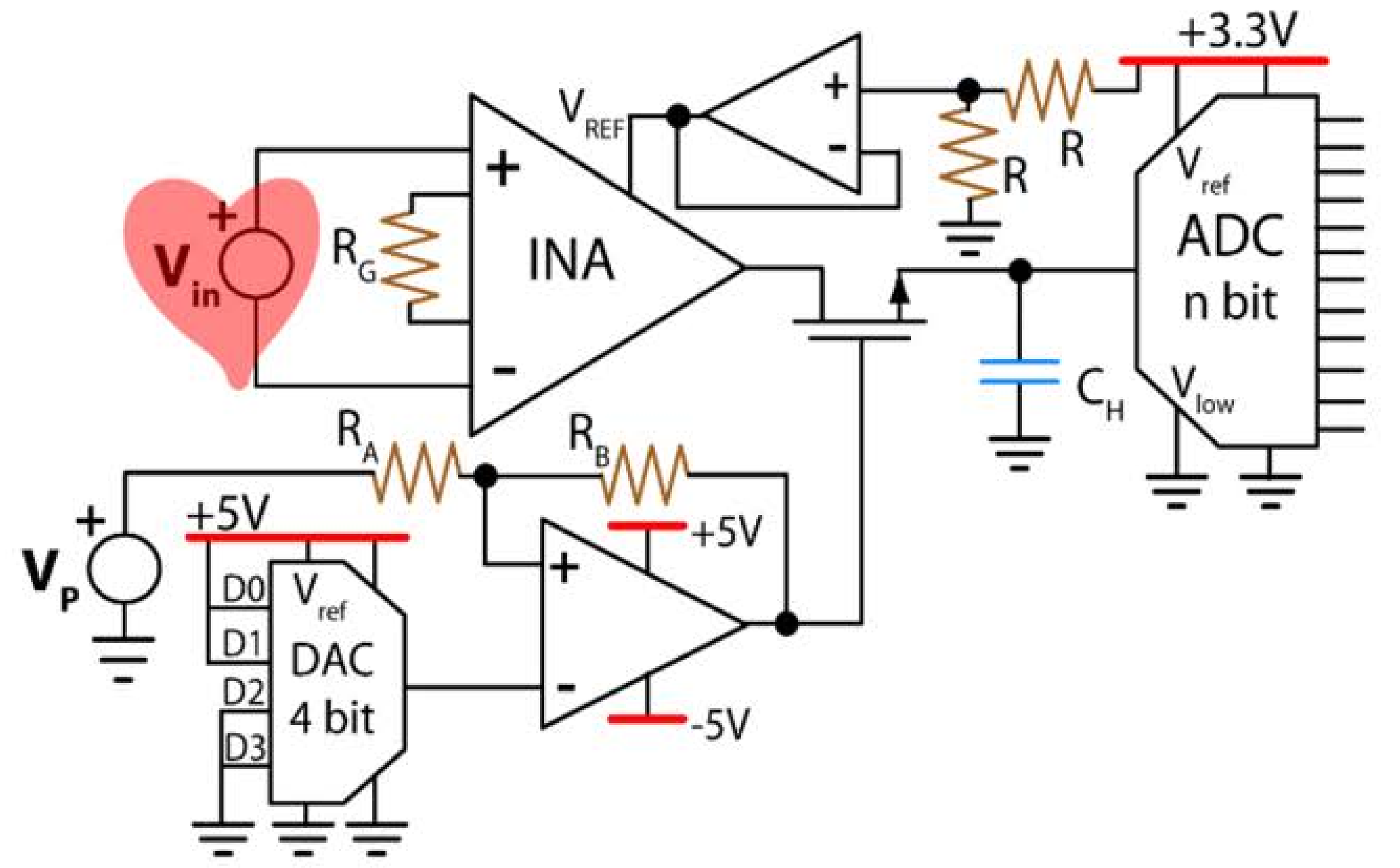
Ex. 1

R_A=1kΩ, R_B=2kΩ, C_H=100nF. INA with internal R_F=10kΩ. Input ECG signal V_{in} (-1mV÷+9mV) sampled when pulse oximetry signal V_P reaches the threshold set by the DAC. MOSFET with V_T=0.8V and $R_{DS\,on}$<100Ω.

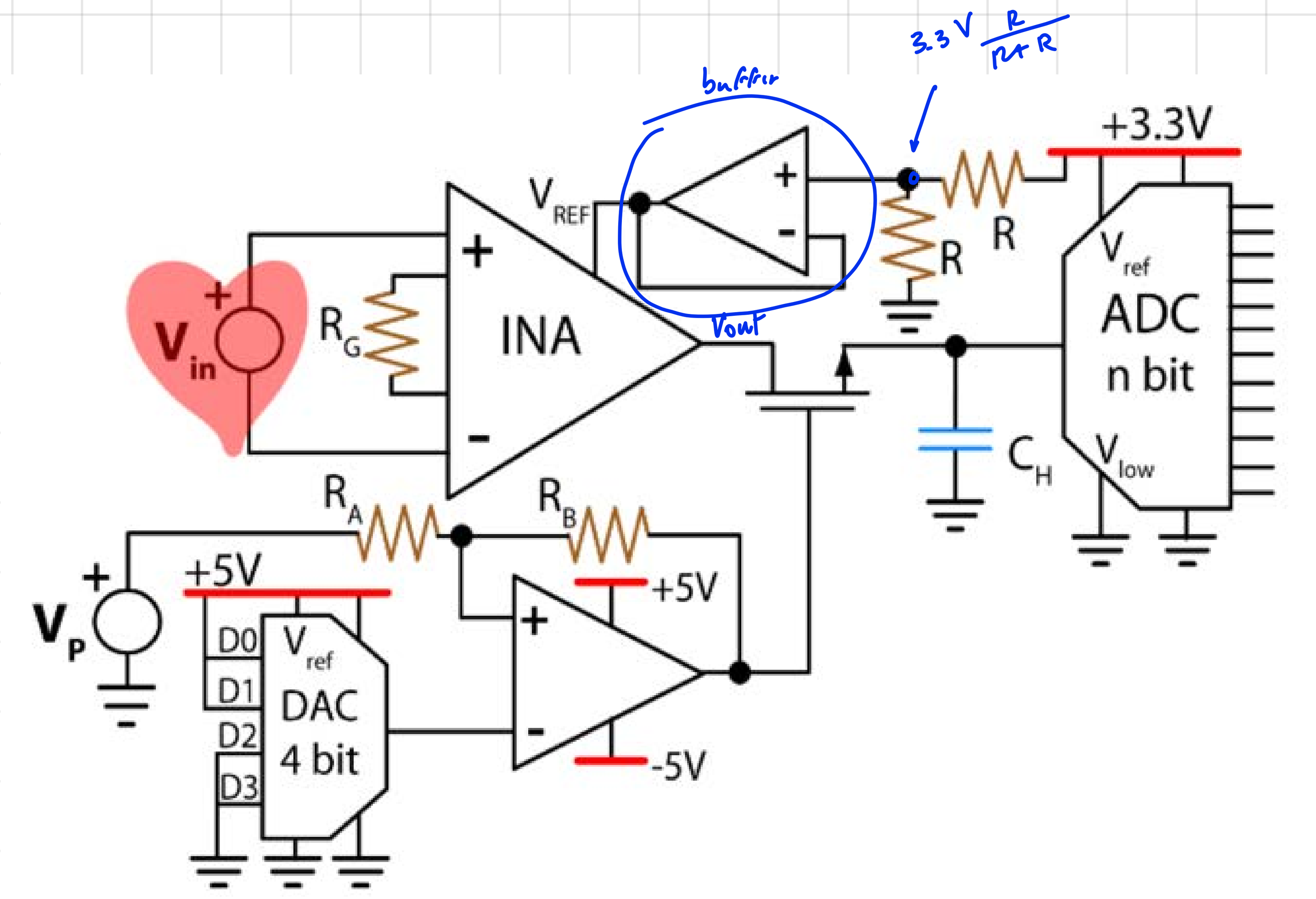
a) Properly size R_G so to exploit ADC dynamics at its best and choose the number n of bits to provide 50ppm FSR resolution.

b) Compute the V_p values that start sampling and hold phases, respectively, of the S&H.

c) Choose the parasitic C_{gsmax} that ensures a charge injection lower than 100μV.



a) $R_G = ?$ $n_{bit} = ?$ 50ppm FSR



- $V_{out} = V_{in}\, G_{INA} + V_{ref}$
- $V_{ref} = 3.3\text{ V}\,\dfrac{R}{R+R} = 1.65\text{ V}$
- $\underbrace{V_{out\,max}}_{3.3V} = \underbrace{V_{in\,max}}_{9mV}\, G_{INA} + \underbrace{V_{ref}}_{1.65V} \longrightarrow G_{INA} = \dfrac{V_{out\,max} - V_{ref}}{V_{in\,max}} = 183.3$

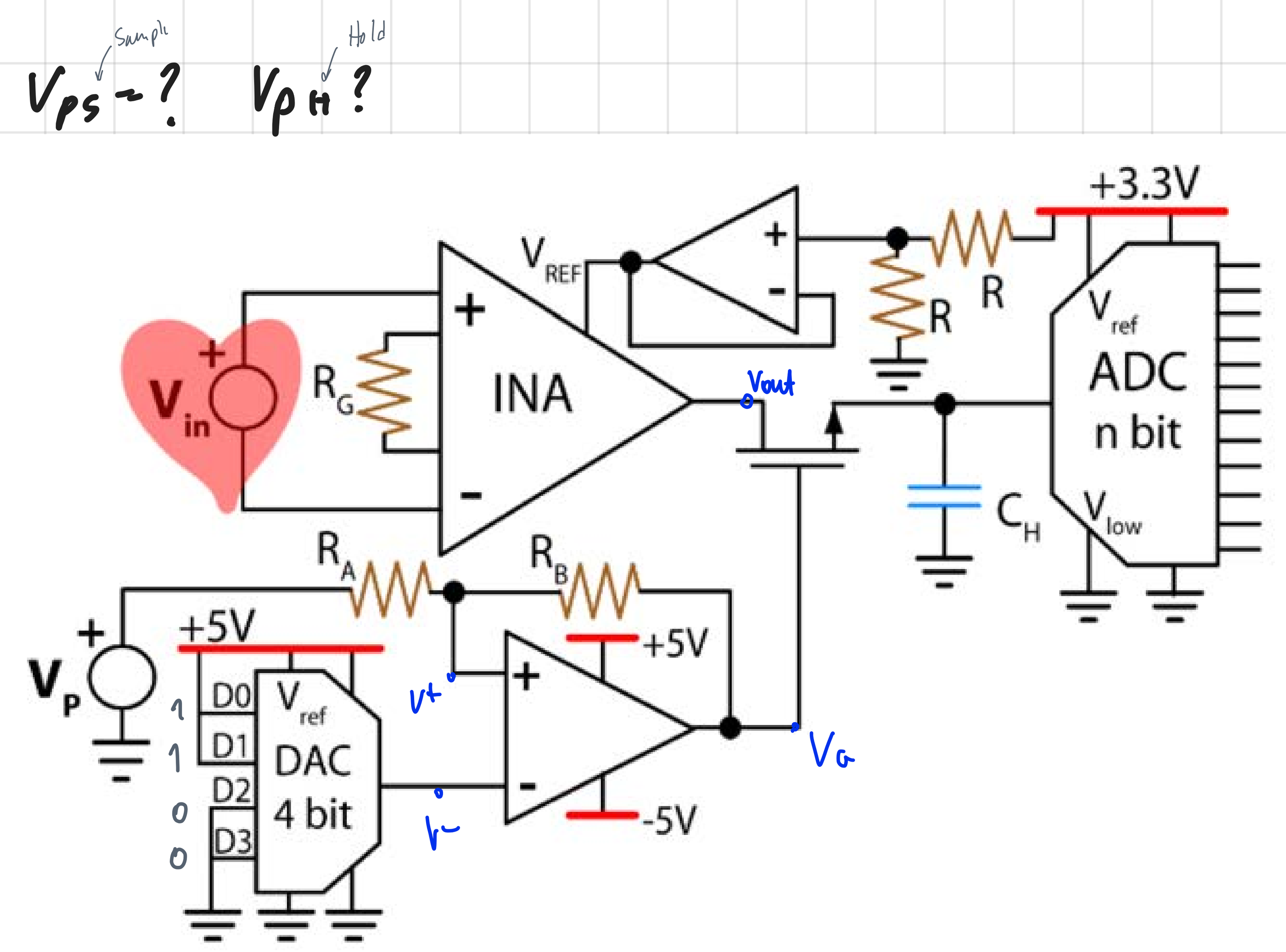
We know, from theory, that: $G_{INA} = 1 + \dfrac{2R_F}{R_G} \longrightarrow R_G = \dfrac{2R_F}{G_{INA}-1} = 110\,\Omega$

LSB = 50ppm FSR

$\dfrac{\cancel{FSR}}{2^{nbit}} = LSB = \dfrac{50}{10^{-6}}\cancel{FSR} \longrightarrow nbit \geq \log_2\left(\dfrac{10^6}{50}\right) = 14.28$

$\hookrightarrow$ nbit = 15 bit

b) $V_{PS} = ?$ V_{PH} ? (Sample, Hold)



- $V^+ > V^- \longrightarrow V_G = +5V \longrightarrow$ MOS ON $\longrightarrow$ S
- $V^+ < V^- \longrightarrow V_G = -5V \longrightarrow$ MOS OFF $\longrightarrow$ H

$\hookrightarrow$ Compute the thresholds of the comparator:

- $V^- = \dfrac{V_{ref}}{2^4} D_{in} = \dfrac{V_{ref}}{2^4}\left(\underset{1}{D_0} 2^0 + \underset{1}{D_1} 2^1 + \underset{0}{D_2} 2^2 + \underset{0}{D_3} 2^3\right) = 937.5\text{ mV}$

  D_{in}: $0011_b = 3_{10}$

- $V_{Th\,H}$: $V_G = -5V$

  Superimposition effect:

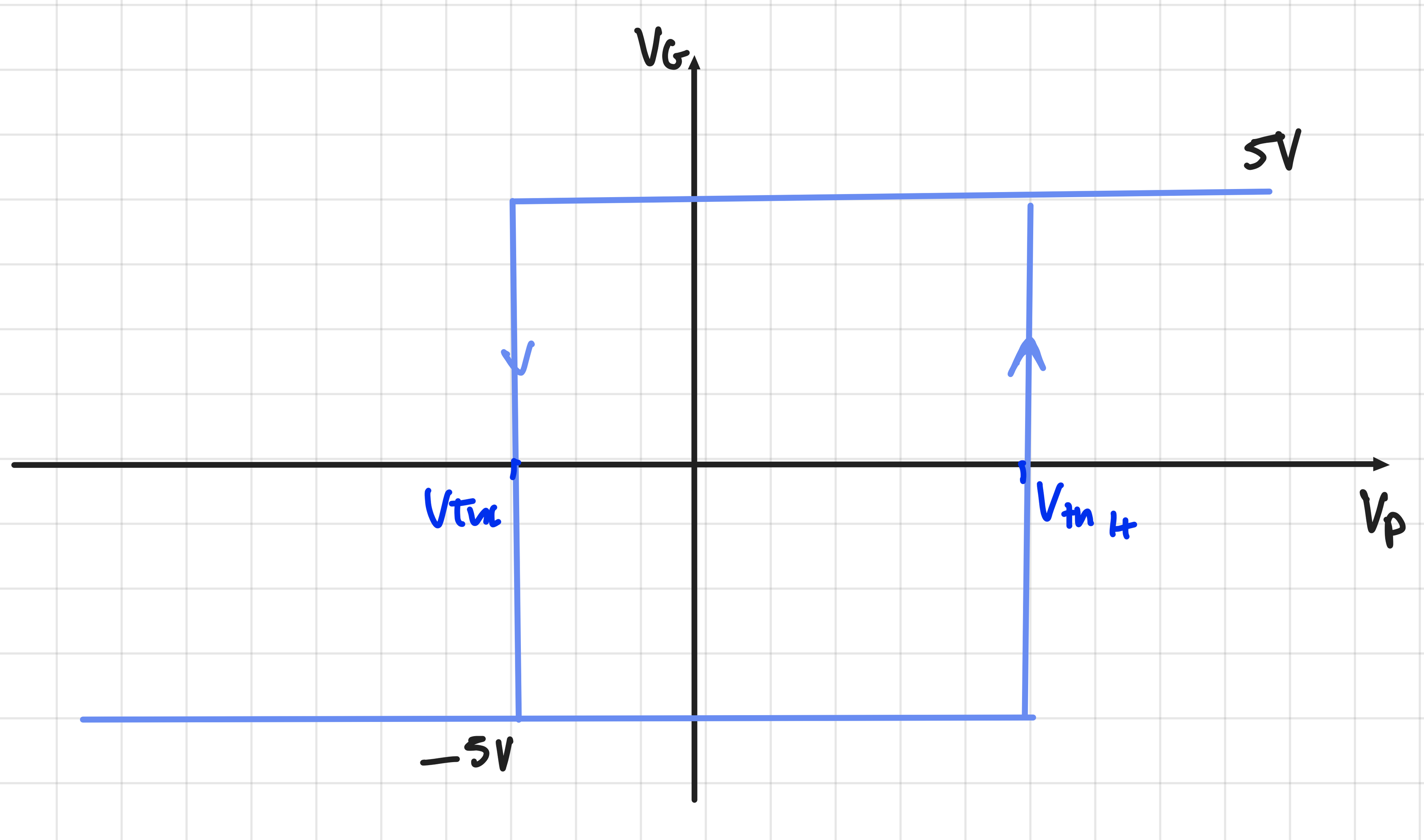
  $V^+ = \underbrace{V_p \dfrac{R_B}{R_A+R_B}}_{V_p\text{ ON},\,V_G\text{ OFF}} \underbrace{- 5V \dfrac{R_A}{R_A+R_B}}_{V_p\text{ OFF},\,V_G\text{ ON}} \geq \underbrace{937.5\text{ mV}}_{V^-}$

  $\hookrightarrow V_p \geq 937.5\text{ mV}\,\dfrac{(R_A+R_B)}{R_B} + 5V\dfrac{R_A}{R_B} = \underbrace{3.91\text{ V}}_{V_{th\,H}}$

- $V_{Th\,L}$: $V_G = 5V$

  $V^+ = V_p \dfrac{R_B}{R_A+R_B} + 5V\dfrac{R_A}{R_A+R_B} < 937.5\text{ mV}$

  $\hookrightarrow V_p < \underbrace{-1.09\text{ V}}_{V_{Th\,L}}$

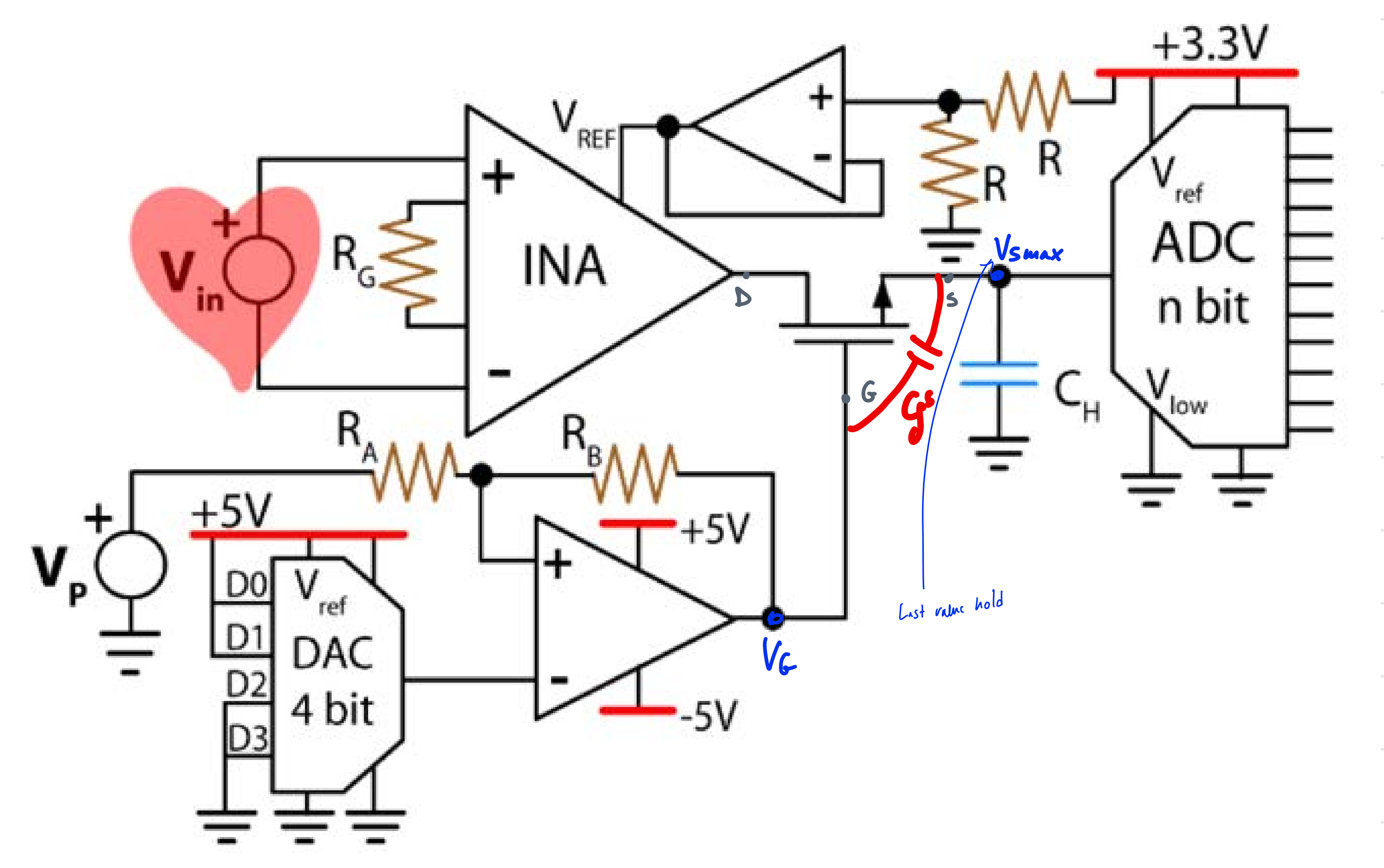


c) $\overset{\text{charge injection}}{\varepsilon_{ci}} < 100\,\mu V \qquad C_{gs\,MAX} = ?$

- $\Delta V_G = \underset{\uparrow \atop 3.3V}{V_S^{MAX}} + \underset{\uparrow \atop 0.8V}{V_T} - \underbrace{(-5V)}_{V_G} = 9.1\,V$

- $\varepsilon_{ci} = \Delta V_G^{MAX} \dfrac{C_{gs}}{C_{gs}+C_H} < 100\,\mu V$

↳ $C_{gs} < C_H \left(\dfrac{1}{\dfrac{\Delta V_G^{MAX}}{\varepsilon_{ci}} - 1} \right) \longrightarrow C_{gs} < 1.1\,pF$

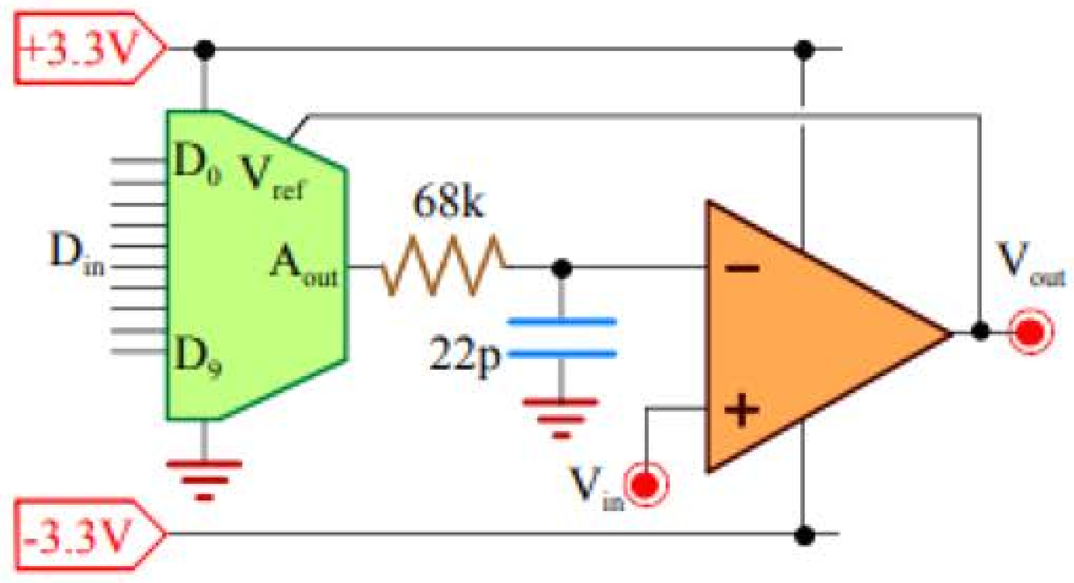


② **Ex. 2**

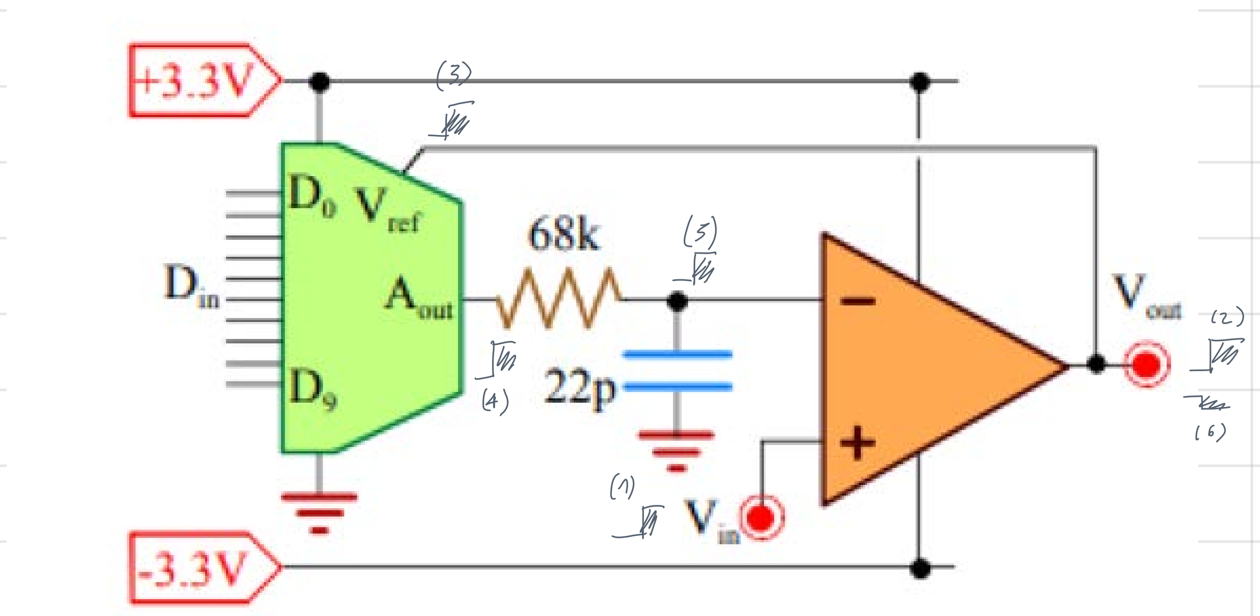
OpAmp biased at ±3.3V. DAC single-battery operated.

a) Plot the V_{out} vs. V_{in} relationship and its dependence on the 10bit D_{in} digital bus content.

b) Discuss bandwidth and stability when A_0=100dB and GBWP=10MHz depending on the D_{in} value.



a) 10 bit, Vout vs Vin

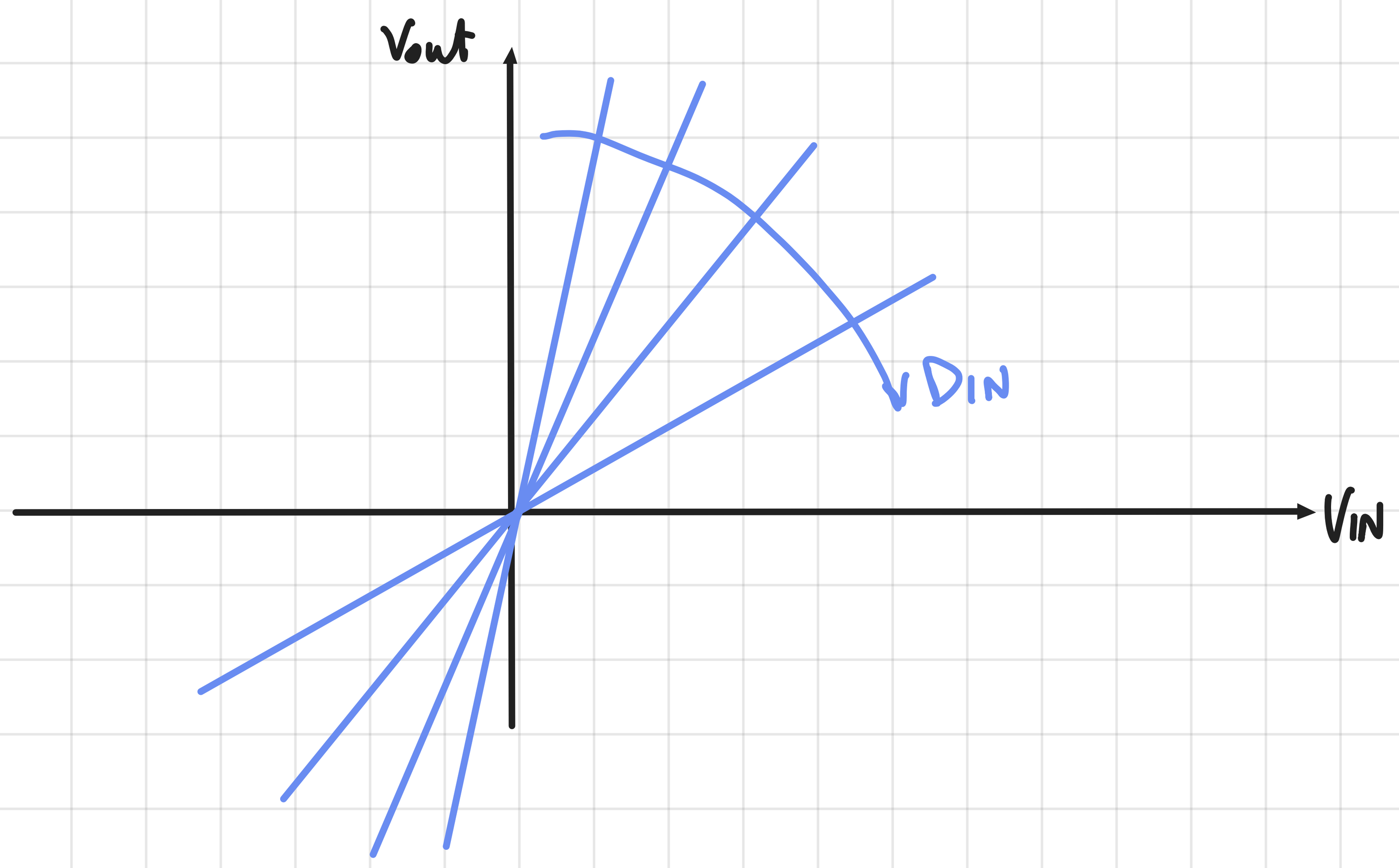


- $V_{out} = V_{ref}$ (negative feedback)
- Neg. feed → $A_{out} = V_{in}$

$A_{out} = \frac{V_{ref}}{2^{10}} D_{in}$

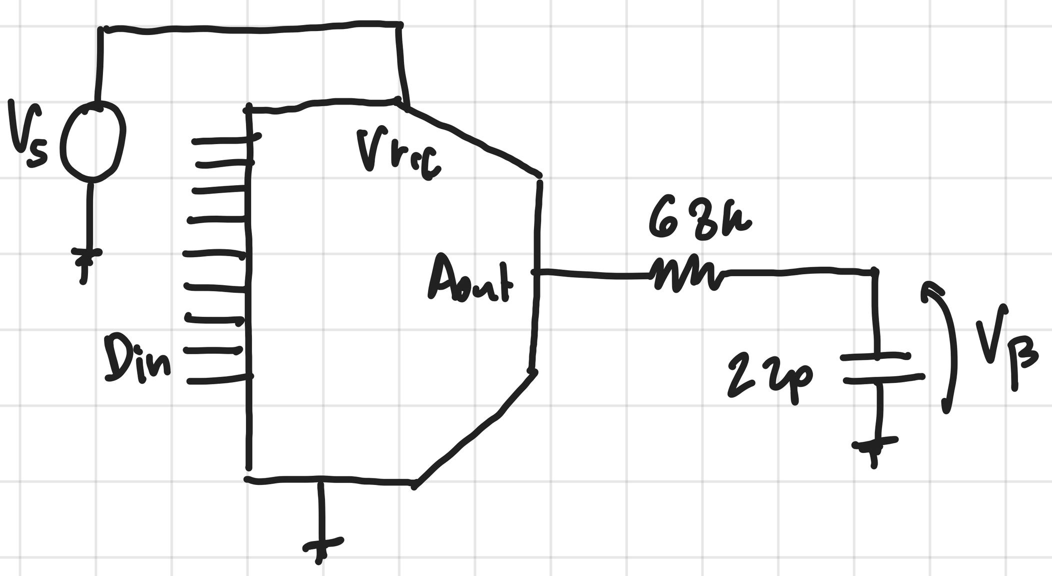
↳ $V_{in} = \frac{V_{out}}{2^{10}} D_{in}$ → $V_{out} = V_{in} \frac{2^{10}}{D_{in}}$

- $D_{IN}^{MAX} = 2^{10} - 1$
  ↳ $V_{out} = V_{IN}$ (Buffer)
- $D_{in}^{MIN} = 0$
  ↳ $G \to \infty$ (comparator)



b) $A_0 = 100\,dB$ GBWP = 10 MHz Stability?

- $A(s) \longrightarrow$ OA
- $\beta(s) \longrightarrow$

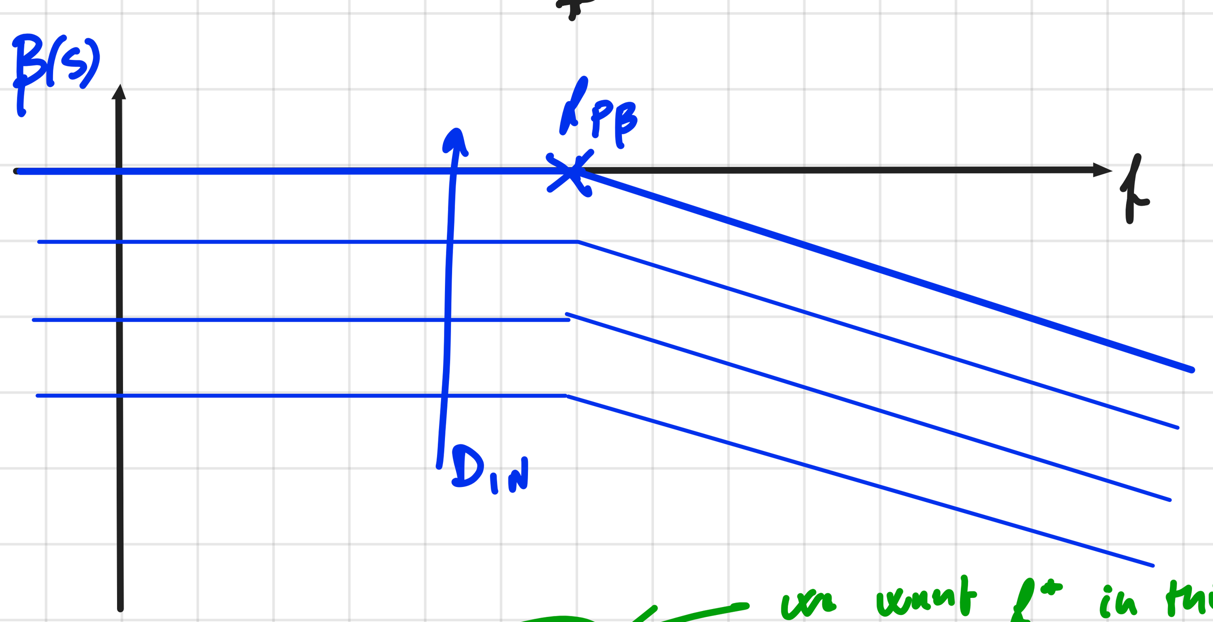


$A_{out} = \frac{V_S}{2^{10}} D_{IN}$

$\beta(0) = \frac{D_{in}}{2^{10}}$

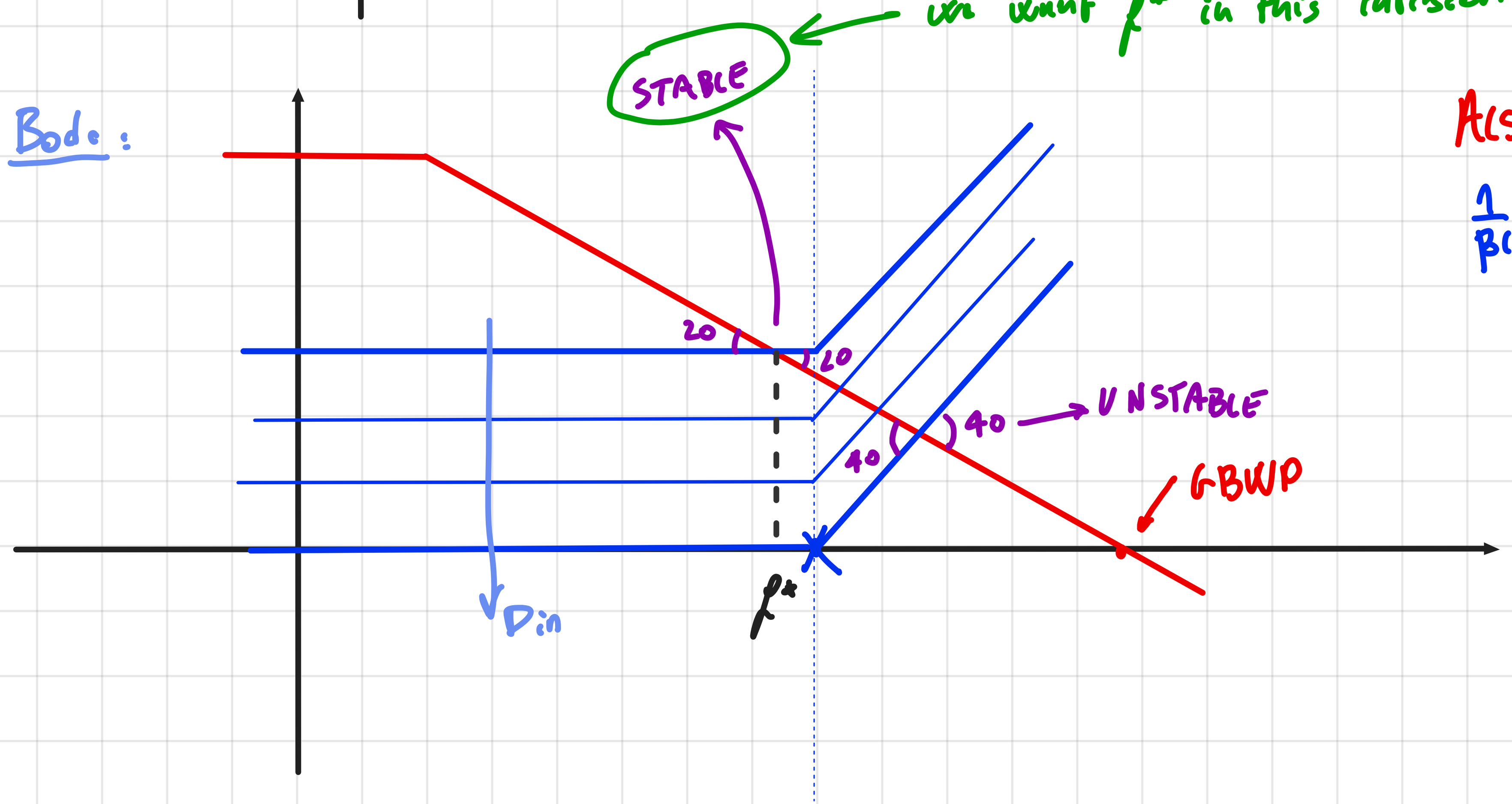
$\beta(\infty) = 0$

$f_{PB} = \frac{1}{2\pi\, 22p\, 68k} = 106\ kHz$



we want f^* in this intersection point

Bode:



$A(s)$

$\frac{1}{\beta(s)}$

→ $f^* < f_{PB}$ (for stability)

$\frac{GBWP}{\frac{1}{\beta(0)}} \le f_{PB}$ → $\frac{GBWP}{2^{10}} D_{in} \le f_{PB}$

$D_{in} \le \frac{f_{PB} \cdot 2^{10}}{GBWP} = 10.85$

$\Rightarrow D_{in_{max}} = 10$

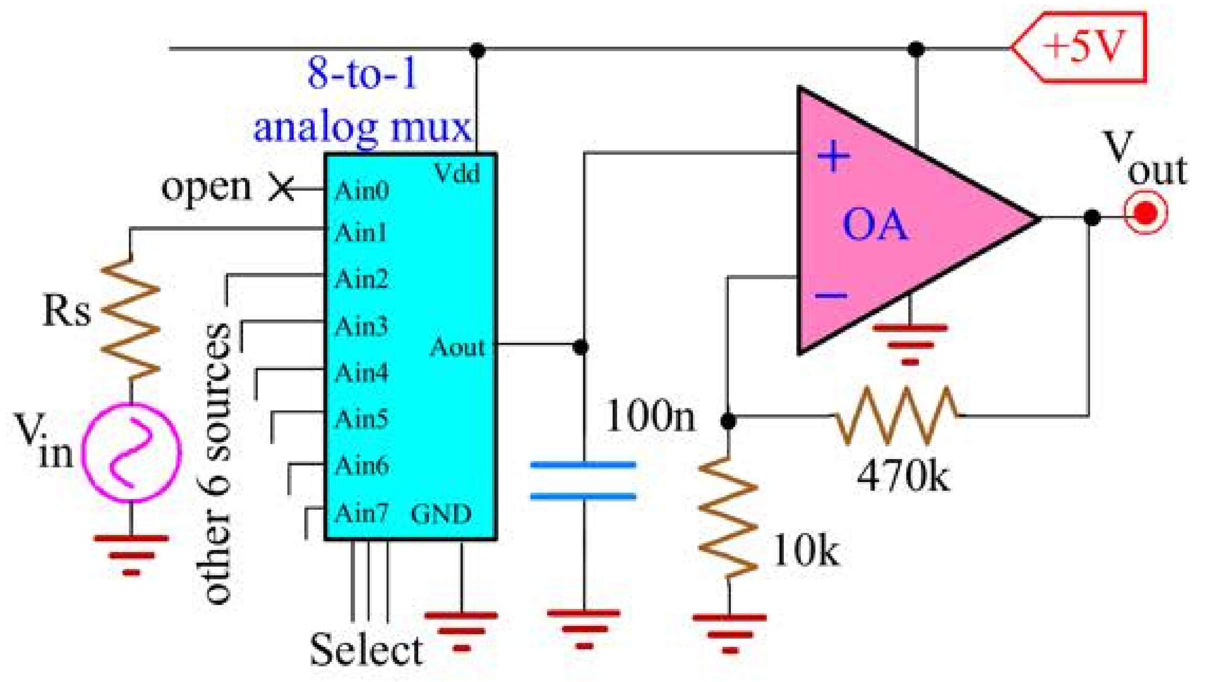
3

Ex. 3

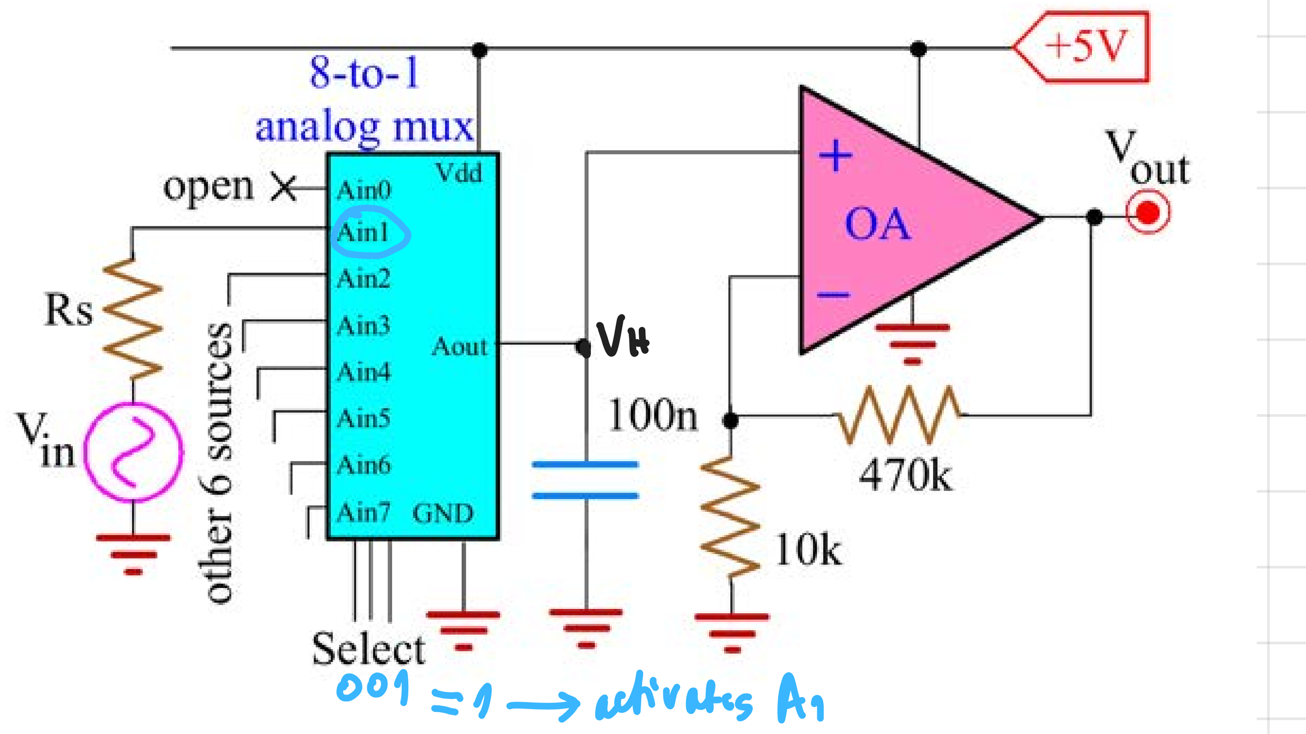
The circuit acquires 7 signals in the range 0÷100mV. R_S is in the 500Ω÷2kΩ range. The OpAmp has I_{bias}=1nA, V_{OS}=1mV, A_0=50V/mV. The mux has R_{on}=2÷20Ω, R_{off}=3MΩ÷30MΩ and $I_{leakage}$=4nA.

a) Compute the sampling time (when Sel=001) and the hold time (Sel=000) to attain an accuracy of 16bit.

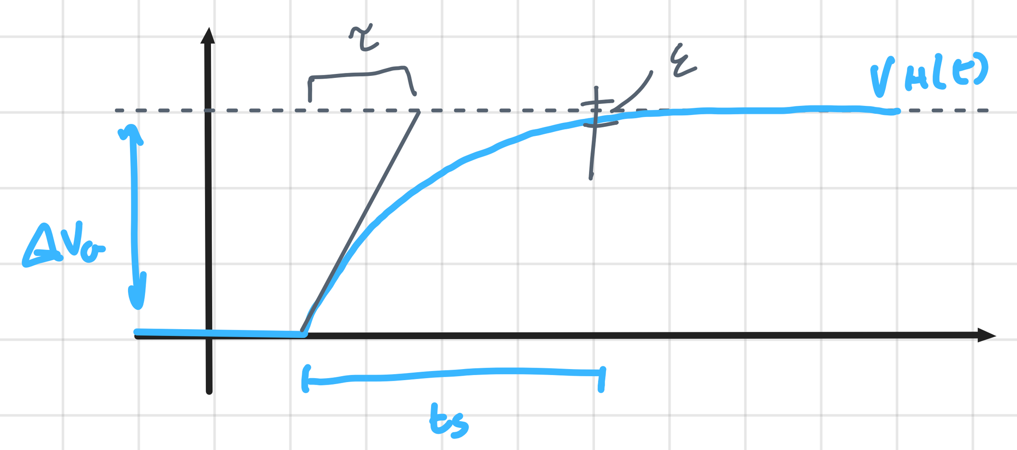
b) Determine the maximum static error at the output.



a) $t_s = ?$ (Sel = 001) ← sampling $t_H = ?$ (Sel = 000) ← Hold | Accuracy of nbit = 16 bit



• Consider the sampling phase:



$V_H(t) = \Delta V_H (1 - e^{-\frac{t}{\tau}})$

$\Delta V_H (1 - e^{-\frac{t_s}{\tau}}) = \Delta V_H - \varepsilon$

$\varepsilon = \Delta V_H \, e^{-\frac{t_s}{\tau}} < \bar{\varepsilon}_s \longrightarrow$ max error: $\bar{\varepsilon}_s = \frac{LSB}{2}$

↳ $\ln\left(\frac{\Delta V_H}{\bar{\varepsilon}_s}\right) < \frac{t_s}{\tau}$

$\Longrightarrow \boxed{t_s > \tau \ln\left(\frac{\Delta V_H}{\bar{\varepsilon}_s}\right)}$

• $\tau^{MAX} = C_H \left[(R_s^{max} + R_{ON}^{max}) \,\|\, \frac{R_{OFF}^{max}}{6} \right] \cong 100nF \cdot 2k\Omega = 200\,\mu s$

6 ← # channels

We have to consider the worst case (for R_s^{max}, R_{ON}^{max}, R_{OFF}^{max})

↳ to compute the minimum sampling time t_s

• $\Delta V_H^{max} = 100\,mV$

• $\bar{\varepsilon}_{s_{Aout}} = \frac{LSB}{2} \cdot \frac{1}{G}$, $LSB = \frac{FSR}{2^{16}} = \frac{5V}{2^{16}} = 76.3\,\mu V$

Hp. of the possible following ADC (seeing that the P.S are always max 5V)

↳ $G = \left(1 + \frac{470k}{10k}\right) = 48$ ⟶ $\bar{\varepsilon}_s = \frac{LSB}{2} \cdot \frac{1}{G} = 795\,nV$

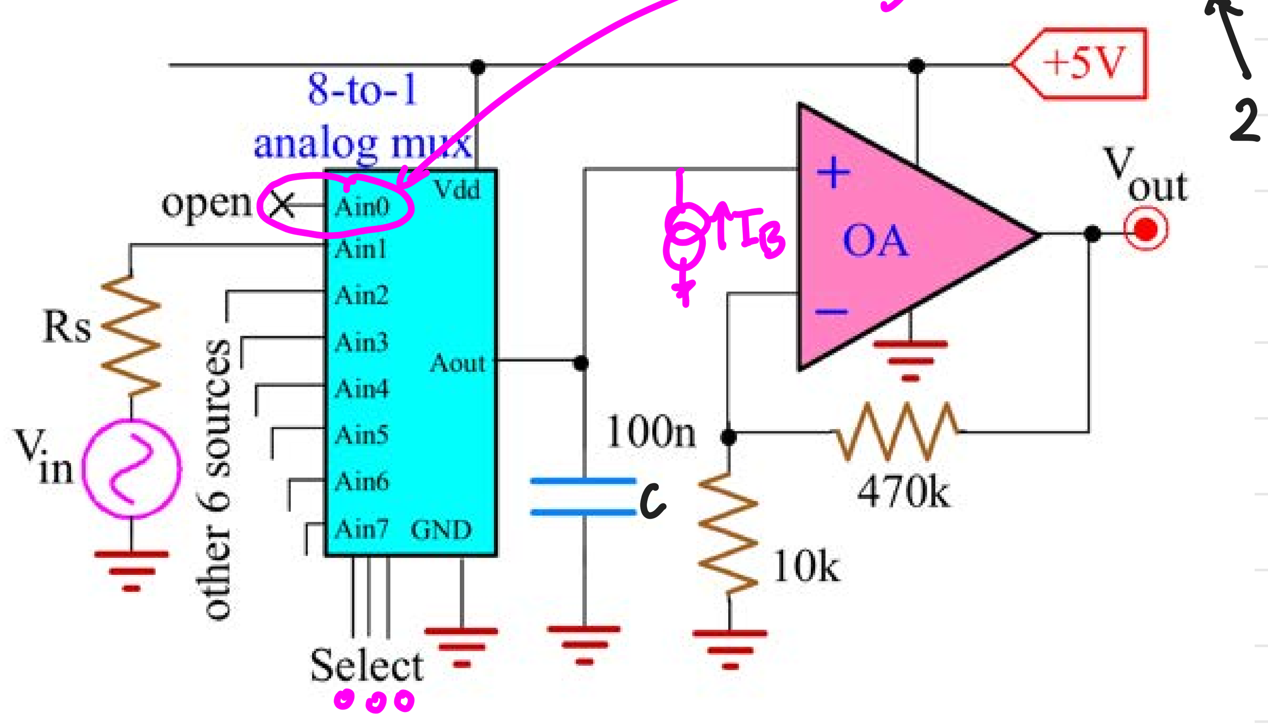
OA: non inverting stage

$\Longrightarrow t_{s_{min}} = \tau^{MAX} \ln\left(\frac{\Delta V_H^{MAX}}{\bar{\varepsilon}_{s_{Aout}}}\right) = 2.37\,ms$ (Sel = 001)

• Consider now the holding phase for Sel = 000

Ron just for Ain0, (from Ain1 – Ain7 all in Roff)

2 leakage currents (one for each side of the switch)

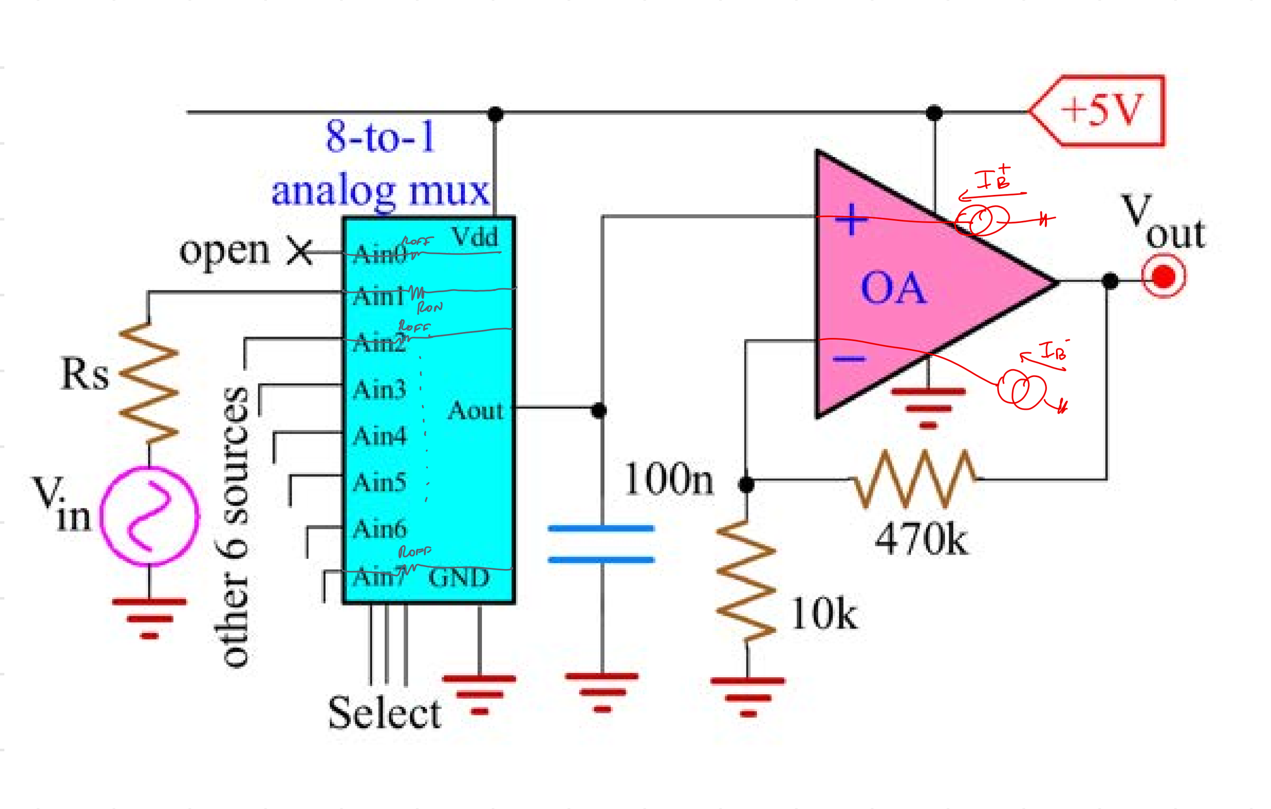


$\underbrace{\frac{I_{leak\,TOT}}{C} \cdot t_H}_{\text{linear discharge of the C capacitance}} = \varepsilon < \bar{\varepsilon}_H = \frac{LSB}{2} \longrightarrow t_H < \frac{C_H \bar{\varepsilon}_H}{I_{leak\,TOT}}$

• $I_{leak\,TOT} = I_B + (7 + 2) I_{leak}$ ⟶ $t_H^{max} = \frac{C_H \bar{\varepsilon}_H}{I_B + 9 I_{leak}} = 2.15\,\mu s$

bias current; OFF (Ain1–7); 2 for ON (Ain0)

b) Static errors



- Static error due to R_{OFF} voltage divider (during sampling phase)

$$\varepsilon_H' = 100\,mV \, \frac{R_s^{max} + R_{ON}^{max}}{R_s^{max} + R_{ON}^{max} + \frac{R_{OFF}^{min}}{6}} = 460\,\mu V$$

$$\varepsilon_{Hout}' = \varepsilon_H' \, G = 22\,mV$$

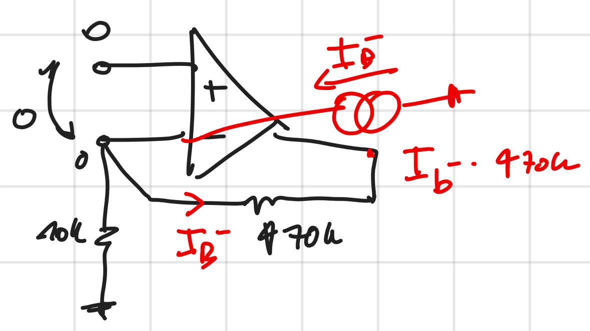
- Static error due to bias current I_B^+ and I_{leak}

$$\varepsilon_{Hout}'' = G\,\varepsilon_H'' = 48\,(I_b^+ + 9\,I_{leak})\left[\frac{R_{OFF}^{max}}{6} \,//\, (R_s^{max} + R_{ON}^{max})\right] = 3.59\,mV$$

same previous reasoning → 2 leak for Ain0, 1 for the rest

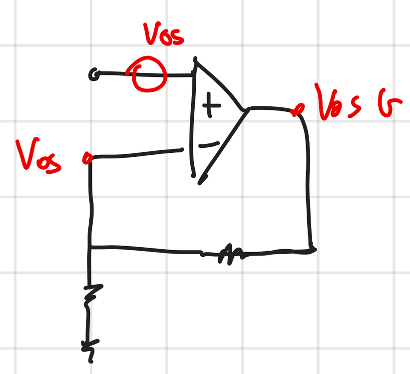
- Static error due to bias current I_B^-

$$\varepsilon_{Hout}''' = I_b^- \cdot 470k = 470\,\mu V$$



- Static error due to offset V_{os}

$$\varepsilon_{Hout}^{IV} = V_{os}\, G = 48\,mV$$



4

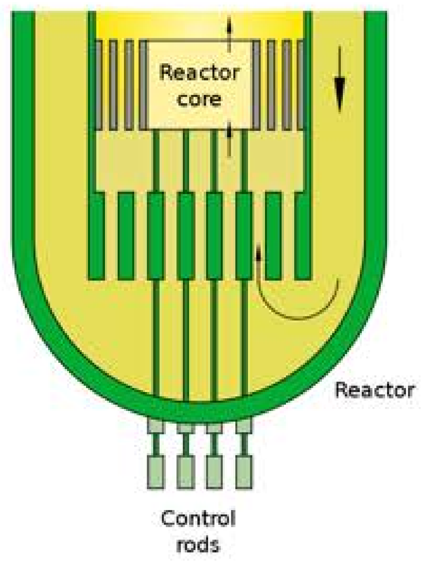
Ex. 4

A reactor heater must be **biased at constant current**, within the 50mA-500mA range. The heater has a **nominal** $R_{heater}=10\Omega$. OpAmps have just 10 mA *output driving capability*.

not enough (*)

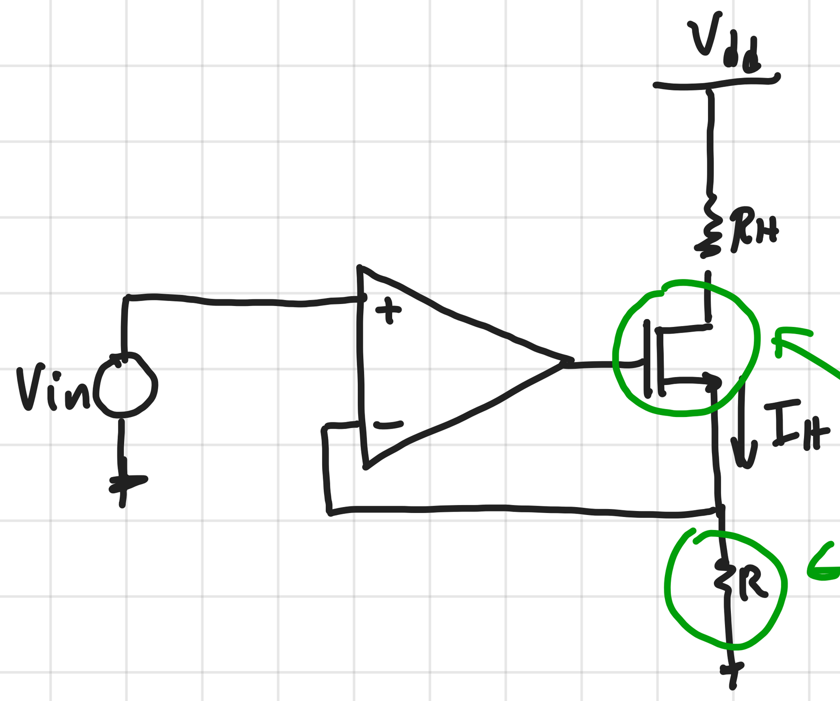
a) **Linearly** drive the heater through a voltage input, from V_{in}=0V (providing I_{heater}=50mA) to V_{in}=5V (I_{heater}=500mA) and all other values in the between (with linear relationship), after filtering with **three** 100Hz **low-pass poles**.

b) Turn on a red LED whenever the voltage across the pump differs from the expected nominal value (**at the set current**) by more than 100mV.



a) We know that just the OpAmp is not enough to drive our circuit (*)

We have:



Add this to provide the current in the correct range

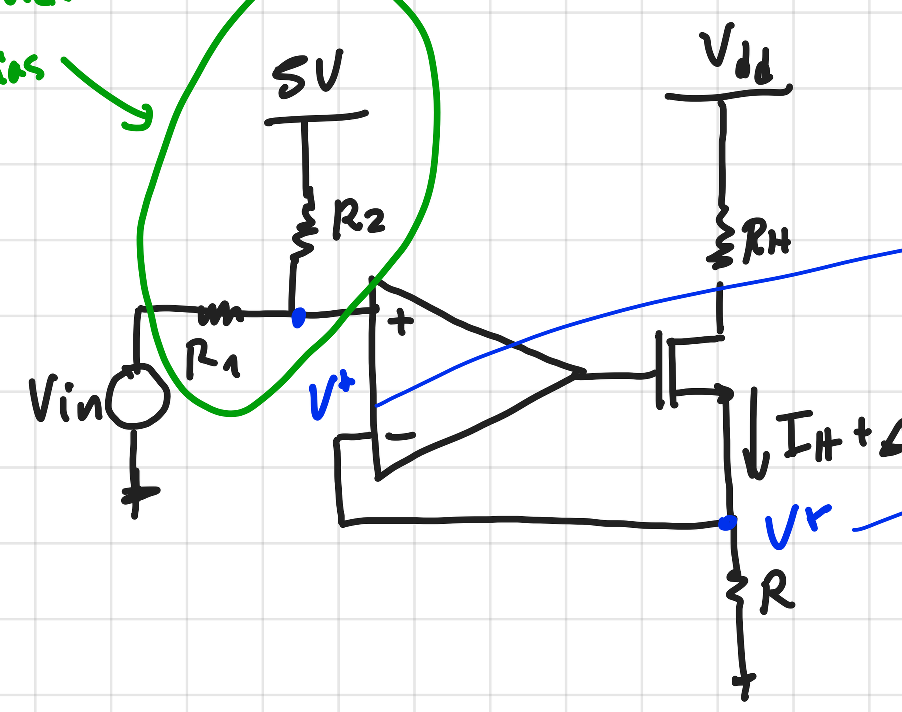
$I_H = \frac{V_{in}}{R}$

- $V_{in} = 0 \longrightarrow I_H = 50$ mA
- $V_{in} = +5V \longrightarrow I_H = 500$ mA
- 3 @ 100Hz

↳ bias baseline current 50mA + $\begin{cases} \Delta I_H = 0\text{mA} & @ V_{in}=0 \\ \Delta I_H = 450\text{mA} & @ V_{in}=5V \end{cases}$

we have to add a bias point

Voltage divider for the bias current



→ For superimposition of effect:

- $V^+ = V_{in}\frac{R_2}{R_1+R_2} + 5V\frac{R_1}{R_1+R_2}$
- $V^+ = R(I_H + \Delta I_H)$

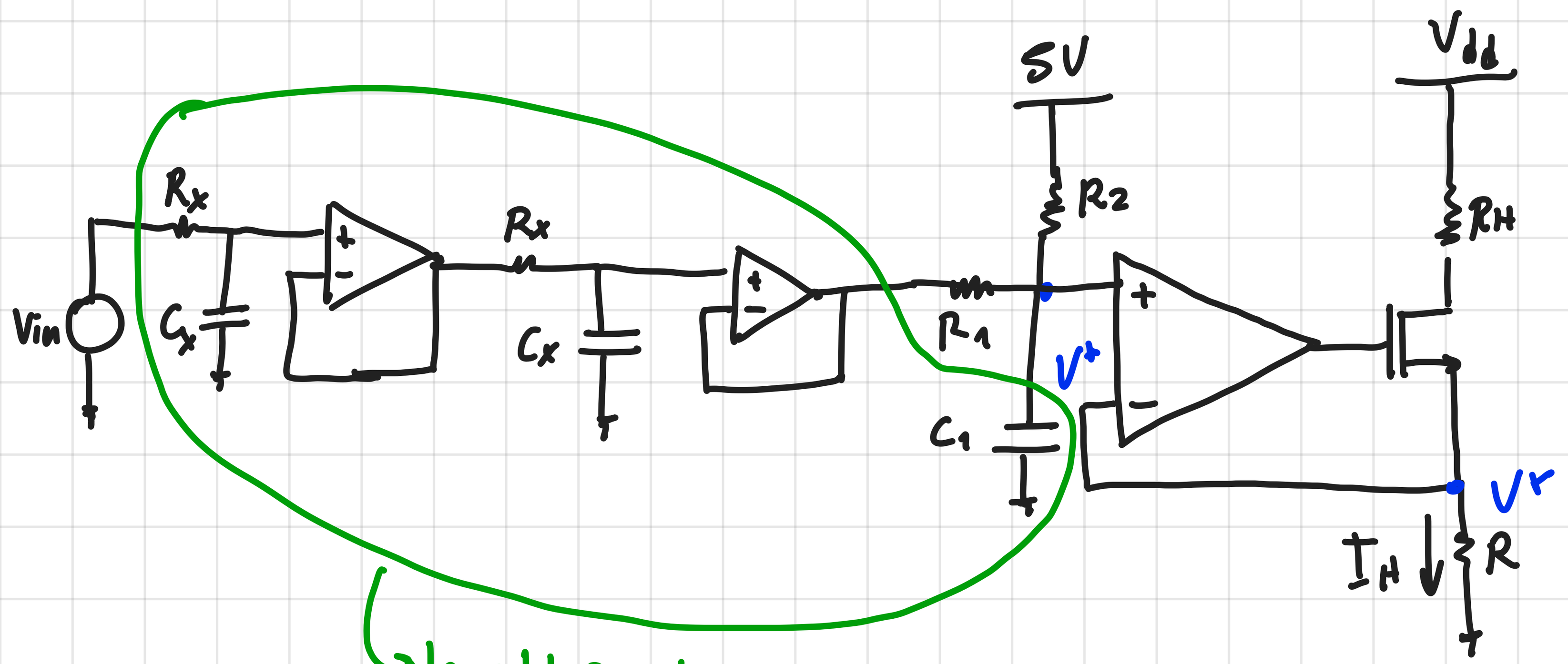
↳ @ $V_{in}=0$: $5V\underbrace{\frac{R_1}{R_1+R_2}}_{1/10} = R\underbrace{I_H}_{50mA}$

↳ @ $V_{in}=5V$: $5V\underbrace{\left(\frac{R_2}{R_1+R_2}+\frac{R_1}{R_1+R_2}\right)}_{1} = R\underbrace{(\overset{50mA}{I_H} + \overset{450mA}{\Delta I_H})}_{500mA}$

↳ $R = 10\,\Omega$

$\begin{cases} R_1 = 1k \\ R_2 = 9k \end{cases}$

↳ Now we want to add 3 pole @ 100Hz



↳ to add 3 poles

→ $I_H = \frac{V_{in}}{R}$

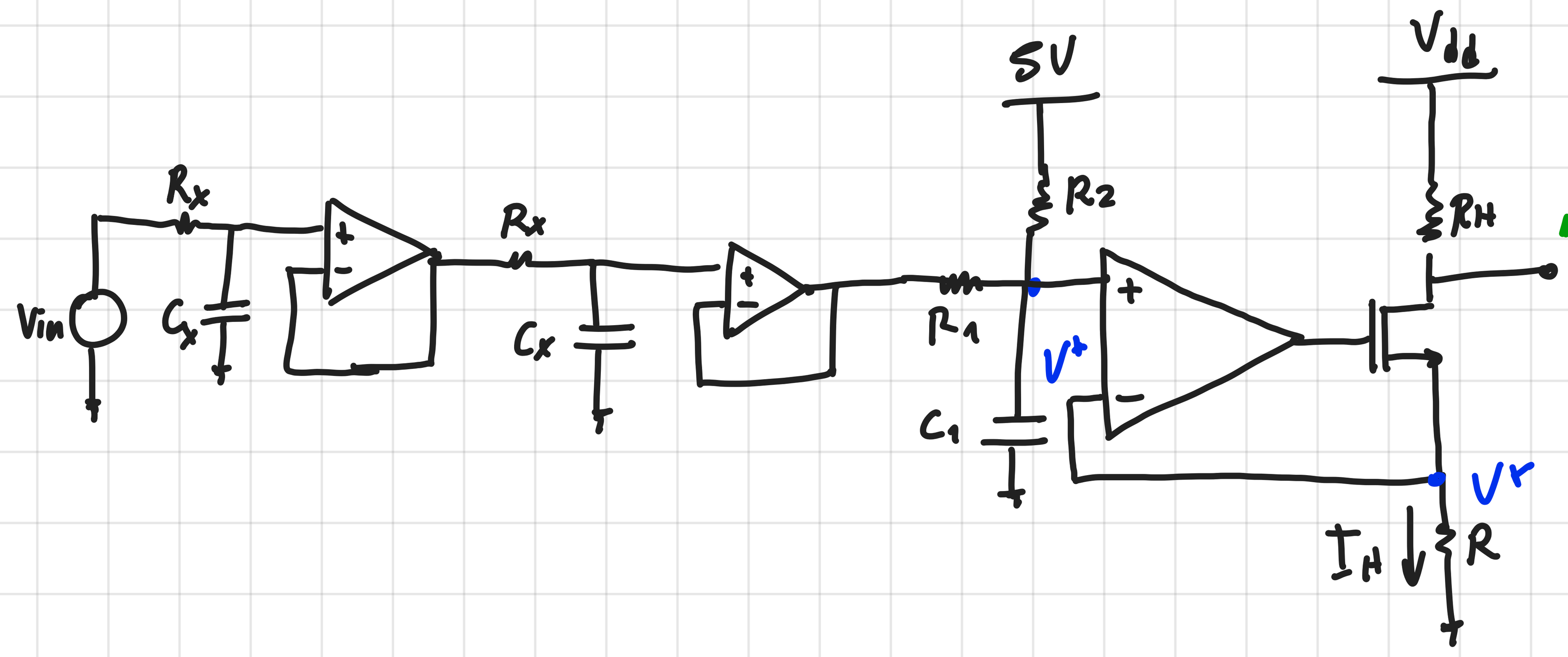
$f_p = \frac{1}{2\pi C_x R_x} = \frac{1}{2\pi C_1(R_1 \| R_2)} = 100$ Hz

$R_x = (R_1 \| R_2) = 900\,\Omega$

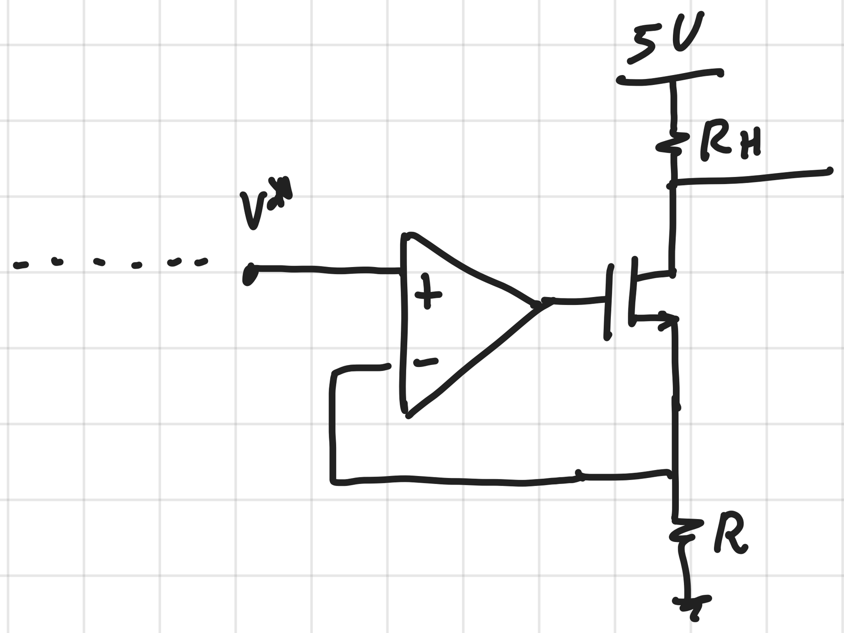
$C_1 = C_x = 1.77\,\mu F$

b) We should expect a nominal value here due to nominal R_H ← but nominal value in reality can change

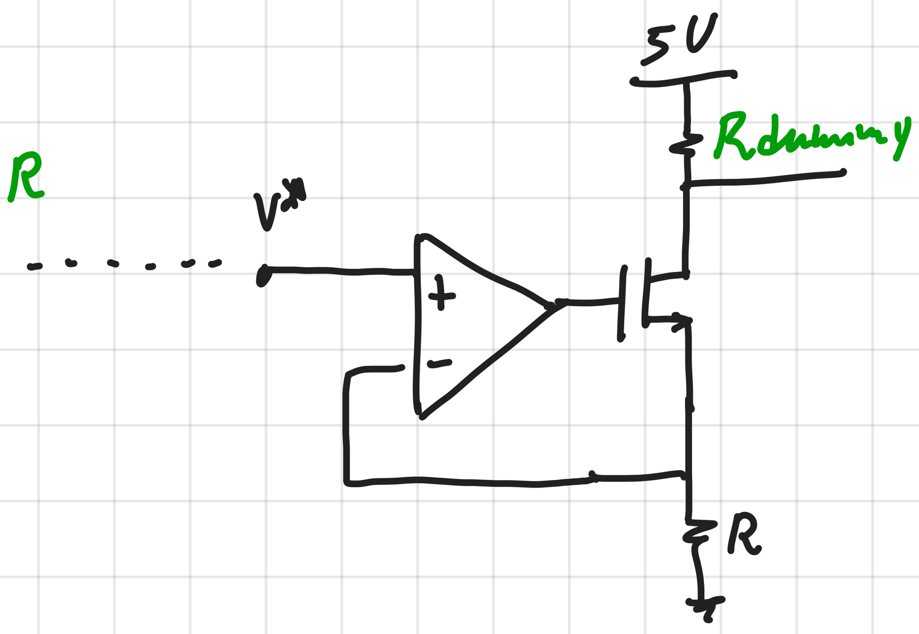
↓ we want to detect these changes an activate a LED when this happens



↳ so considering: $|\Delta V| > 100\,mV \longrightarrow$ LED ON (*)

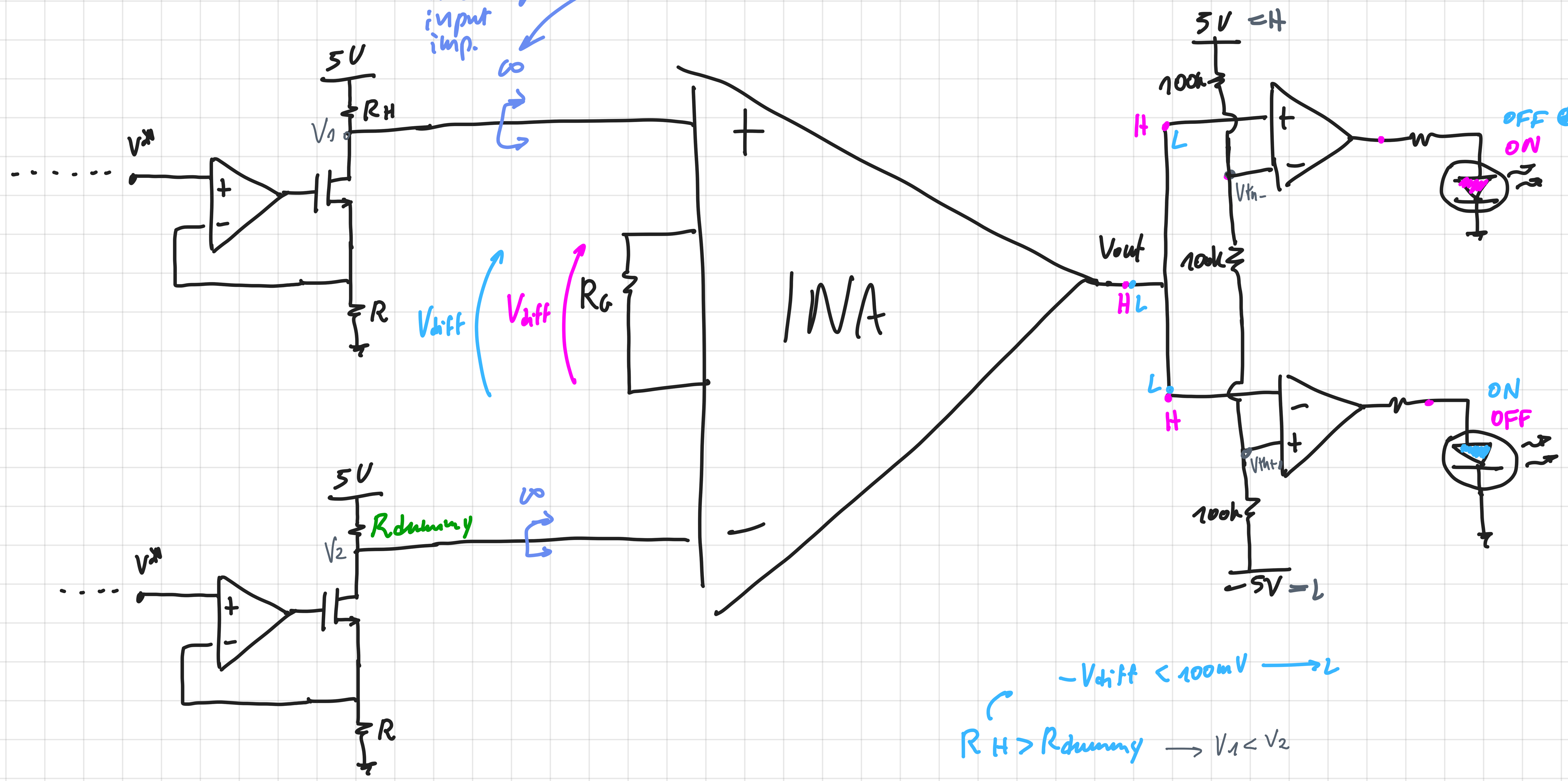


we then consider it with a "dummy" R to check the difference



to compute the difference we can use a INA

because it has high input imp. ∞



$-V_{diff} < 100\,mV \longrightarrow L$

$R_H > R_{dummy} \longrightarrow V_1 < V_2$

$R_H < R_{dummy} \longrightarrow V_1 > V_2$

↳ when $V_{diff} > 100\,mV \longrightarrow H$
$\quad = \Delta V$

↳ if $V_{out} > V_{th-}$ (*)

↳ Now we have to compute the INA gain

$$V_{TH} = \underbrace{5V\,\frac{2}{3}}_{\text{due to } 5V} - \underbrace{5V\,\frac{1}{3}}_{\text{due to } -5V} = 1.67\,V$$

$$V_{TL} = \underbrace{-5V\,\frac{2}{3}}_{\text{due to } -5V} + \underbrace{5V\,\frac{1}{3}}_{\text{due to } +5V} = -1.67\,V$$

$$G_{INA} = \frac{1.67\,V}{100\,mV} = 16.66 \Rightarrow R_{INA} = 100\,k\Omega$$

$$G_{INA} = 1 + \frac{2R_{INA}}{R_G} \longrightarrow R_G = 12.77\,k\Omega$$

Voltage difference (*) → when this $V_{diff} = \pm 100\,mV$ happens at the input we want to switch → output $= \pm 1.67\,V$ = thresholds

↳ in order to switch on the LEDs as described

(5) **Ex. 5**

Monitor the laser power emitted by a laser curing device, by means of a photodiode, whose photocurrent I_{in} must stay in the 10÷70µA range, with a nominal value of 40µA. The photodiode is operated reverse-biased at 5V.

a) Provide a V_{out} in the 0÷5V range, proportional to the **absolute unbalance** away from the nominal value (i.e. 0V@40µA and +5V@10µA and +5V@70µA).

b) Switch on an LED when the photocurrent dose exceeds 2.4mC and reset the measurement every 5min.

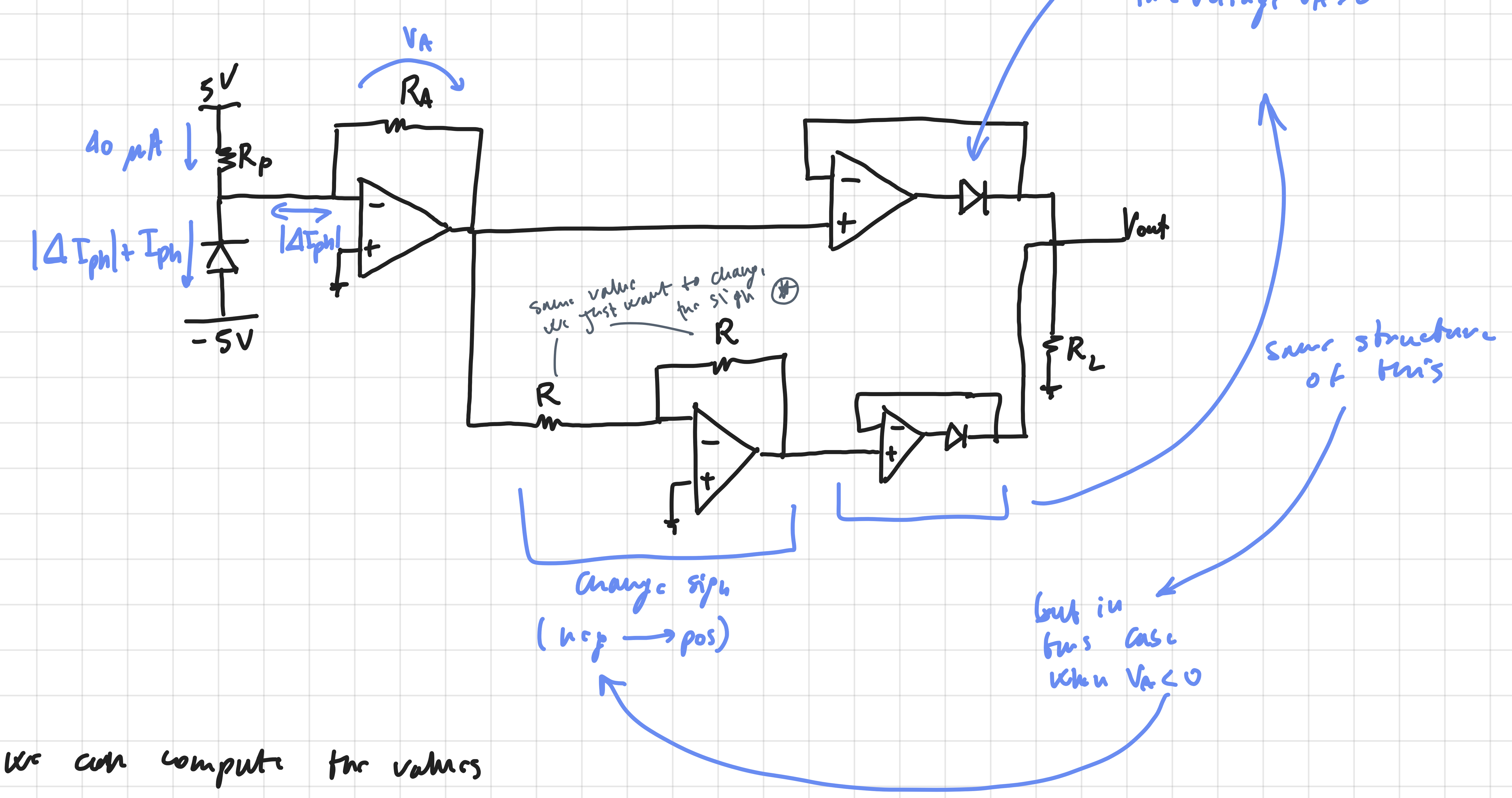
a) $V_{out} = 0 - 5V$

$$\begin{cases} \text{photodiode current } I_{in} = 10 \div 70\,\mu A \;\; [\text{nominal value } 40\,\mu A] \\ \text{photodiode reverse bias } V_{pn} = 5V \end{cases}$$

$$|\Delta I_{ph}|_{max} = 30\,\mu A$$

↳ We want: $\begin{cases} @\,40\,\mu A \longrightarrow V_{out} = 0V \\ @\,10\,\mu A \longrightarrow V_{out} = 5V \\ @\,70\,\mu A \longrightarrow V_{out} = 5V \end{cases}$

Consider the photodiode



↳ Now we can compute the values

$$R_p = \frac{5\,V}{40\,\mu A} = 125\,k\Omega$$

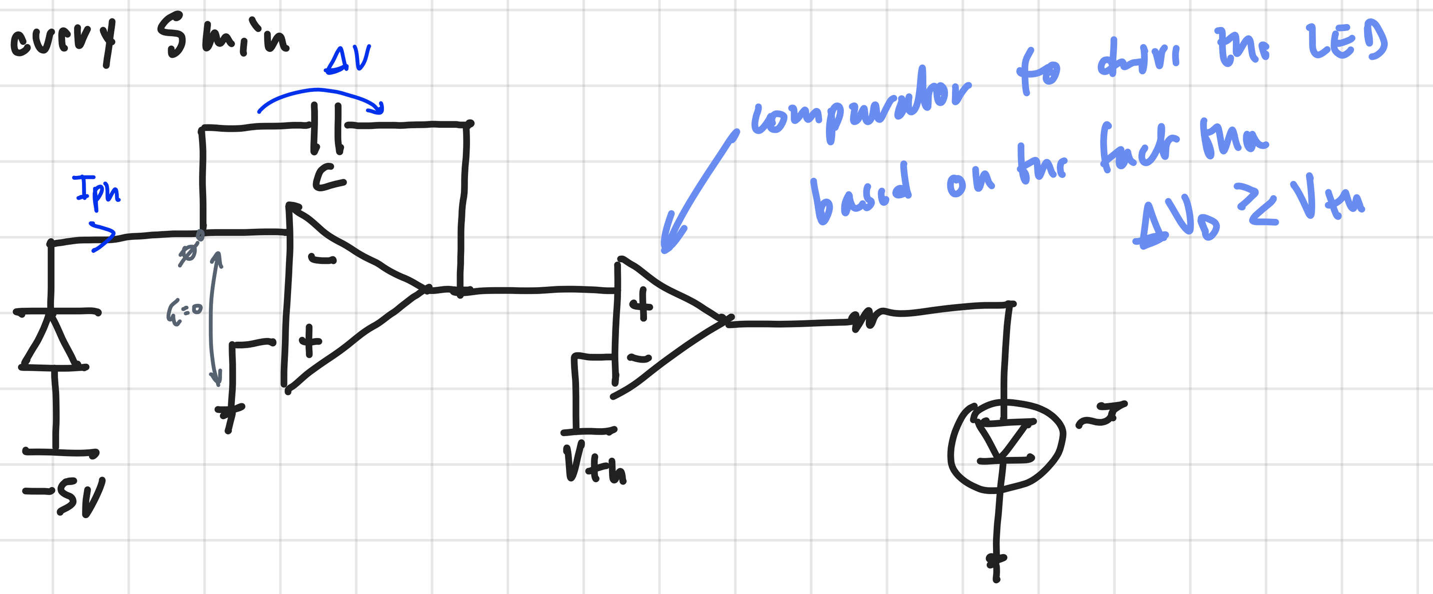
$$|V_A| = R_A |\Delta I| \longrightarrow R_x = \frac{5V}{|30\,\mu A|} = 166.66\,k\Omega$$

(R is not important the important thing is (*))

b) $Q_{ph} \geq 2.4\,mC$ ⟵ to check it we can use an integrator stage

↑ charge

\+ reset every 5 min



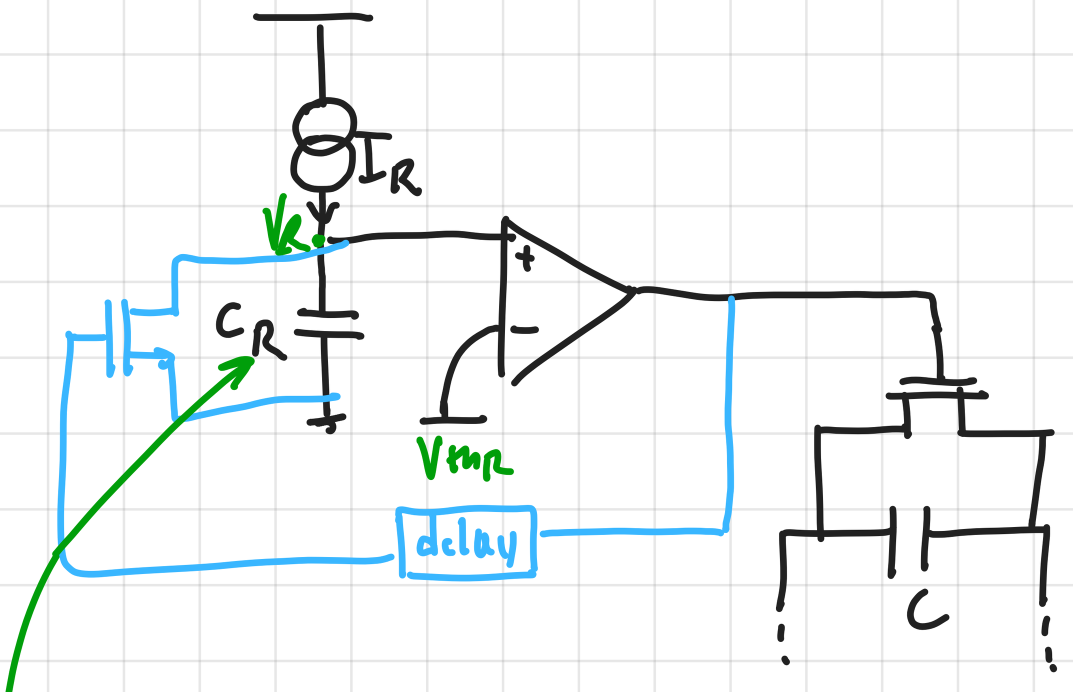
$$I_{ph} = C\,\frac{dV}{dt}$$

$$Q_{ph} = C\,\underbrace{\Delta V}_{\text{this value depends on the } V_{th} \text{ value we fix}}$$

↳ If e.g. we consider $V_{th} = 5V = \Delta V$ to turn ON the LED

$$C = \frac{Q_{ph}}{\Delta V} = \frac{2.4\,mC}{5\,V} = 480\,\mu F$$

↳ For the reset circuit we need a switch (MOS) to reset the circuit every 5 min



We can increase the value across the capacitance C_R with a const. current → charge the C_R with a const. current
↳ when the value $V_R > V_{thR}$ the comparator reset the circuit

↳ then we need to reset also C_R → branch with delay with a switch to reset also C_R → so when we reset C we then also reset C_R

↳ Now we can compute the values:

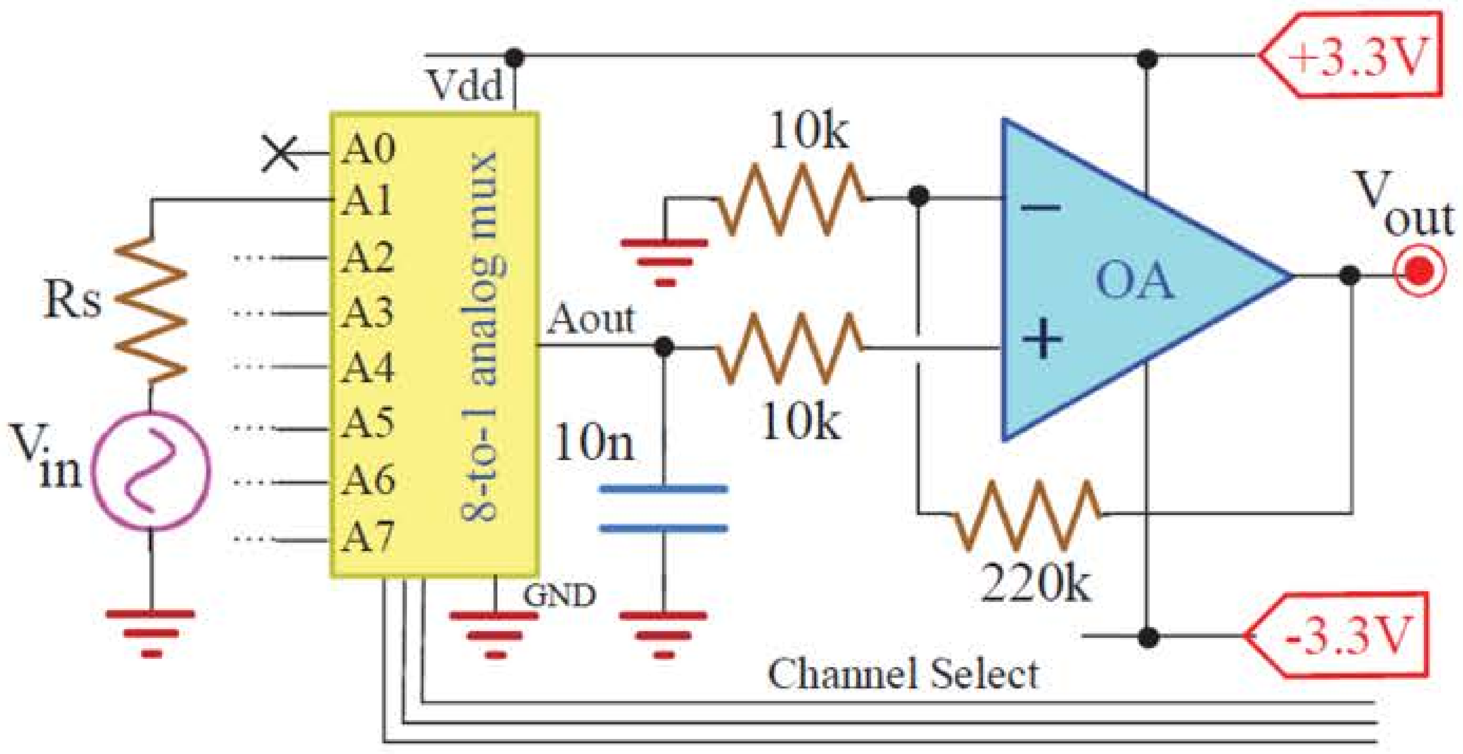
$$\frac{\Delta V_R}{\Delta t} = \frac{I_R}{C_R} \longrightarrow \frac{I_R}{C_R} = \frac{5V}{5 \cdot 60s} = 16.67\ \frac{mV}{s}$$

→ $I_R = 167\ \mu A$

→ $C_R = 100\ \mu F$

EXOS_ ES11

1



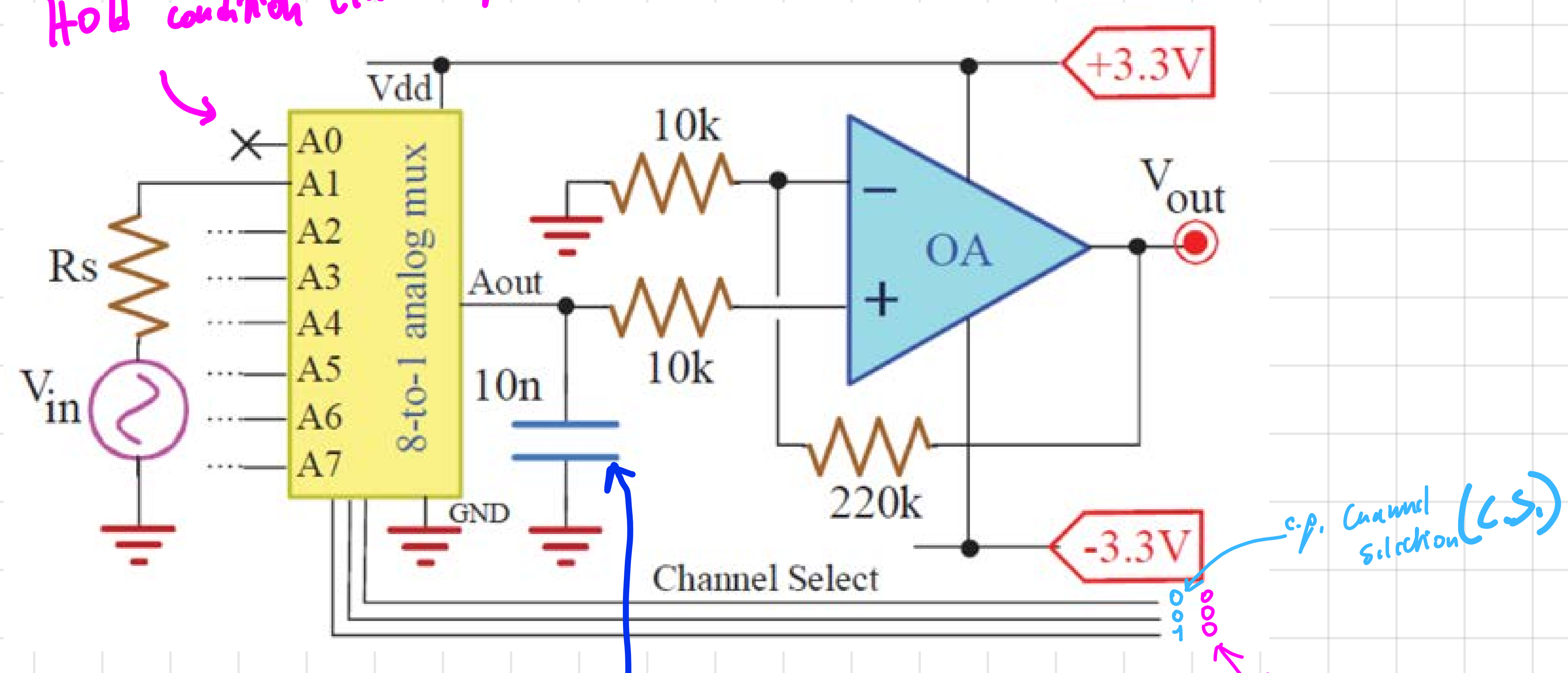
Worst case conditions

Seven inputs with R_s=100Ω-1kΩ. OpAmp with sourcing I_B=1nA and V_{OS}=0.2mV. Mux with R_{on}=5-50Ω R_{off}=2MΩ-20MΩ and I_{leak}=5nA.

a) Compute **sampling** and **hold** times for 12 bit resolution and $V_{in,max}$=±50mV and specify if they are max or min values.

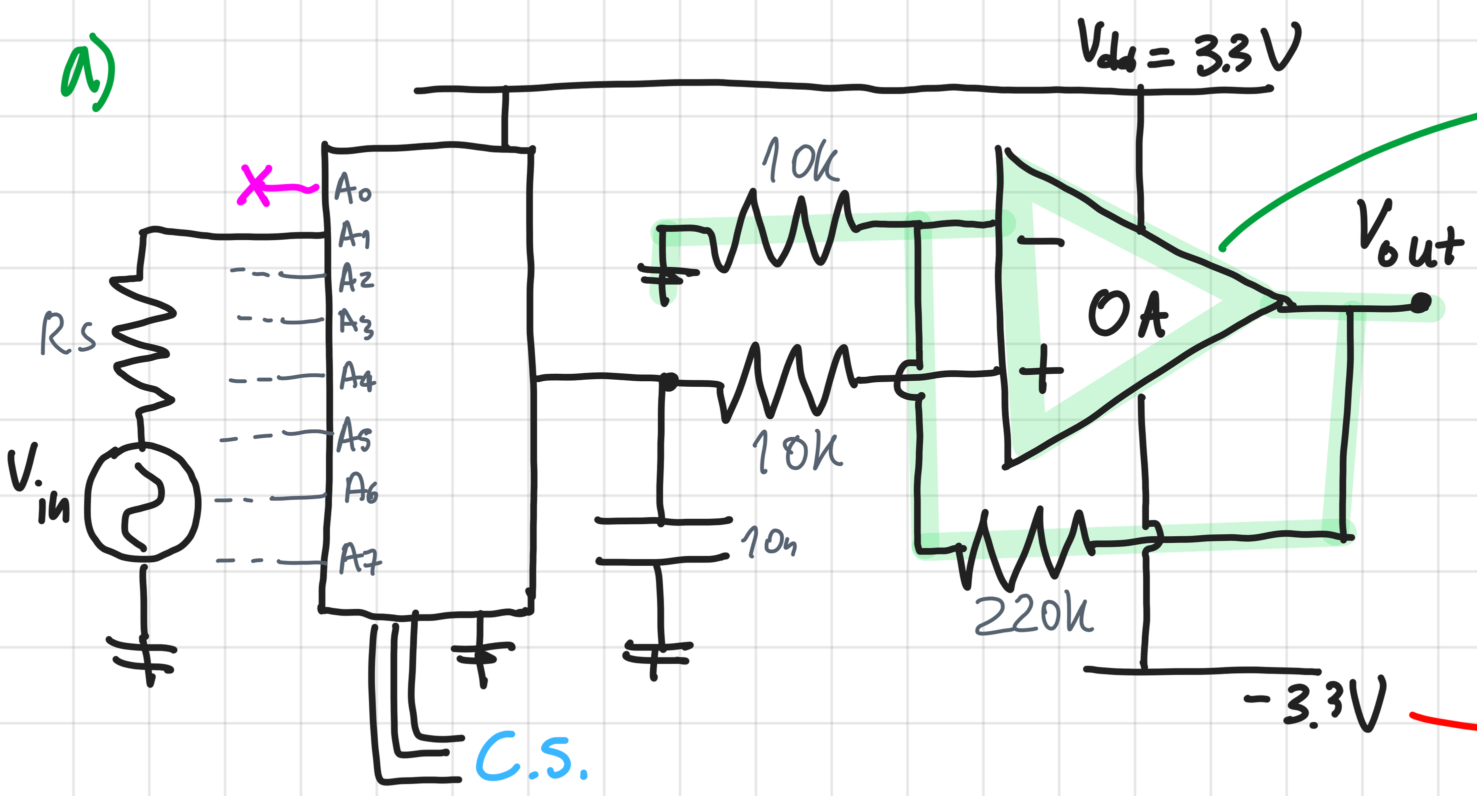
b) Compute all static errors and properly add them to compute the total output error in LSBs.

→ Hold condition (the capacitor is left floating)



the capacitor will work as a S&H where the S and H phases are commanded directly with the switches from the MUX

a)



Gain OpAmp: The OpAmp is connected in a std non-inverting config.

$$G_{OA} = 1 + \frac{R_2}{R_1} = 1 + \frac{220k}{10k} = 23$$

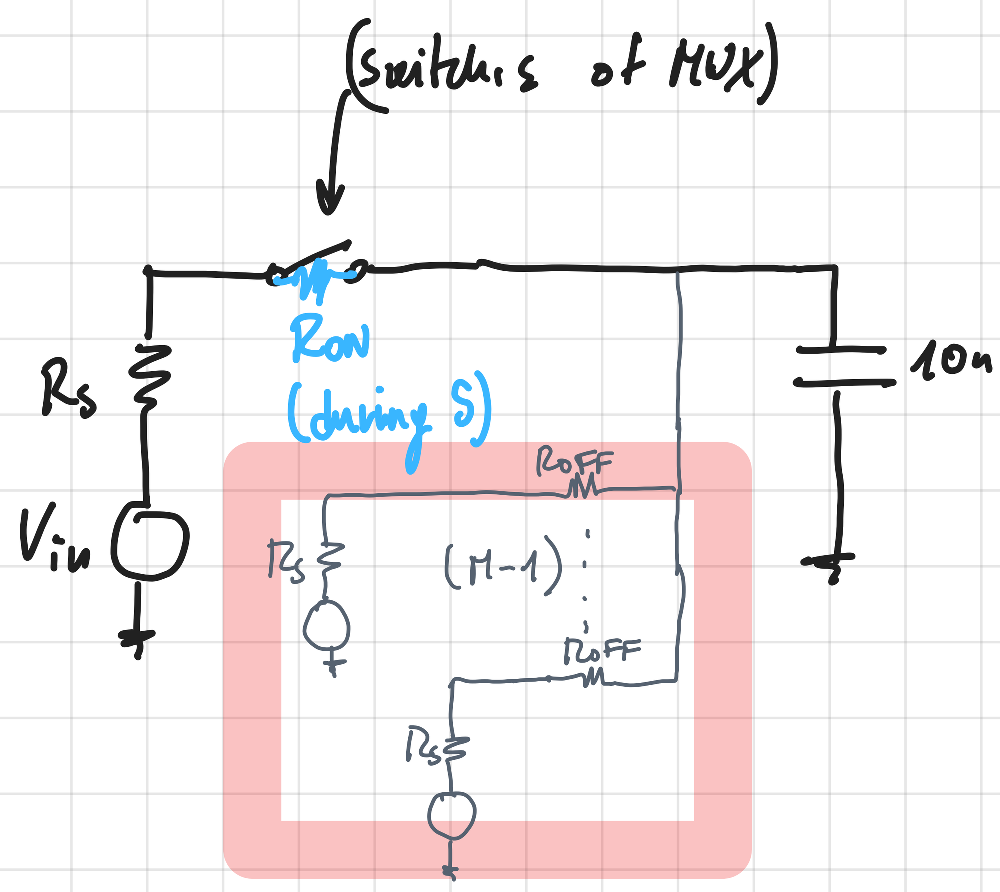
↳ $V_{out,max} = \pm V_{in,max} \cdot G = \pm 50mV \cdot 23 = \underbrace{\pm 1.15 V}_{\text{output swing}}$

$FSR = 2 \cdot 3.3V = 6.6V$

↳ $LSB = \frac{FSR}{2^n} = \frac{6.6V}{2^{12}} = \frac{6.6V}{4096} \cong 1.6\ mV$ (n: 12 bit)

The constraints

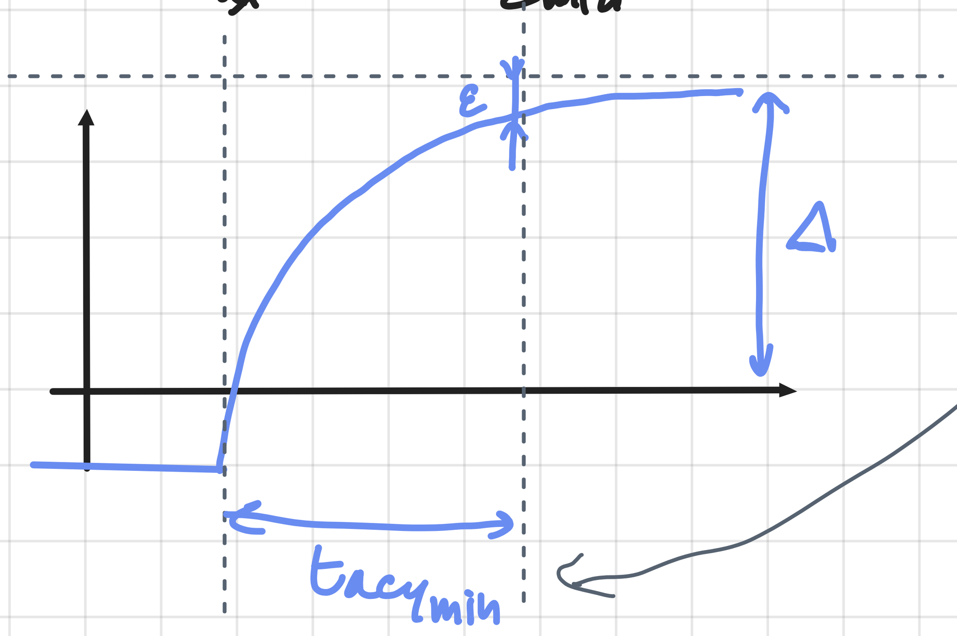
Consider the S&H circuit:



M=7

It may seem misleading but with this $|_{max}$ we indicate the max constraint which in case of acquisition time the max extreme constraining condition is $t_{acq,min}$

$$\rightarrow t_{acq}\Big|_{max} = \tau_{max} \ln \frac{\Delta_{max}}{\varepsilon_{min}}$$

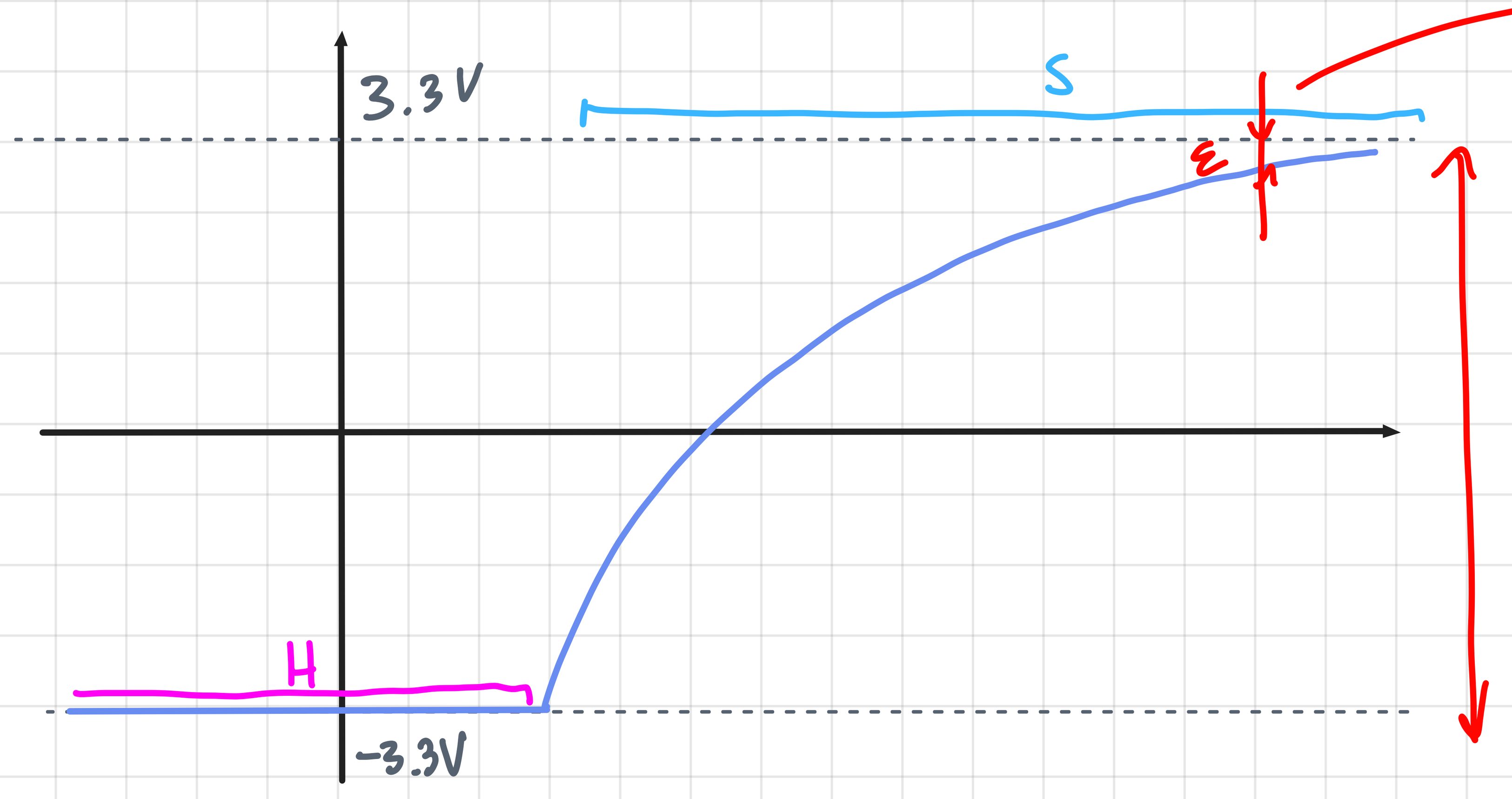


↳ Considering also the effect of the other switches (that are OFF) and the C component tollerance:

$$t_{acq\,min} = \tau_{MAX} \ln \frac{\Delta_{max}}{\varepsilon_{min}} = \left[\left(R_{s\,max} + R_{on\,max}\right) // \underbrace{\frac{\left(R_{OFF} + R_s\right)}{6}}_{\text{negligible}}\right] C\,(1 + toll.) \cdot \ln \frac{\Delta_{max}}{\varepsilon_{min}}$$

$R_{s\,max}$: 1kΩ, $R_{on\,max}$: 50Ω, C: 10n, toll.: 0.2

↳ For Δ_{max} and ε_{min} we can consider:

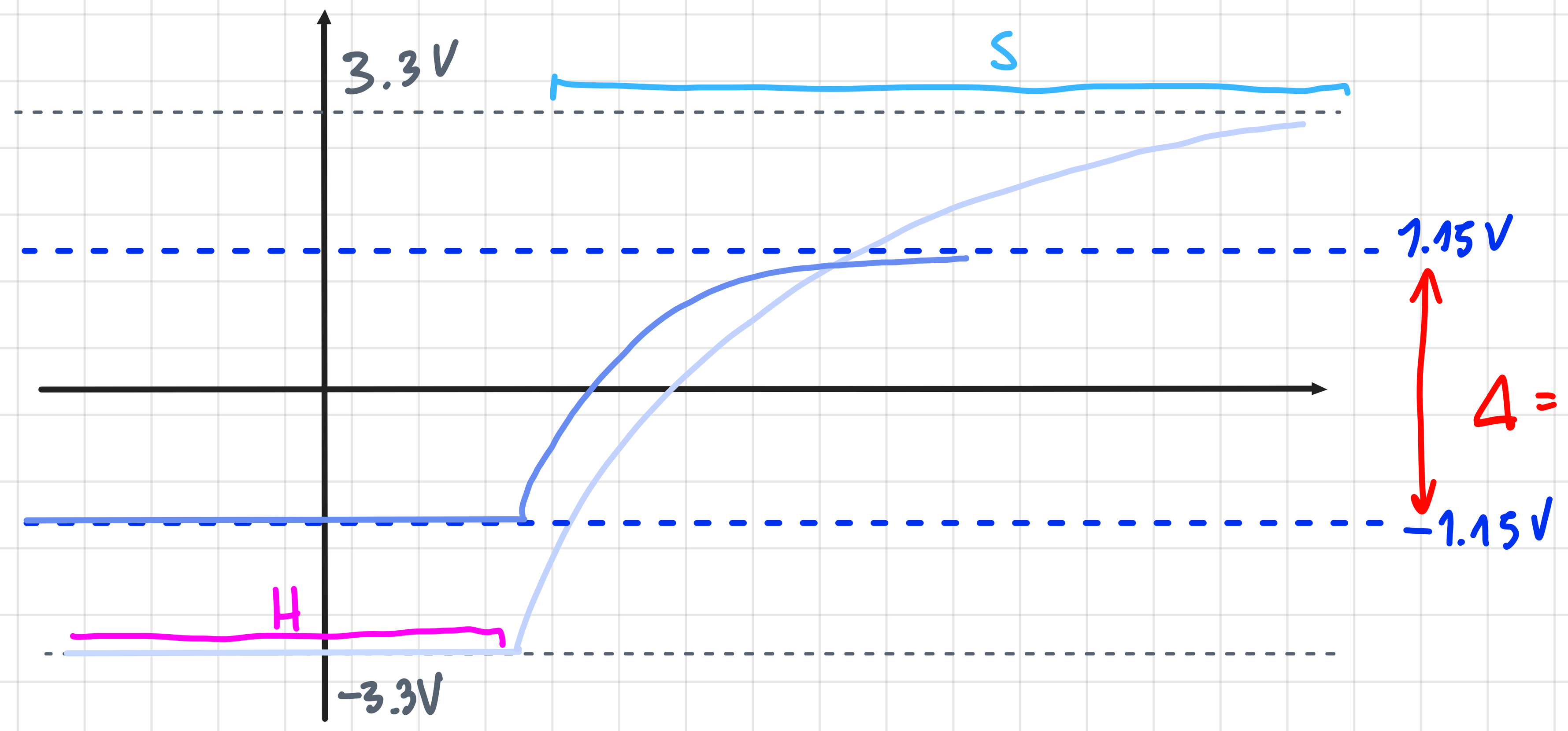


$\varepsilon = \frac{LSB}{2}$ (minimum) → $\varepsilon = \frac{1.6mV}{2} = 0.8mV$

worst case
$\Delta_{max} = FSR$

→ MOST CONSERVATIVE SOLUTION for t_{acq}

→ Instead of this most conservative solution we would like to consider the actual output swing of ± 1.15V



$\Delta = 2 \cdot 1.15V = 2.3V$

error on the output

$\left(\varepsilon = \frac{LSB}{2}\right)$

we must consider them at the same node

Δ on the output

we bring it to the node of C by dividing it by G

$$\begin{cases} \varepsilon = \frac{LSB}{2G} \\ \Delta = \frac{2.3V}{G} \end{cases}$$

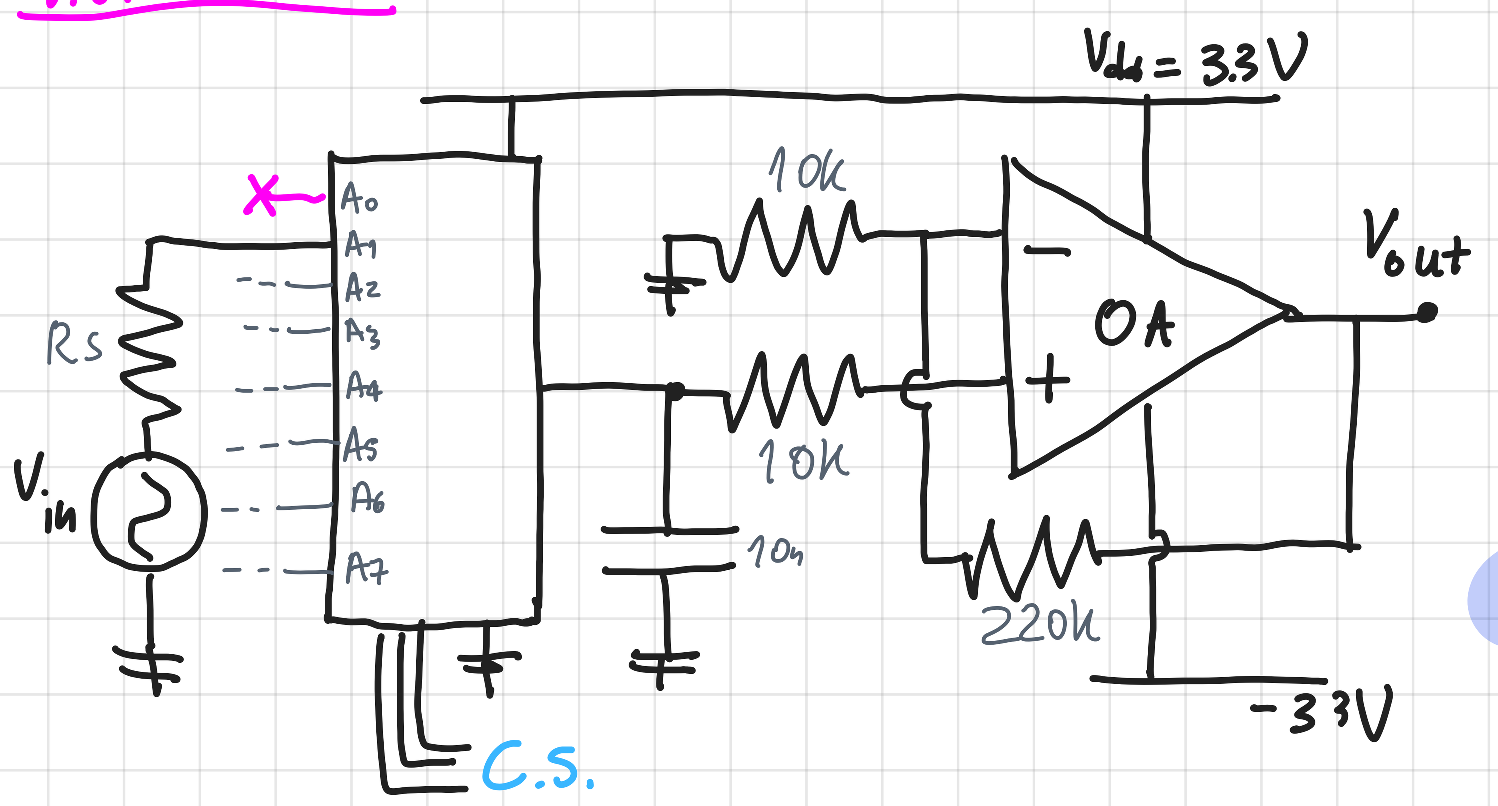
↳ So in the previous expression

$$t_{acq\,min} = \tau_{MAX} \ln \frac{\Delta_{max}}{\varepsilon_{min}} = \boxed{\left[\left(\underset{1k\Omega}{R_{Smax}} + \underset{50\Omega}{R_{ON\,max}}\right) \,//\, \overbrace{\frac{(R_{OFF} + R_S)}{6}}^{\text{negligible}}\right] \overset{10n}{C}\,(1 + \overset{0.2}{tol.}) \cdot \ln \frac{\Delta_{max}}{\varepsilon_{min}}} =$$

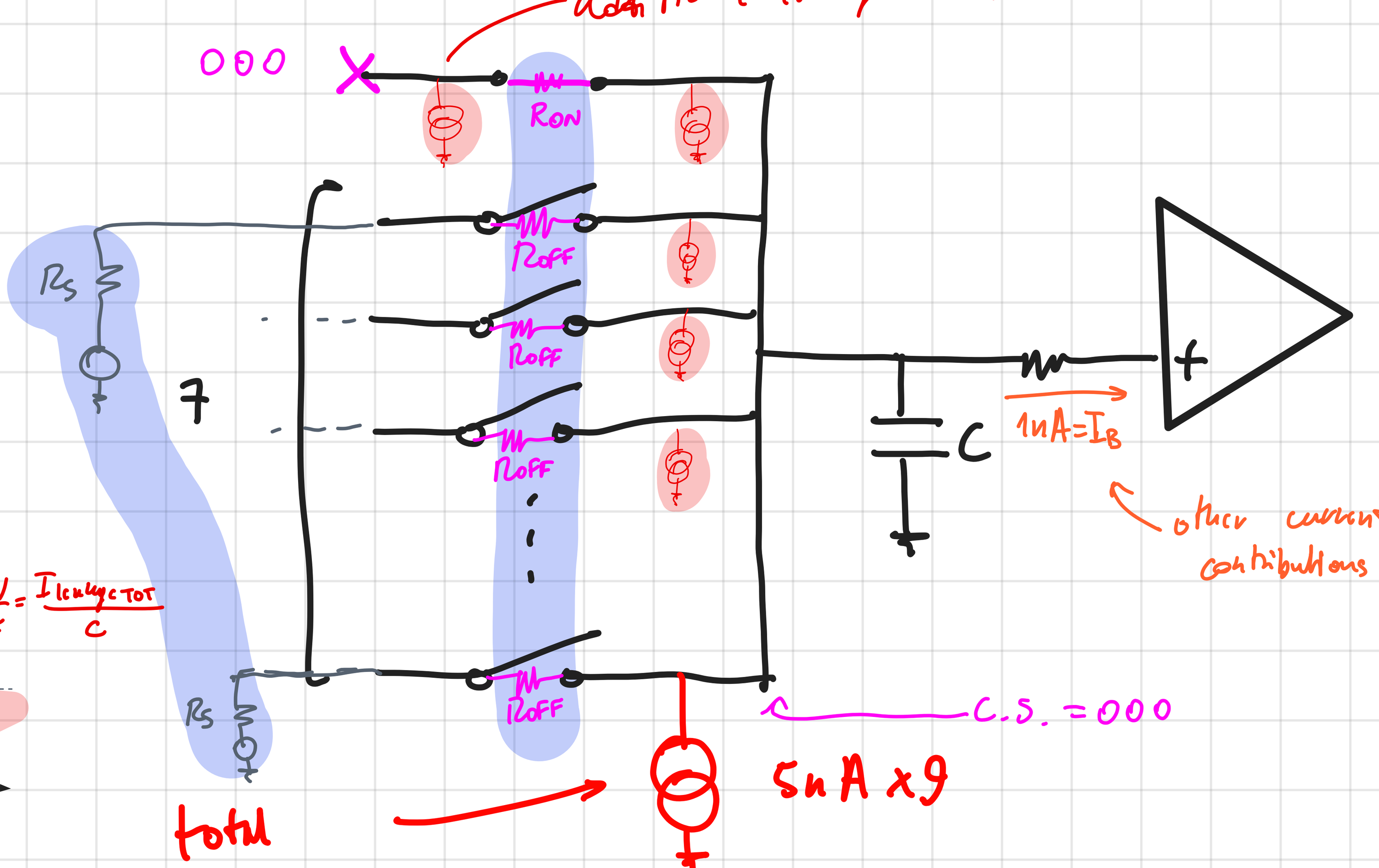
↑ SAMPLING TIME

$$= 1050\,\Omega \cdot 12\,nF \cdot \underbrace{\ln \frac{2.3\,V}{0.3\,mV}}_{7.96} \cong 100\,\mu s$$

Hold time



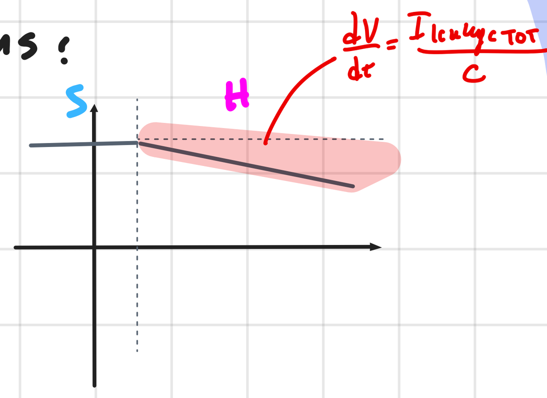
→ the first channel A0 will be connected



total leakage currents from all the 9 contributions

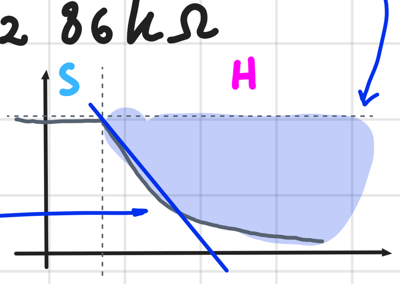
→ currents ($I_{leakage} + I_{bias}$) contributions:

$I_{leakage\,TOT} = 9 \cdot I_{leak} + I_B = 46\,nA$



→ resistors contributions → discharges C:

$R_{OFF\,min\,TOT} = \frac{R_{OFF\,min} + R_{S\,min}}{7} = \frac{2\,M\Omega}{7} = 286\,k\Omega$



to simplify let's consider a linear discharge

$\hookrightarrow I_{OFF} = \frac{V_{max}}{R_{OFFmin}} = \frac{1.15V}{286k\Omega} = 4\mu A$

for resistors

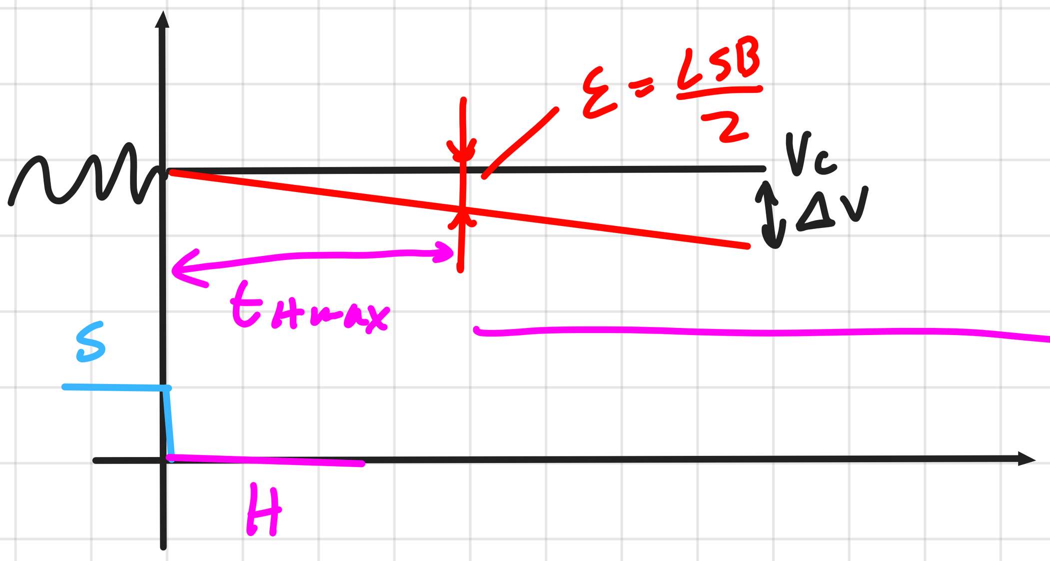
$\hookrightarrow$ So we can see that: $I_{OFF} = 4\mu A$, $I_{leakage,TOT} = 46 nA$

negligible wrt

$\hookrightarrow$ so we can define the droop rate: $droop = \left.\frac{dV}{dt}\right|_{max} = \frac{I_{OFF}}{C_{min}} = \frac{4\mu A}{8nF} = 500 \frac{V}{s}$

$(10nF)(1 - toll) = 8nF$

$\rightarrow$ For the hold time consider:



time it takes to reach an error of $\varepsilon = \frac{LSB}{2}$

$\hookrightarrow$ so for an ADC in series to the S&H we will need $t_{conv} < t_{Hmax}$

$\Rightarrow t_{Hmax} = \frac{\overset{=\varepsilon}{\Delta V}}{\frac{I_{OFF}}{C}} = \frac{\frac{LSB}{2}}{500\frac{V}{s}} = \frac{0.8mV}{500\frac{V}{s}} = 1.6\mu s$

So we discovered that:

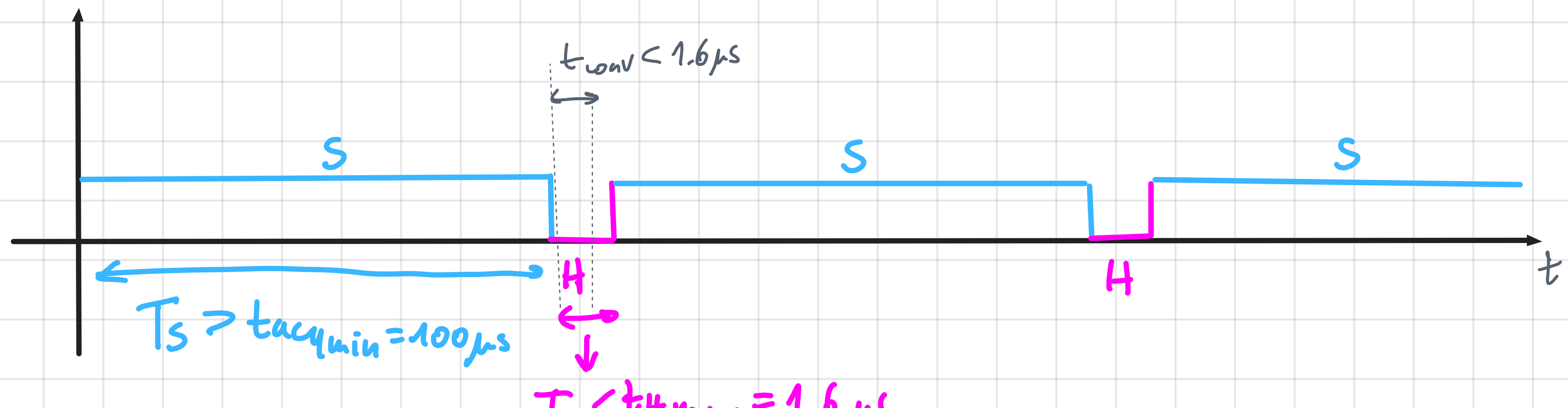
Sampling time: $t_{acq\,min} = 100\mu s$

Holding time: $t_{Hmax} = 1.6\mu s$

Pretty BAD S&H

$\hookrightarrow$ wait long with close switches (but very high speed)

f_s ⊛



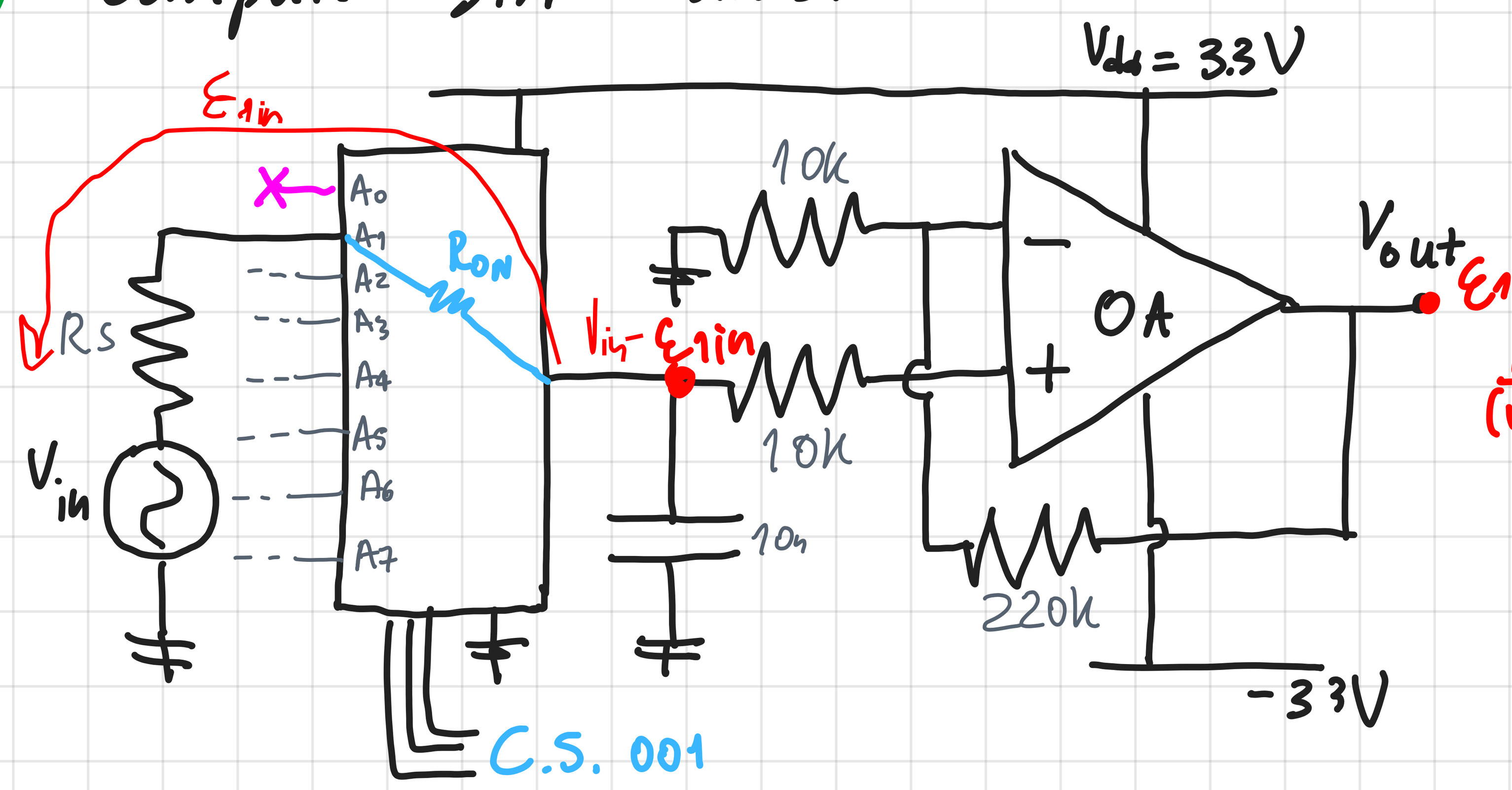
$\hookrightarrow$ expensive ADC for $t_{conv} < 1.6\mu s$

⊛ $f_s = \frac{1}{T_S + T_H} = \frac{1}{102\mu s + 1\mu s} = 9.7\ ksps$

For ex.

Bandwidth (Shannon): $f_{max} \le \frac{f_s}{2} \le 4.7\ kHz$ (To avoid aliasing)

b) Compute static errors:



When sampling we connect one of the 7 channel btw $A_0 \rightarrow A_7$

e.g. we connect A_1 $\rightarrow$ it will have a voltage drop across $R_S + R_{ON}$

001

multiplied by gain to have it at the output

First error: (voltage drop): $\varepsilon_1 = \underbrace{V_{in}\big|_{MAX} \cdot \frac{(R_S + R_{ON})_{MAX}}{(R_S + R_{ON})_{MAX} + \left(\frac{R_{OFF} + R_S}{6}\right)\Big|_{MIN}}}_{\varepsilon_{1in}} \cdot 23 = \pm 50mV \frac{1050}{1050 + \frac{2M}{6}} \cdot 23 \cong \pm 3.6mV$

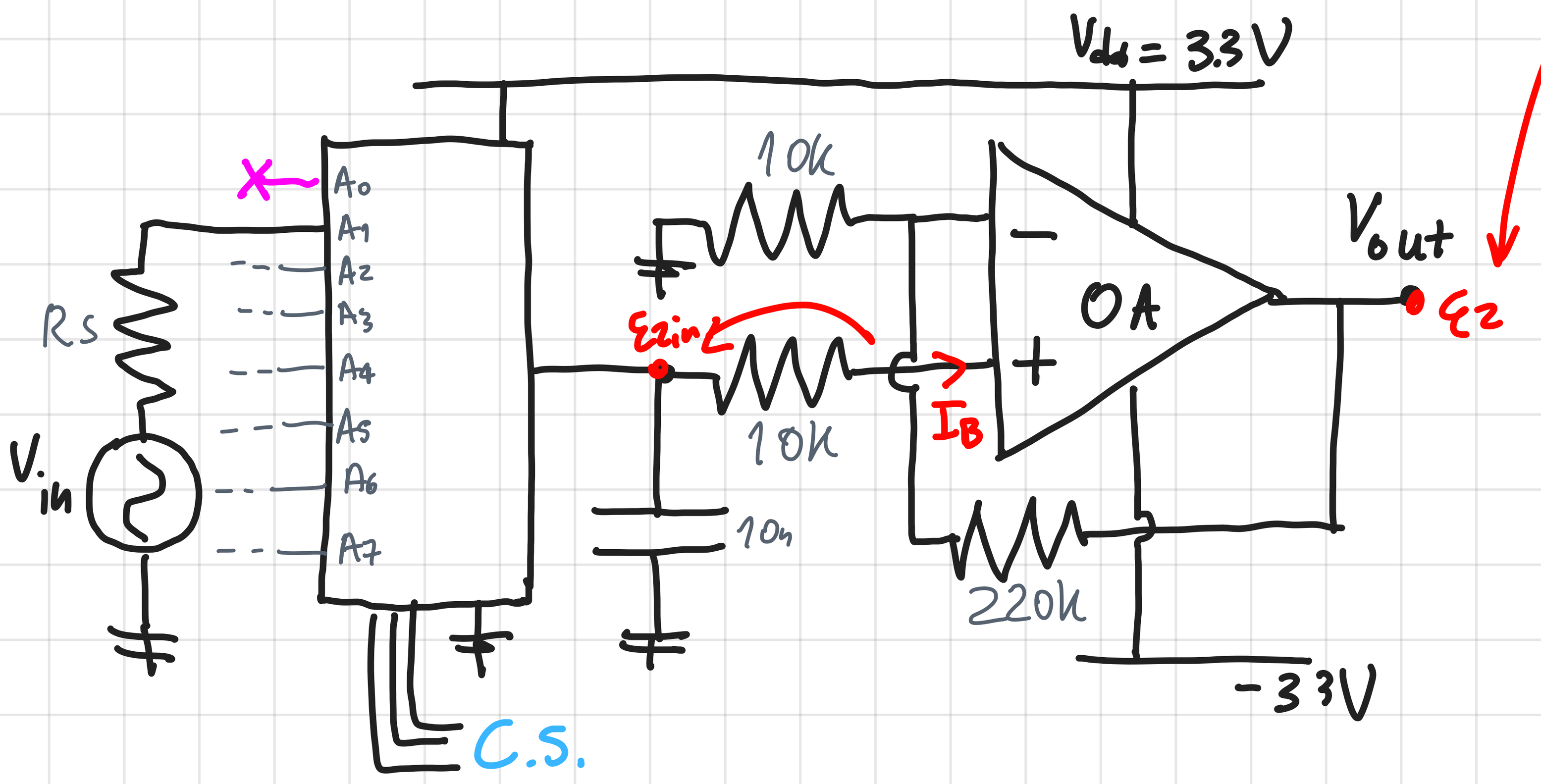
negligible

other 6 non active switches

↳ **Second error**: (Voltage drop across resistor 10Ω due to I_B)

$$\varepsilon_2 = \underbrace{-I_B \cdot 10k}_{\varepsilon_{2in}} \cdot \underset{\uparrow}{G} = -1n \cdot 10k \cdot 23 = -230\,\mu V$$

at the output



↳ **Third error**: (voltage drops due to leakages)

$$\varepsilon_3 = (9 I_{leak} + I_B)\left[(R_s + R_{ON})\Big|_{MAX} \parallel \underbrace{\frac{(R_{OFF} + R_s)}{6}\Big|_{MAX}}_{negligible}\right] \cdot G = 46nA \cdot 1050 \cdot 23 = 1.1\,mV$$

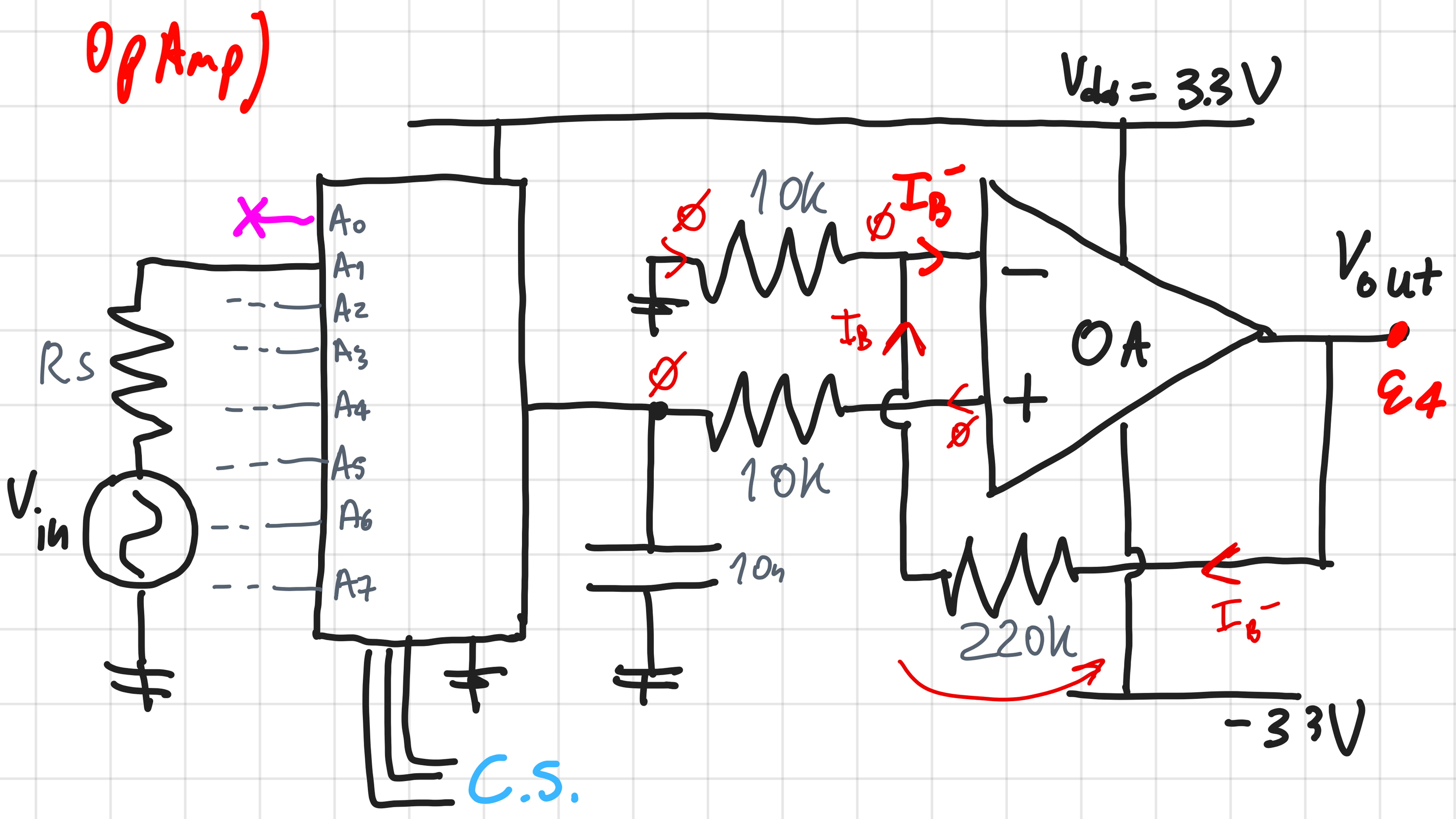
at the output

usually the sign of the leakages is not known

↳ As seen before in sampling time

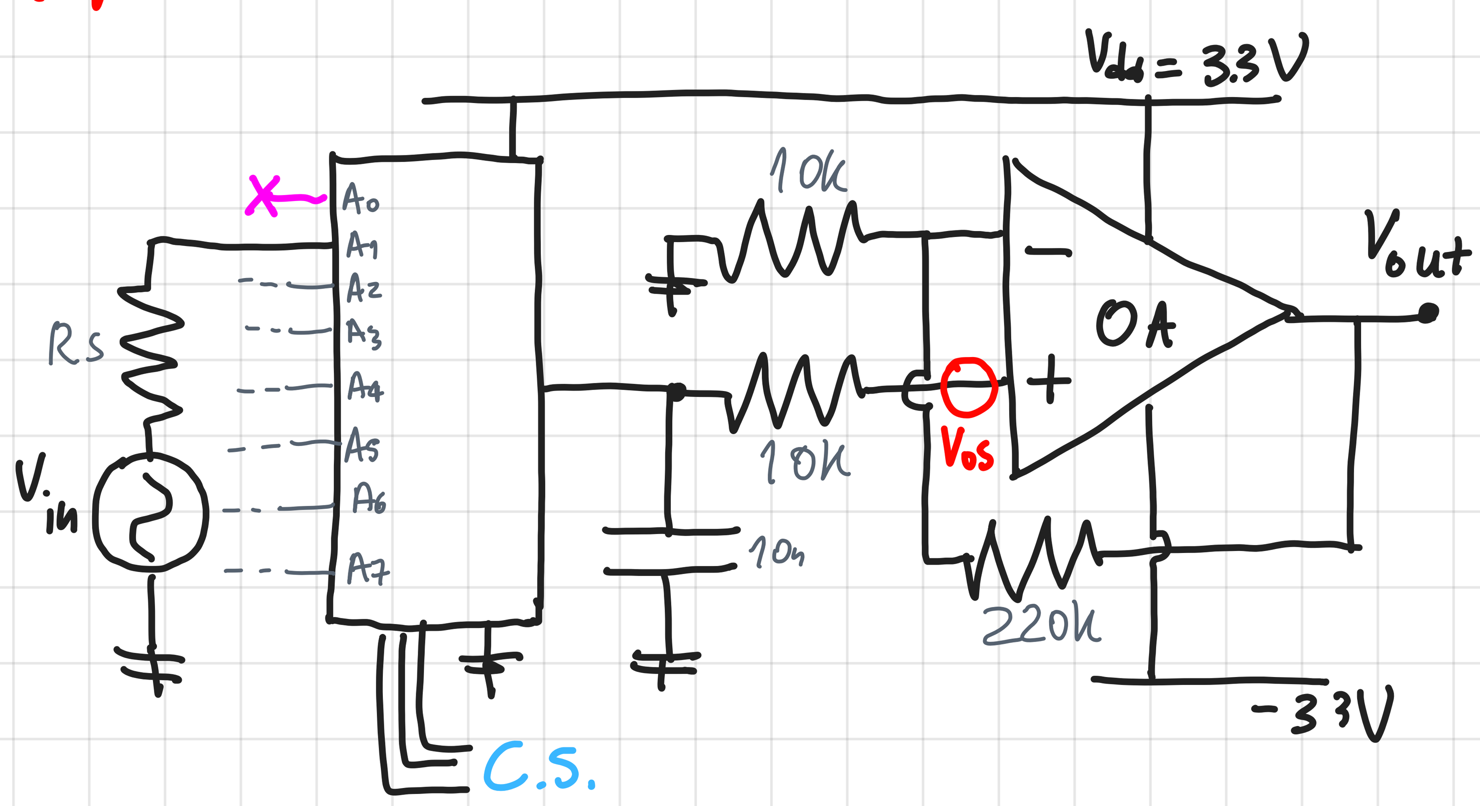
↳ **Fourth error**: (I_B^- of the OpAmp)

$$\varepsilon_4 = I_B^- \cdot 220k = 220\,\mu V$$



↳ **Fifth error**: (OpAmp offset)

$$\varepsilon_5 = \pm V_{os} \cdot G = \pm 0.2\,mV \cdot 23 = \pm 4.6\,mV$$



⟹ TOTAL ERROR at the output

$$\sum_{i=1}^{5} \varepsilon_i = \pm 3.6mV \overbrace{- 230\mu V \pm 1.1mV + 220\mu V}^{\simeq} \pm 4.6mV = \pm 9.3\,mV$$

(Prof different → wrong computation?)

Obs.
- We can try to change components to reduce this error
- Or after the ADC conversion we can try to remove this error, indeed:

Considering that:

$$\frac{9.3\,mV}{LSB} = \frac{9.3\,mV}{1.6\,mV} \cong 6 \longrightarrow D_{out} = D_{Out\,ideal} \pm 6$$

↑ digital level

(B = $11_{DECIMAL}$)

$2B_H = 0010\ 1011_B = 43_D$

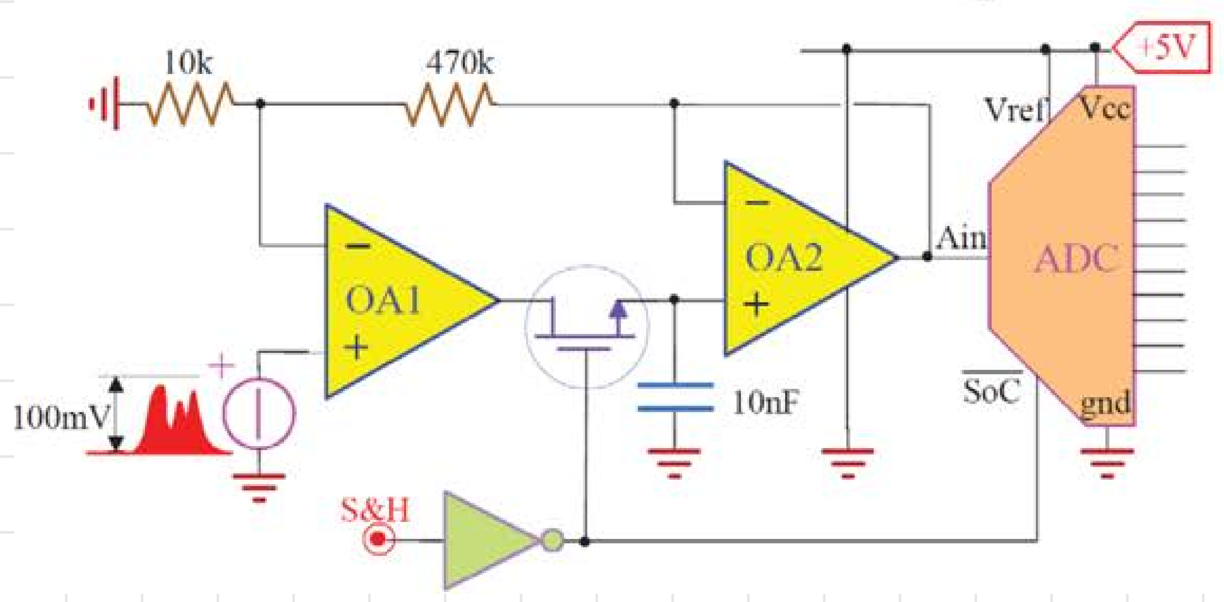
$25_H = 0010\ 0101_B = 37_D$

$31_H = 0011\ 0001_B = 49_D$

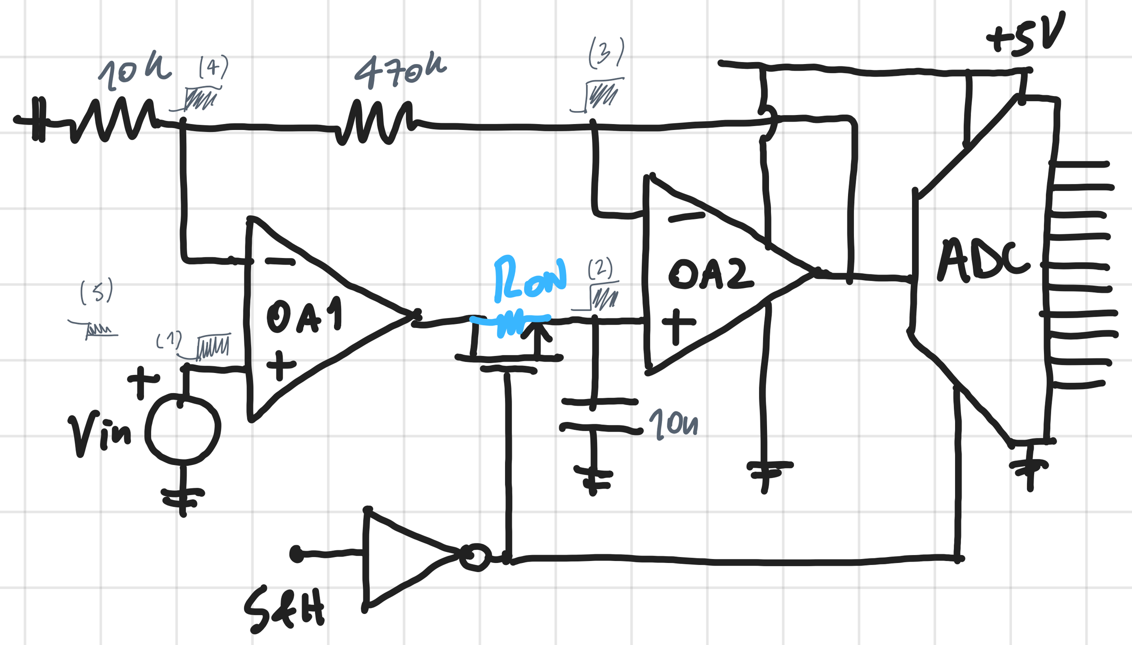
(e.g. If we're supposed to be in $2B_H$ we'll be in the range of $2B_H \pm 6 = 25_H \div 31_H$)

hexadecimal

2



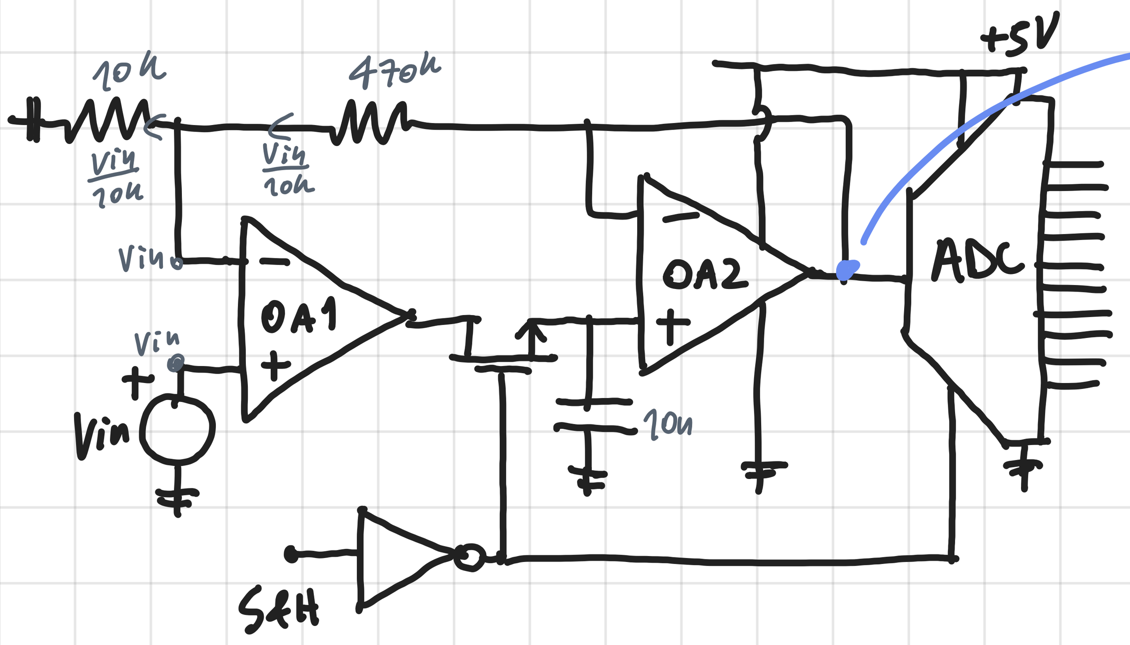
OpAmps: A_0=100dB, GBWP=100MHz.
MOS: R_{on}<100Ω, V_T=0.8V. ADC: 12bit.
a) Compute the acquisition time.
b) Compute static error on Ain in LSB, due to I_B=5nA (sink) and V_{OS}=5mV.



During sampling (S)

→ (1) → (5) (NEGATIVE FEEDBACK chain)

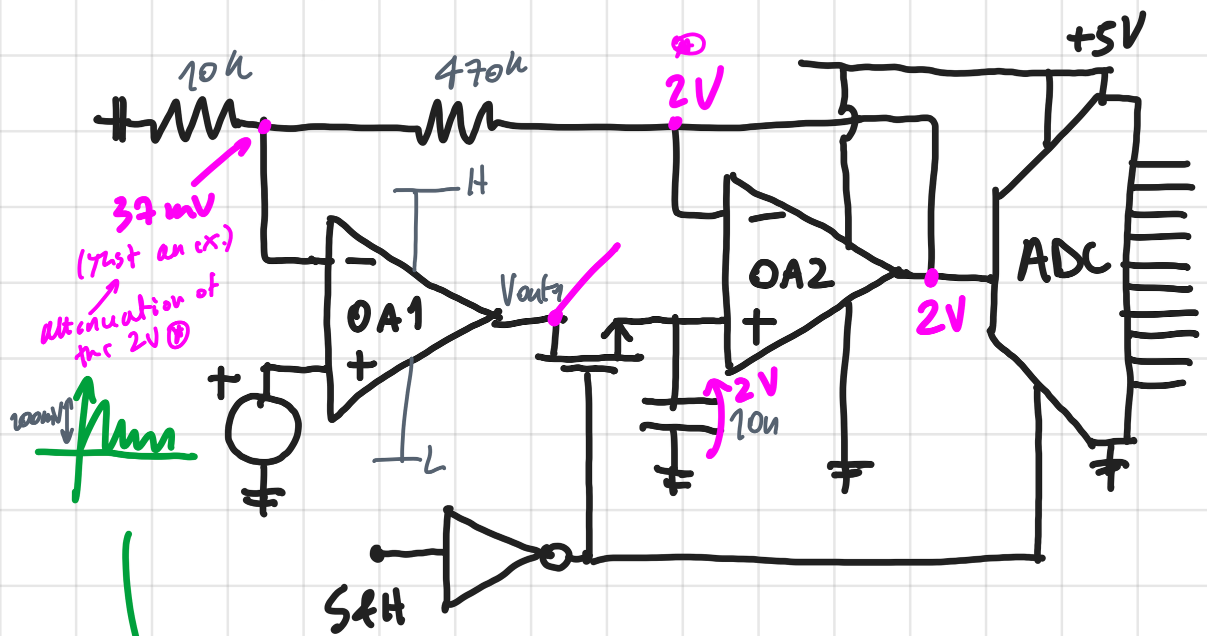
Gain



$$V_{out} = \frac{V_{in}}{10k}(10k + 470k)$$

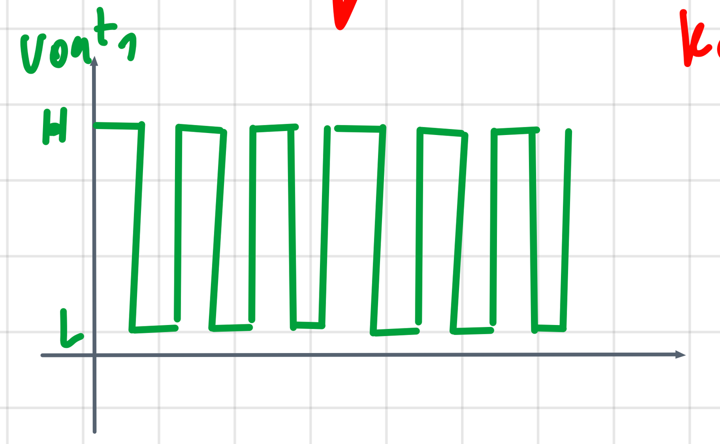
$$G = 1 + \frac{R_2}{R_1} = 1 + \frac{470k}{10k} = 48$$

a) Acquisition time



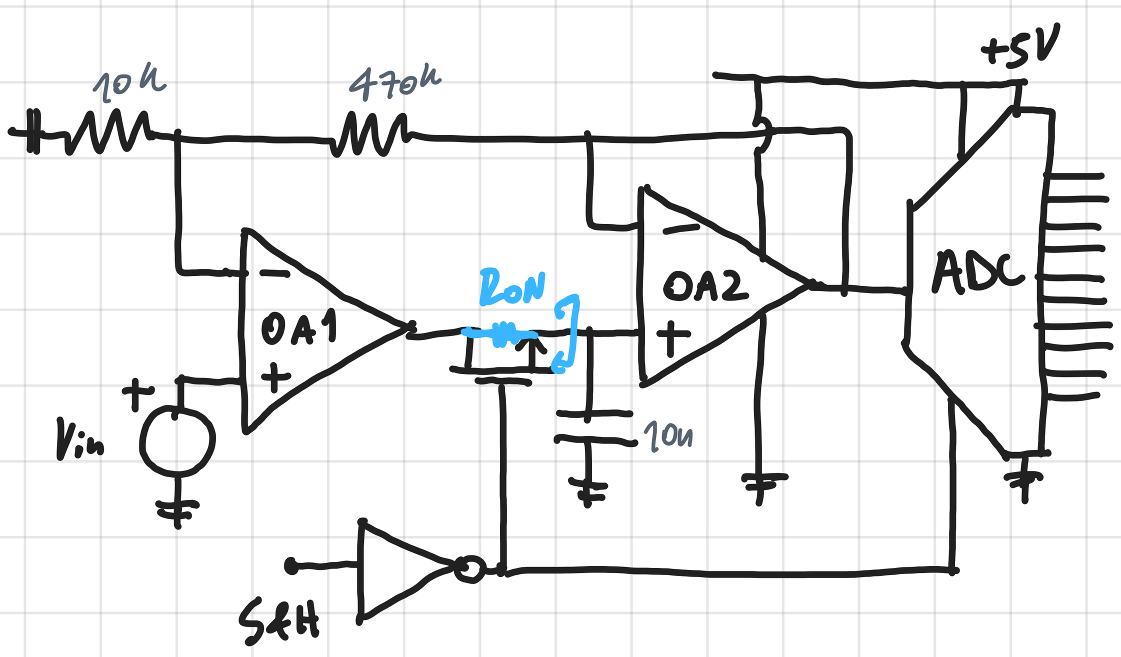
During hold phase

BAD BEHAVIOUR!
(OA1 has no feedback, switch open, so it keeps saturating btw High and Low values of P.S.)



If $V_{in} > V^-_{OA1} \Longrightarrow V_{out1}$ (H)

If $V_{in} < V^-_{OA1} \Longrightarrow V_{out1}$ (L)



During Sampling ⇒ OA1 has now feedback!

$$t_{acq} = \tau \ln \frac{\Delta}{\varepsilon}$$

$\tau \neq R_{ON}\cdot C_H$ ← 'cause we have feedback

We need to compute the BW of the closed loop config.

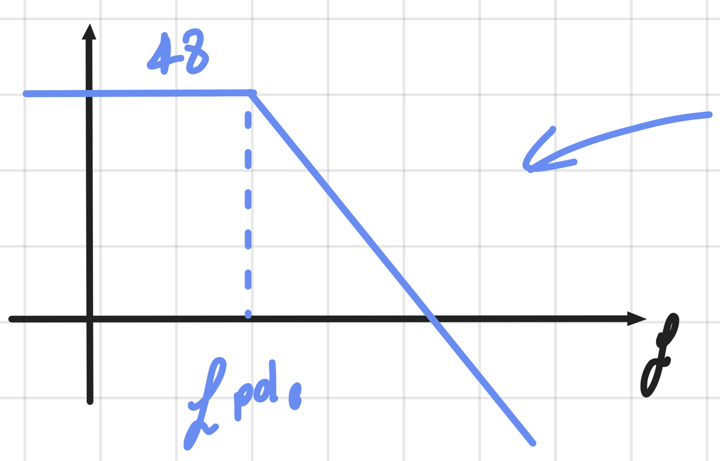
f_{pole}

$$\tau = \frac{1}{2\pi f_{pole}}$$

Since we have a feedback circuit C sees an $R_{eq} = \frac{R_{ON}}{1-G_{loop}}$ → $f_{pole} = \frac{1}{2\pi C \frac{R_{ON}}{1-G_{loop}}}$

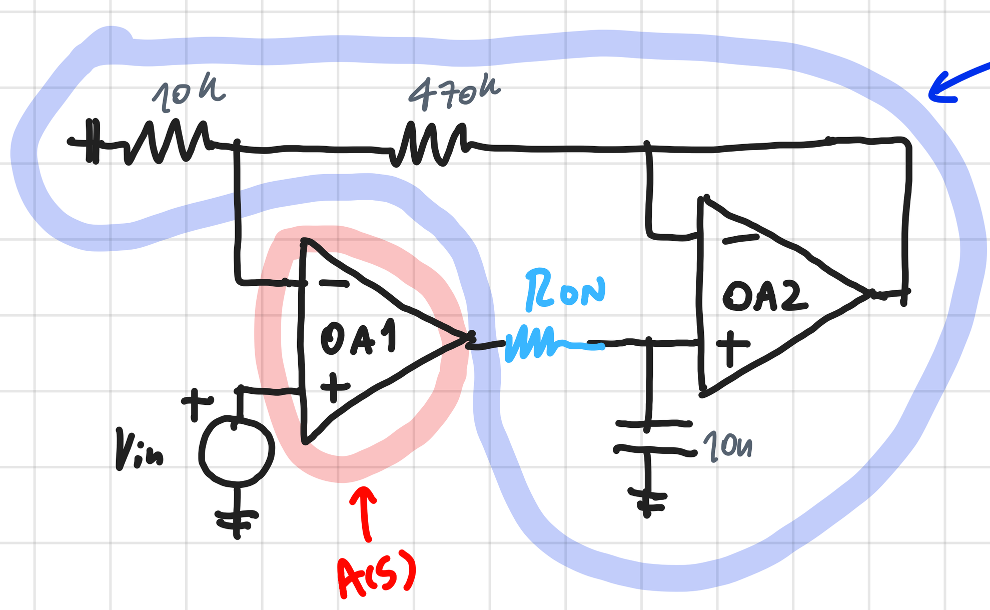
better to study the gain directly in the total Bode diagram →

Bode:



ideal gain

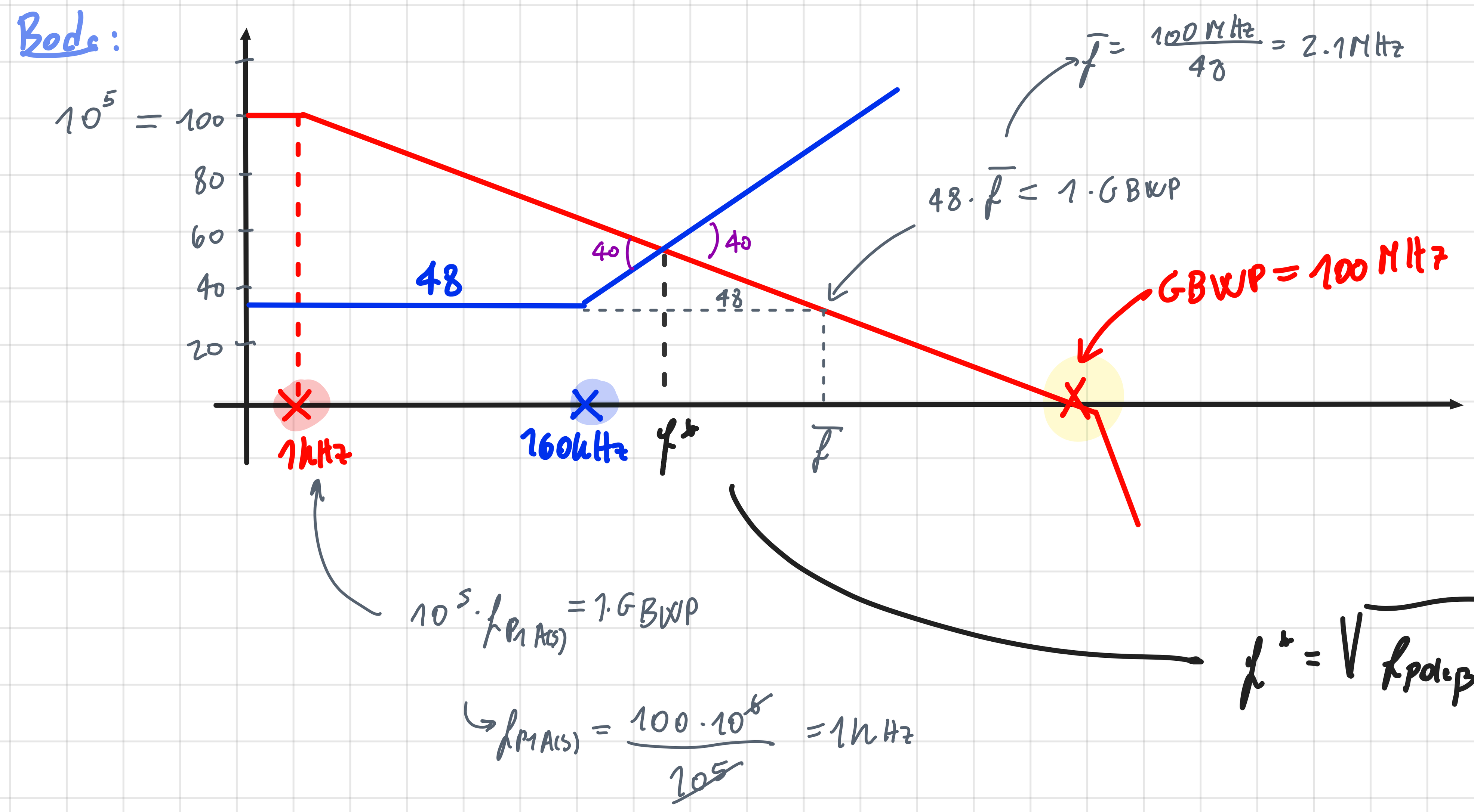
Consider:



- $\beta(0) = \frac{10k}{10k+470k}\cdot \underset{\text{buffer}}{1}$ → $\frac{1}{\beta}(0) = 48$
- $\beta(\infty) = \emptyset$ → $\frac{1}{\beta}(\infty) = \infty$

$$f_{pole_\beta} = \frac{1}{2\pi R_{ON} C} = 160kHz$$

Bode:

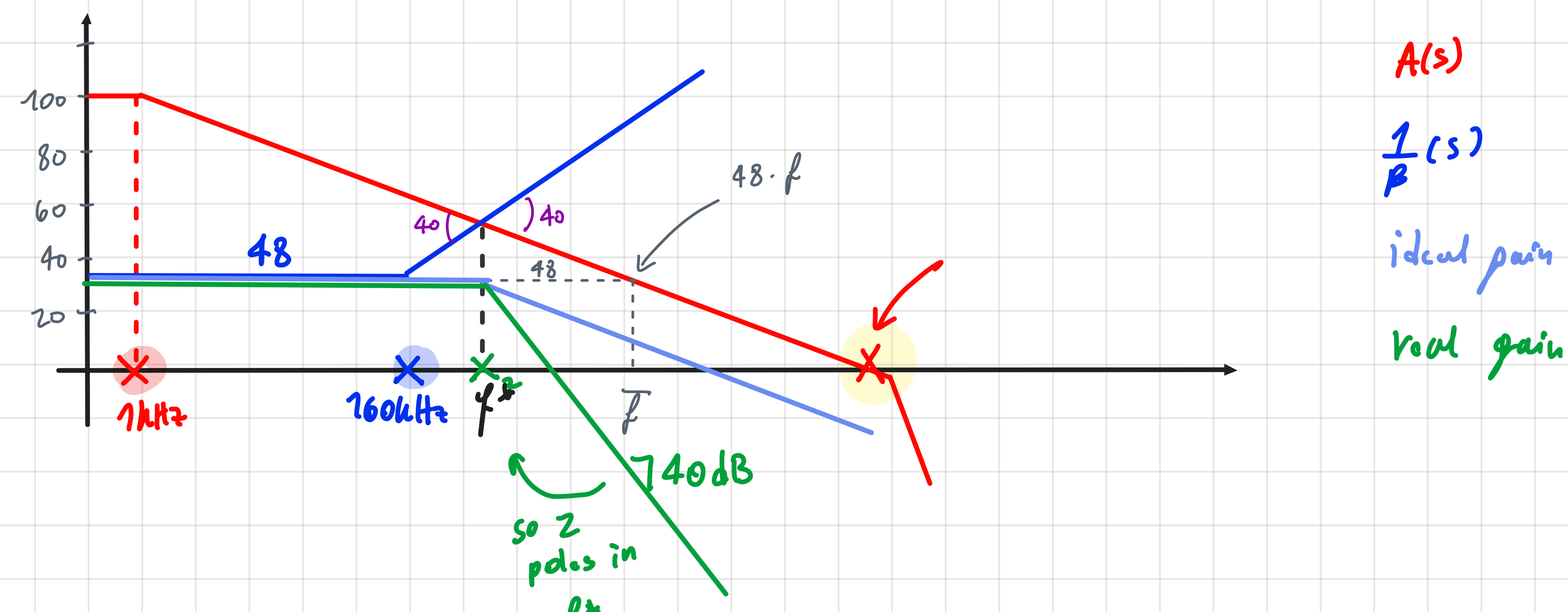


$$f^* = \sqrt{f_{pole\beta} \cdot \bar{f}} = \sqrt{160\,kHz \cdot 2.1\,MHz} = 580\,kHz$$

The closure angle is 40-40 but f^* is near 160kHz but maybe we're not already unstable:

↳ compute the $PM = 180° - 90° - \arctan\frac{f^*}{160\,kHz} - 0 = 90° - \arctan\frac{f^*}{160\,kHz} = 15°$ ⟶ too low → circuit is UNSTABLE

↳ Let's avoid compensation in this case, and just analyze the real gain response:

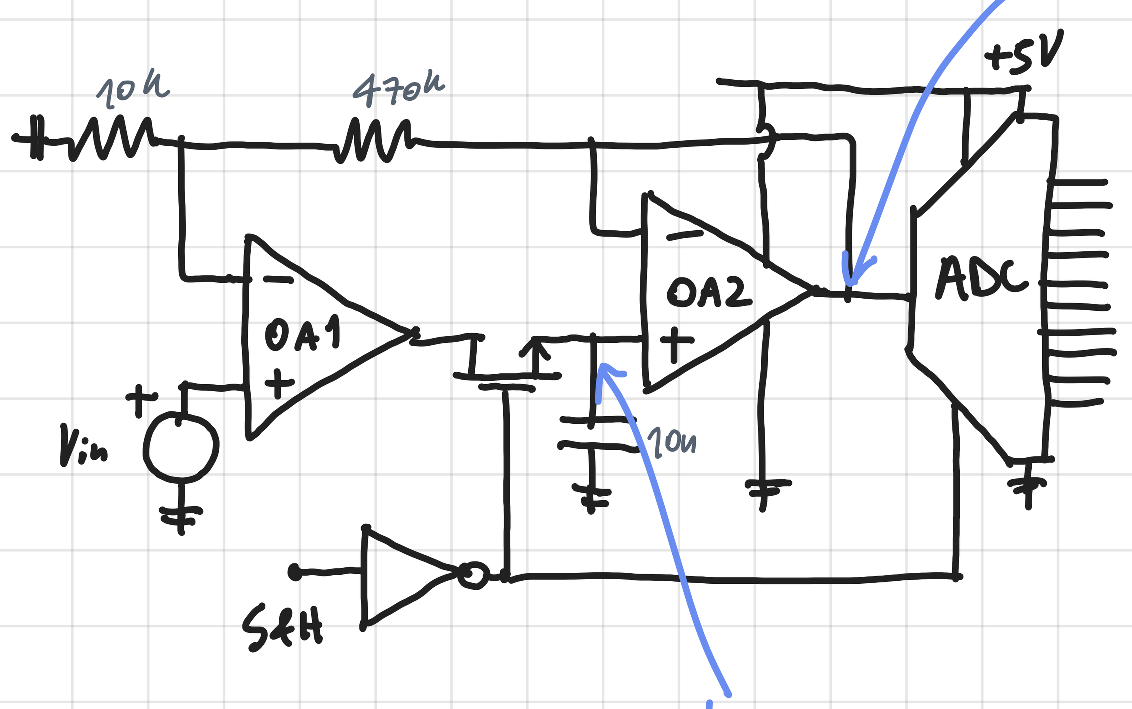


so 2 poles in f^* (unstability) ⟶ we can't realistically say that: $\tau = \frac{1}{2\pi f^*}$

↳ But we make an approx. $\tau \simeq \frac{1}{2\pi f^*} = \frac{1}{2\pi \cdot 580k} = 275\,ns$ (At the written test it will specify if we can use this approx.)

↳ $t_{acq} \simeq \tau \ln \frac{\Delta}{\varepsilon} =$

For Δ and ε consider:



- FSR = 5V (from P.S. 0–5V)
- $LSB = \frac{FSR}{2^{12}} = 1.2\,mV$ ⟵ 12 bit ⟶ $\varepsilon = \frac{LSB}{2} = 0.6\,mV$

At this node since OA2 = buffer the error is the same of the output

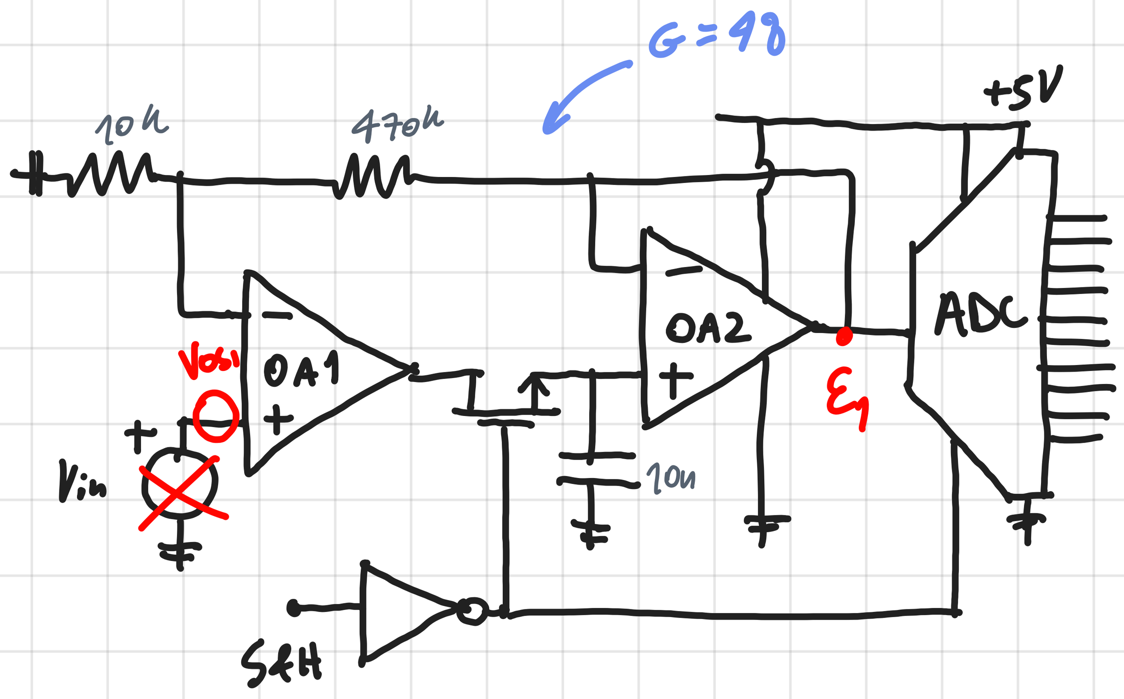
Δ: ⟶ worst case: $\Delta = 5\,V$

↳ If we instead consider the real max input of 100mV

↳ $V_{out\,max} = 100\,mV \cdot 48 = 4.8\,V \simeq 5\,V$ (we can consider this)

$$\Rightarrow t_{acq\,min} = \tau \ln \frac{\Delta_{max}}{\varepsilon_{min}} = 275\,ns \cdot \underbrace{\ln \frac{5\,V}{0.6\,mV}}_{9} = 2.5\,\mu s$$

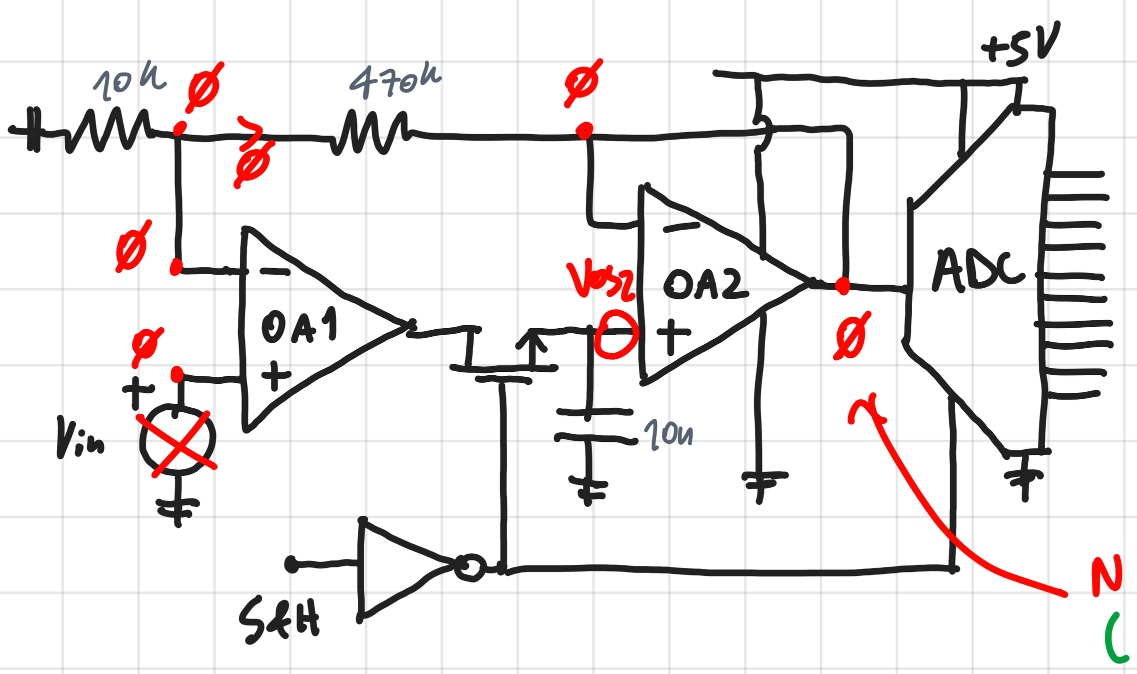
b) Computation of static errors



V_{os1} $\varepsilon_1 = V_{os1} \cdot 48 = 240\,mV! = \pm 200$ digits

e.g. $F38_H$ → $F38_H + 200$ / $F38_H - 200$ ← Very inaccurate!

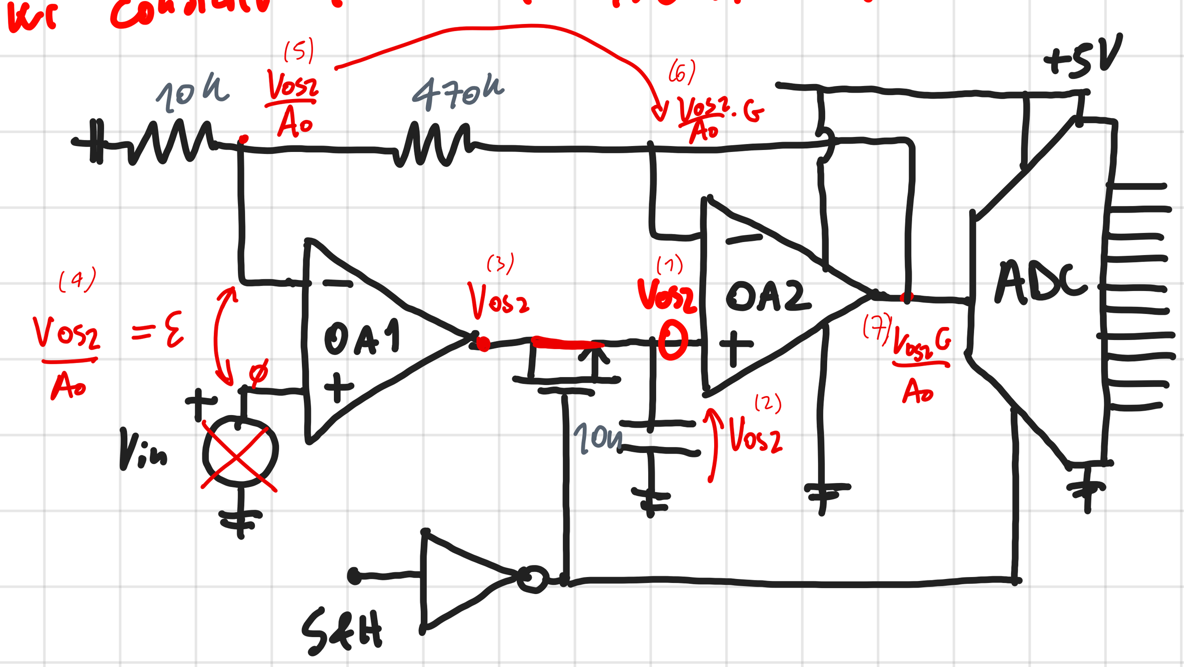
12 bit = 4x3 → 3 hexadec. digits



V_{os2} $\varepsilon_2 = 0$

NO EFFECT (ideally)

If we consider the real circuit ($\varepsilon \neq 0$)



Consideration direction:

(1) V_{os2} applied

(2) V_{os2} on C

(3) V_{os2} must be provided by OpAmp1

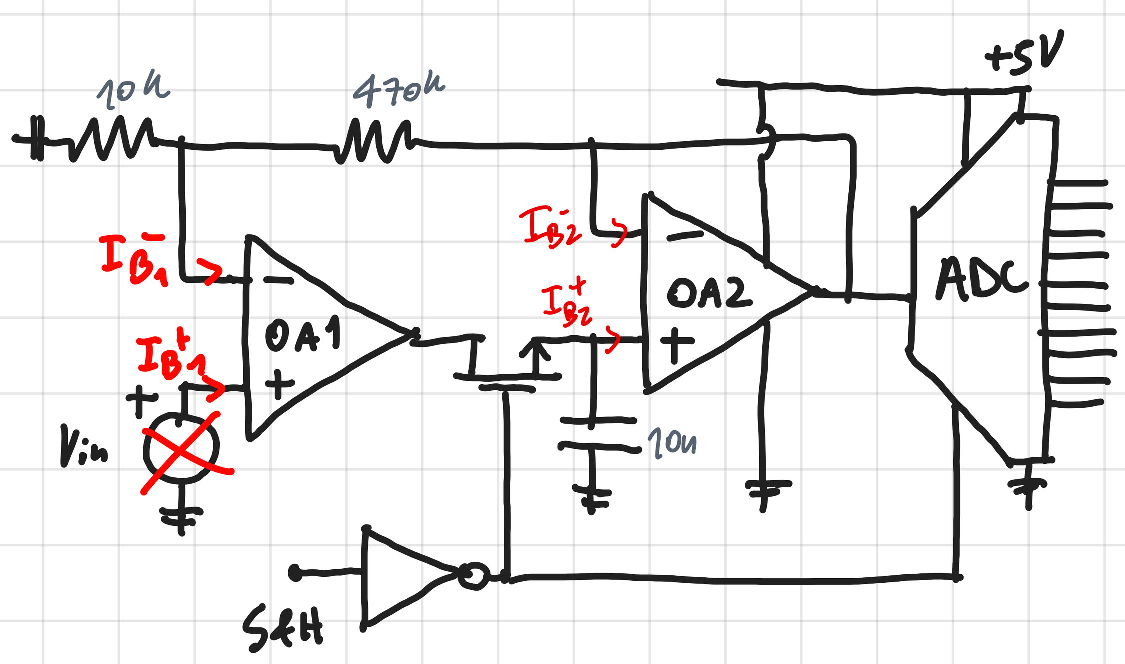
(4) To be provided $V_{out1} = V_{os2}$ it means the diff input of OA1 is $\varepsilon = \frac{V_{os2}}{A_0}$

Since $V_{o1} = \varepsilon A_0 = V_{os2}$

(5) V_{os2}/ε on the node

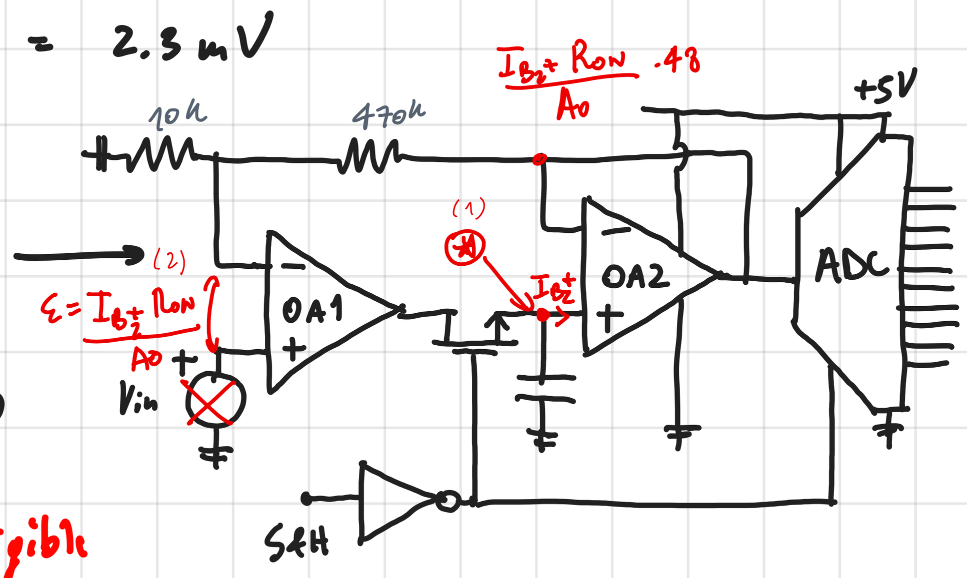
(6) $\frac{V_{os2}}{\varepsilon} \cdot G$ = (7)

→ so $\varepsilon_2 = \frac{V_{os2}}{A_0} \cdot G \cong 0$ (negligible indeed)



I_B

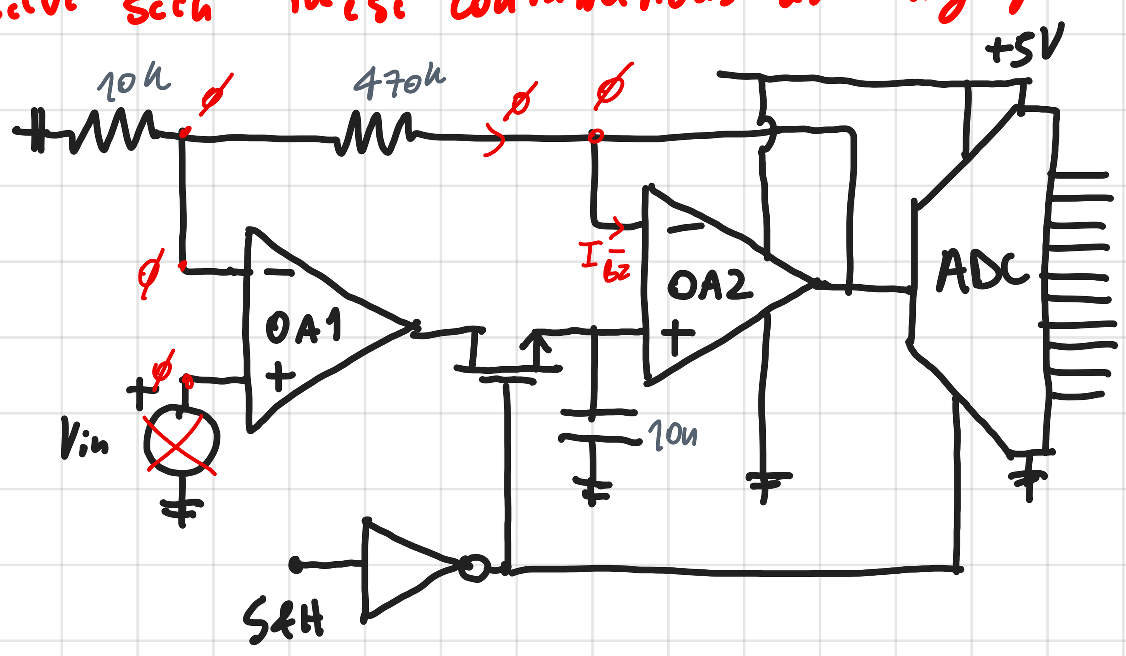
- I_{B1}^+ (no effect) $\varepsilon_3 = 0$
- I_{B1}^- → $\varepsilon_4 = I_{B^-} \cdot 470k = 2.3\,mV$
- I_{B2}^+ → (*) $I_{B2^+} \cdot R_{ON}$ →



$\varepsilon_5 = \frac{I_{B2^+} \cdot R_{ON}}{A_0} \cdot 48 \simeq 0$ ← negligible

- I_{B2}^- (no effect) $\varepsilon_6 = 0$

Ideally → but we've seen these contributions are negligible



05/12/2022

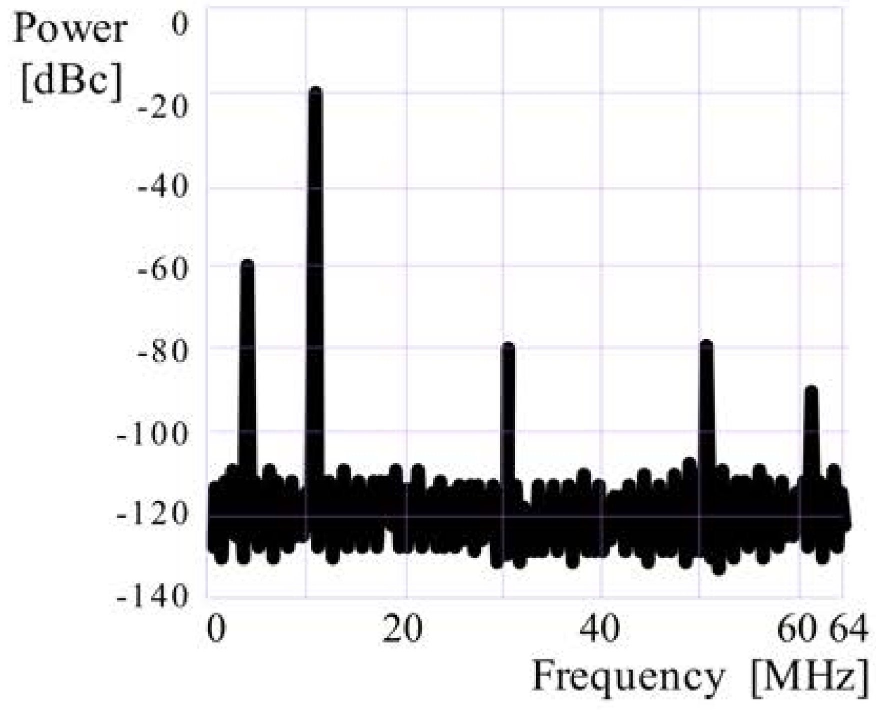
EX07_DAC

(1)

The 12bit DAC has 5V FSR. The measured output spectrum has a 2kHz bin-width. There is a distortion tone at 5MHz.

a) Compute SNR_{ideal}, SNR_{theor}, SNR_{real}, and ENOB.

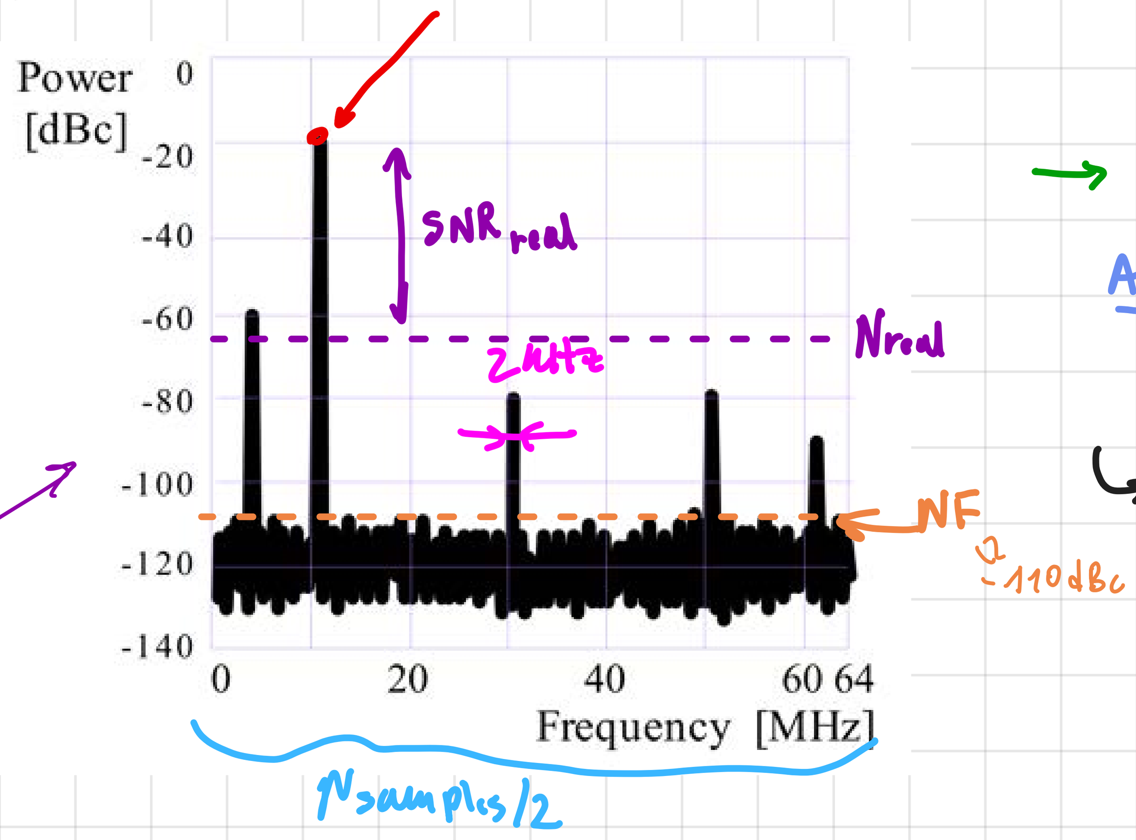
b) Compute the THD and the SiNAD.



a) $FSR = 5\,V \qquad n = 12\ bit$

→ $SNR_{ideal} = 6.02n + 1.76 = 74\,dB$

↳ But we can see here that $S_{real} \neq S_{max} = 0\,dBc$ → $S_{real} = -20\,dBc$ ('cause we take $\Delta S = (S_{max} - S_{real})_{dB} = 20\,dB$)



→ Theoretical SNR: $SNR_{th} = SNR_{ideal} - \Delta S = 74dB - 20dB = 54dB$

Attenuation: $\Delta S = 20\,dB$

↳ $N_{real} = ?$

↳ We can compute that:

$$N_{ideal} = N_{min} = N_{quantization} = \frac{LSB^2}{12} = \ldots = -SNR_{ideal} = -74\,dBc$$

↳ We know that: $\frac{f_s}{2} = 64\,MHz \qquad f_s = 2 \cdot 64\,M = 128\,M_{ps}$ ↳ bin-width $= 2kHz$

↳ $N_{samples} = \frac{f_s}{bin\_width} = \frac{128\,MHz}{2kHz} = 64k\ samples$

$$N_{real} = NF_{real} \cdot \frac{N_{samples}}{2} = -110\,dBc + 10\log_{10}\frac{N_{samples}}{2} = -110\,dBc + 45\,dB = -65\,dBc$$

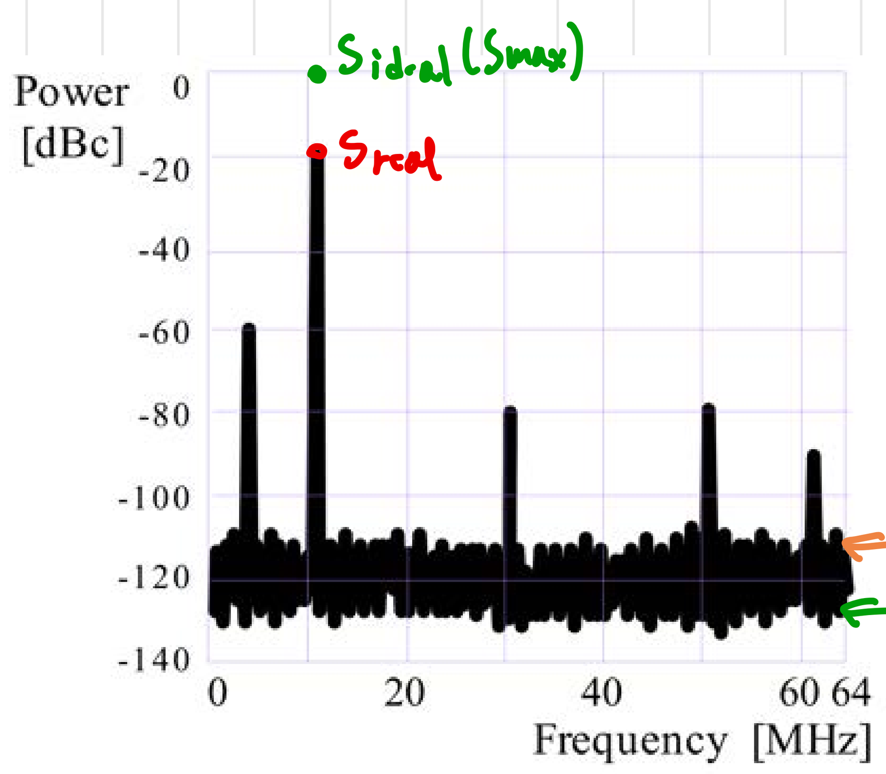
the result has the power dimension (dBc)

↳ $SNR_{real} = \frac{S_{real}}{N_{real}} = -20\,dBc - (-65\,dBc) = 45\,dB$

a ratio btw powers is a adimensional ratio → dB

↳ Then we know that: $SNR_{real} = SNR_{ideal} - \Delta S - \Delta N$ ⟶ EXTRA NOISE: $\Delta N = 74dB - 20dB - 45dB = 9\,dB$

our DAC is not ideal



→ $NF_{ideal} = \frac{N_{ideal}}{\frac{N_{samples}}{2}} = -74\,dBc - \underbrace{10\log_{10}\left(\frac{N_{samples}}{2}\right)}_{45\,dB} = -119\,dBc$

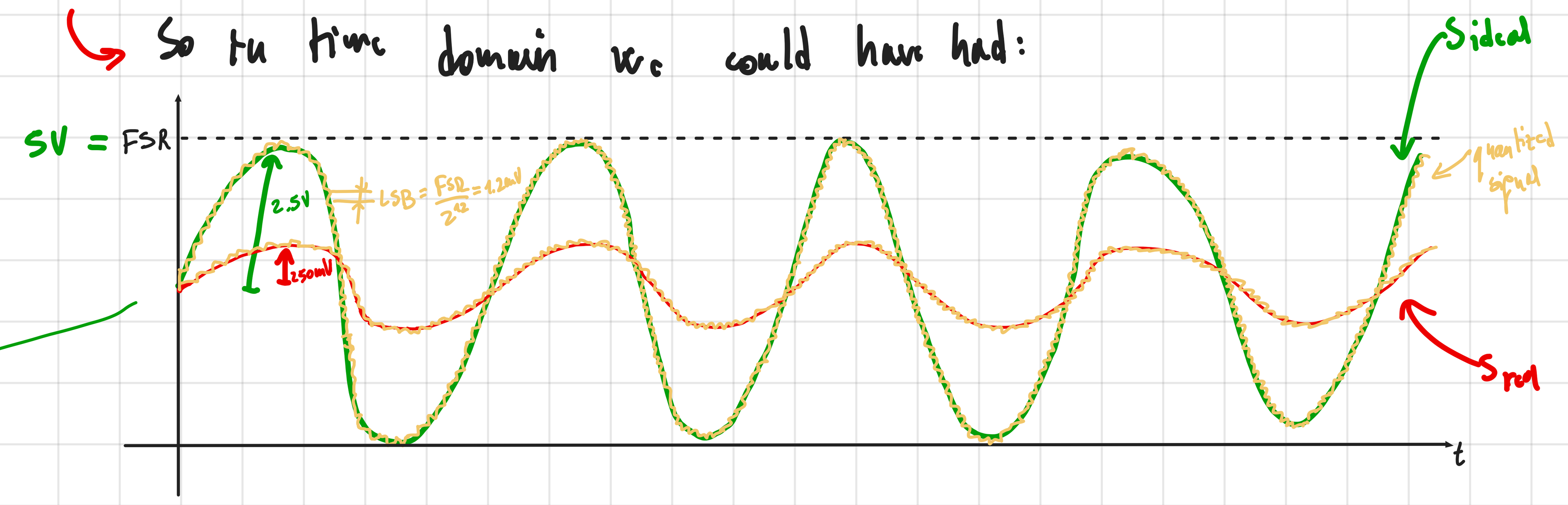
$NF = -110\,dBc$

$NF\ ideal = -119\,dBc$

$\Delta N = 9\,dB$

if we would have amplify for the all FSR

↳ So in time domain we could have had:



ideally

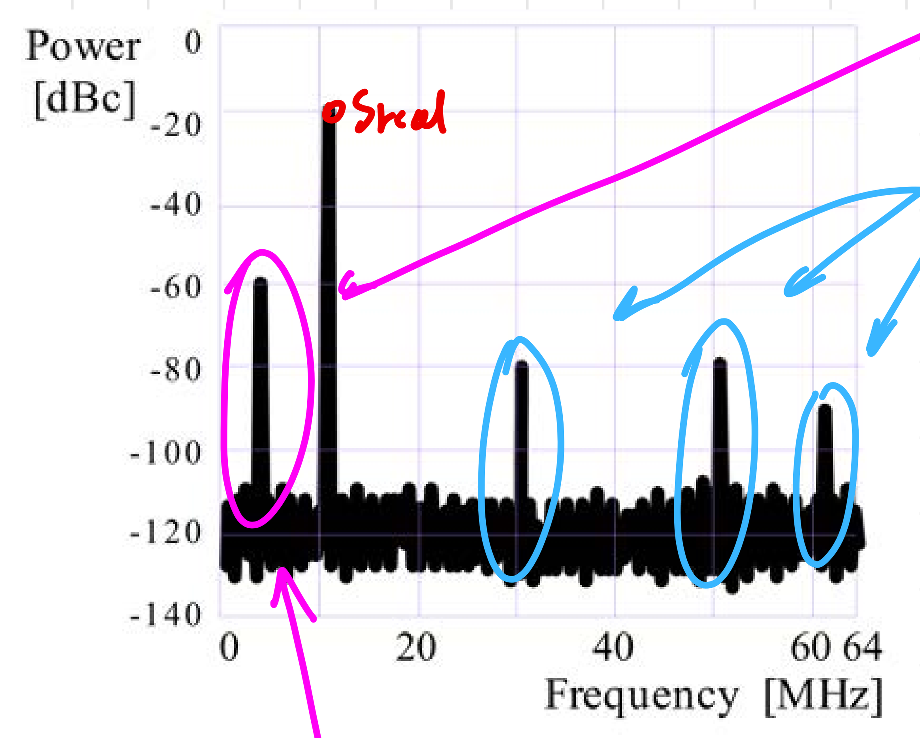
- $S_{max} = 0\,dB$
- $V_p = 2.5\,V$
- $N_{min}^2 = \frac{LSB^2}{12}$
- $SNR_{ideal} = 74\,dB$

in reality

- $S_{real} = 250\,mV$ → $SNR_{th} = 54\,dB$
- $V_p = 250\,mV$
- $N_{real} = N_{min} + \Delta N$
- $SNR_{real} = 45\,dB$

$$\hookrightarrow ENOB = \frac{SNR_{real} - 1.76}{6.02} = 7.8 \text{ bit} \longrightarrow 8 \text{ bit}$$

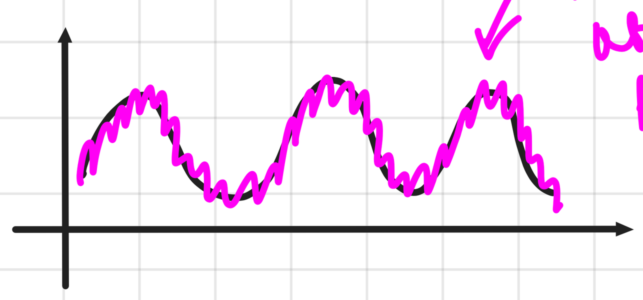
b) We now want to consider the other tones



these are harmonics → harmonic distortion → change with signal freq.

↳ usually due to DAC non-linearities ⊛

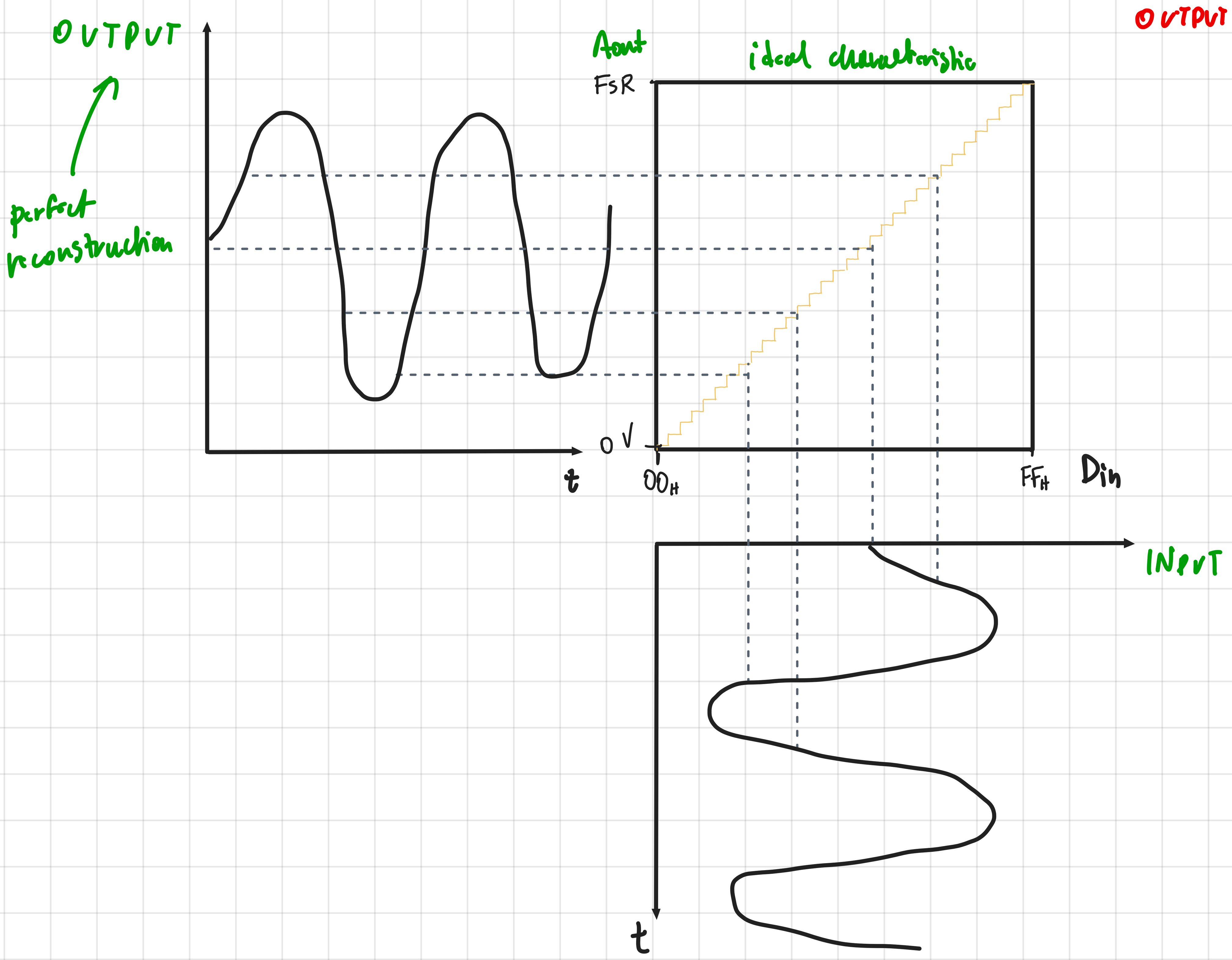
disturbance at 5MHz →

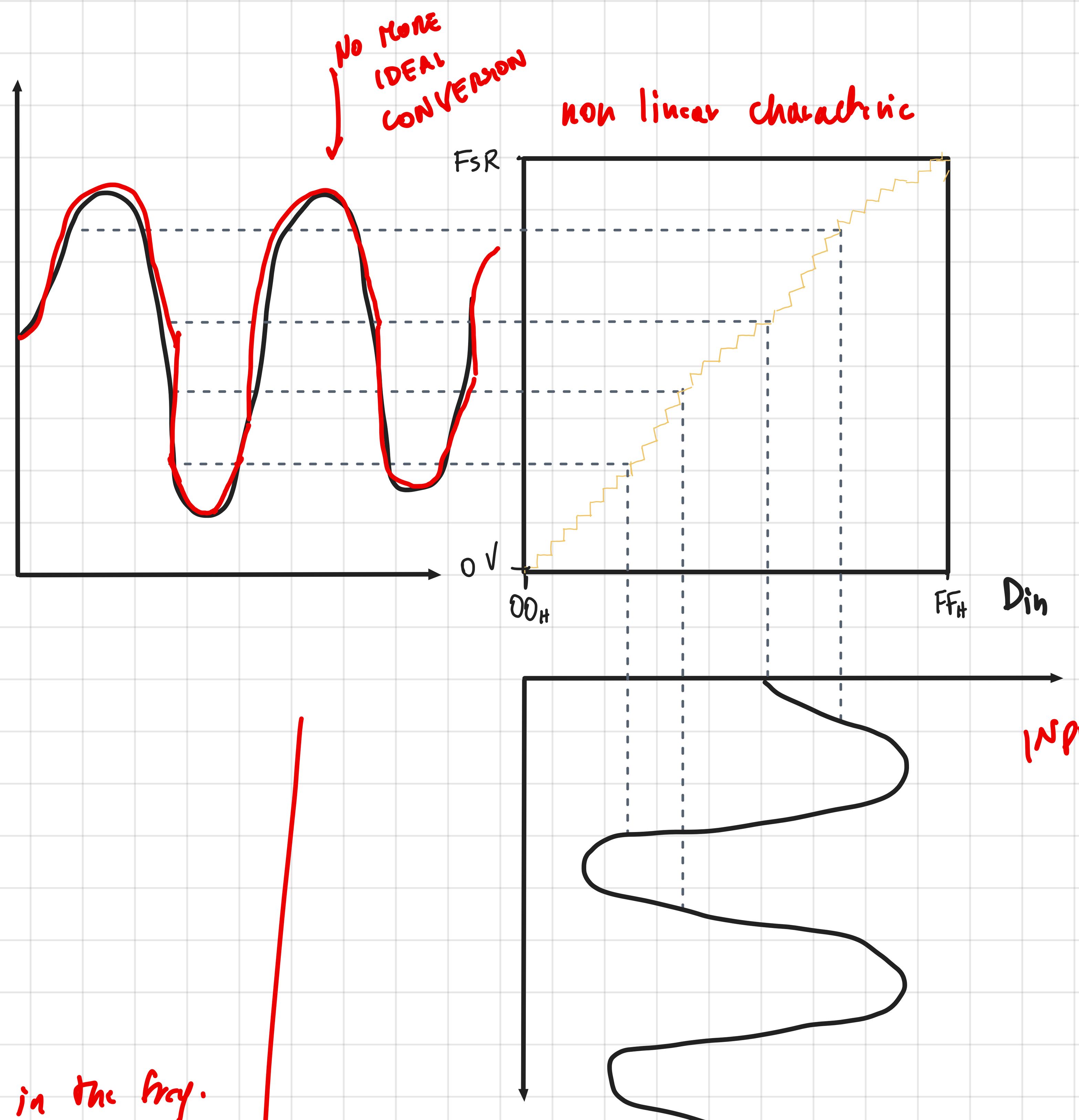


disturbance at fixed freq.

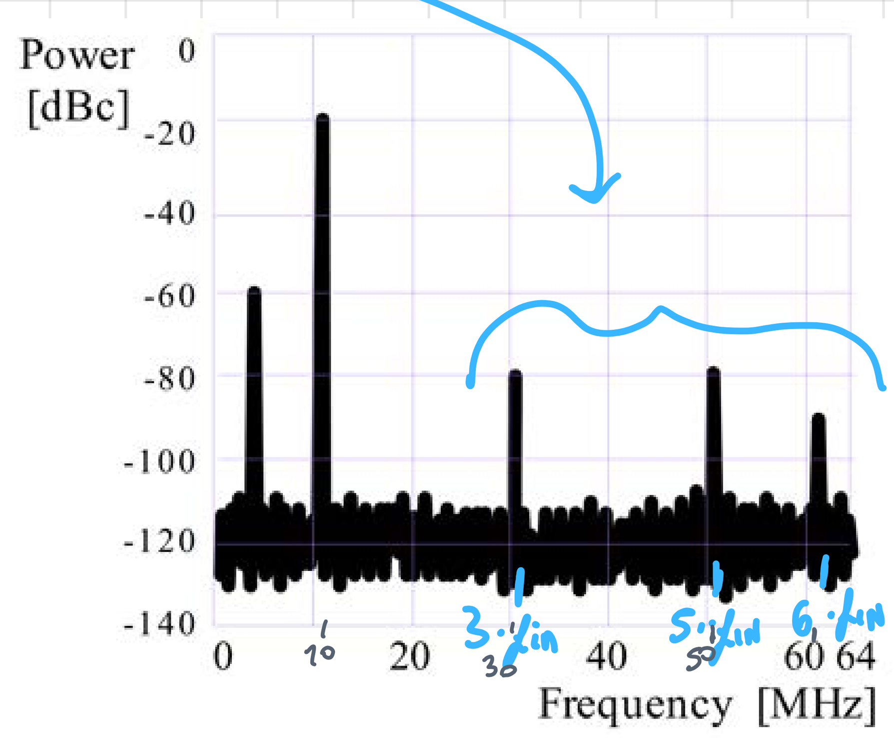
→ If we vary the signal freq. this disturbance doesn't change while

⊛ So observing the converter characteristics:





in the freq. spectrum we'll have all the other spurious harmonics of the tones

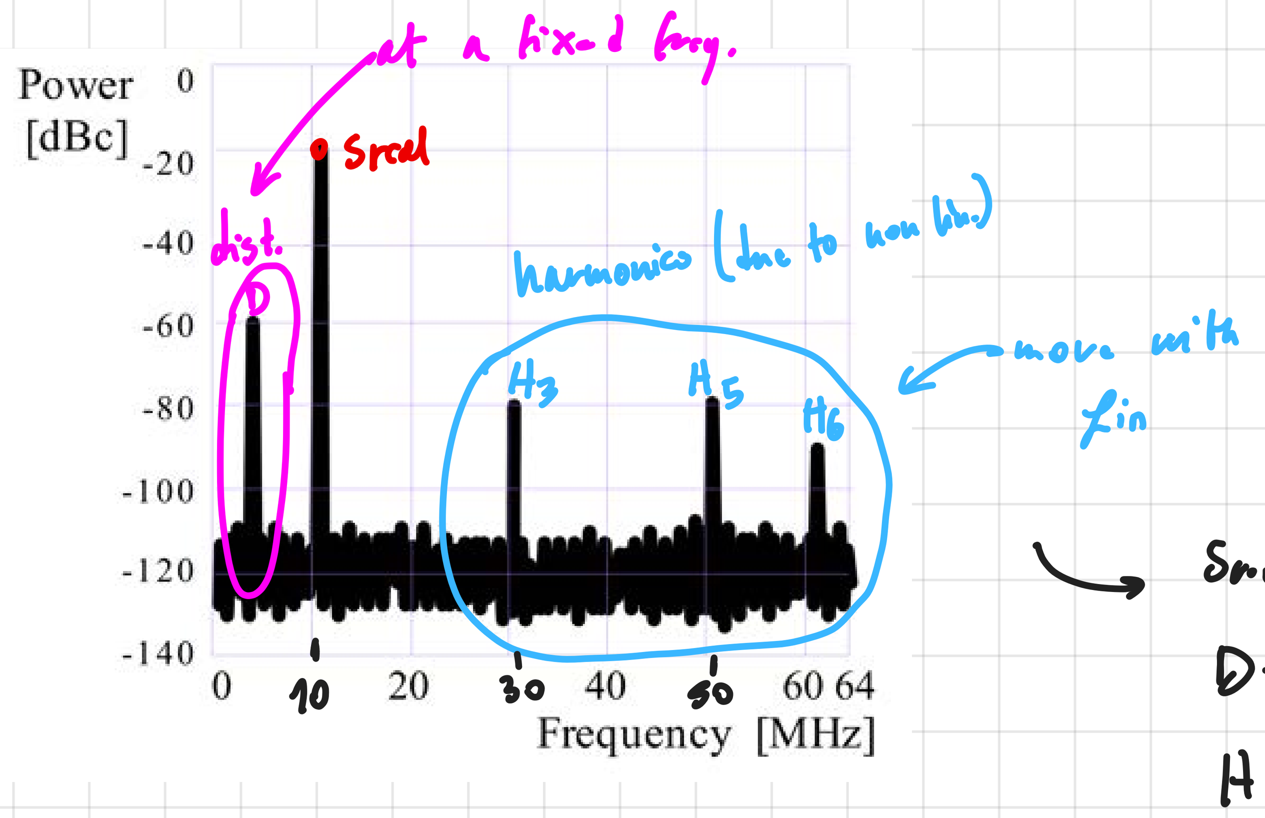


So if we change the input freq. the harmonics distortions

↓

all the freq. move away

↳ So given the experimental plot:



signal to (disturbance) distortion ratio:

$\rightarrow S_{real} = -20\,dBc$ $\quad SDR = -20\,dBc - (-60\,dBc) = 40\,dB$

$D = -60\,dBc$

$$H = \sum H_i = \underbrace{H_3 + H_5 + H_6}_{\text{sum powers}} = 10^{-\frac{80dBc}{10}} + 10^{-\frac{80dBc}{10}} + 10^{-\frac{90dBc}{10}} = 2.1 \cdot 10^{-8} = -77\,dBc$$

(it's not a product so not the sum in dBc)

$$\hookrightarrow \begin{cases} H_3 = -80\,dBc \\ H_5 = -80\,dBc \\ H_6 = -90\,dBc \end{cases}$$

↳ So the Total Harmonic Distortion is:

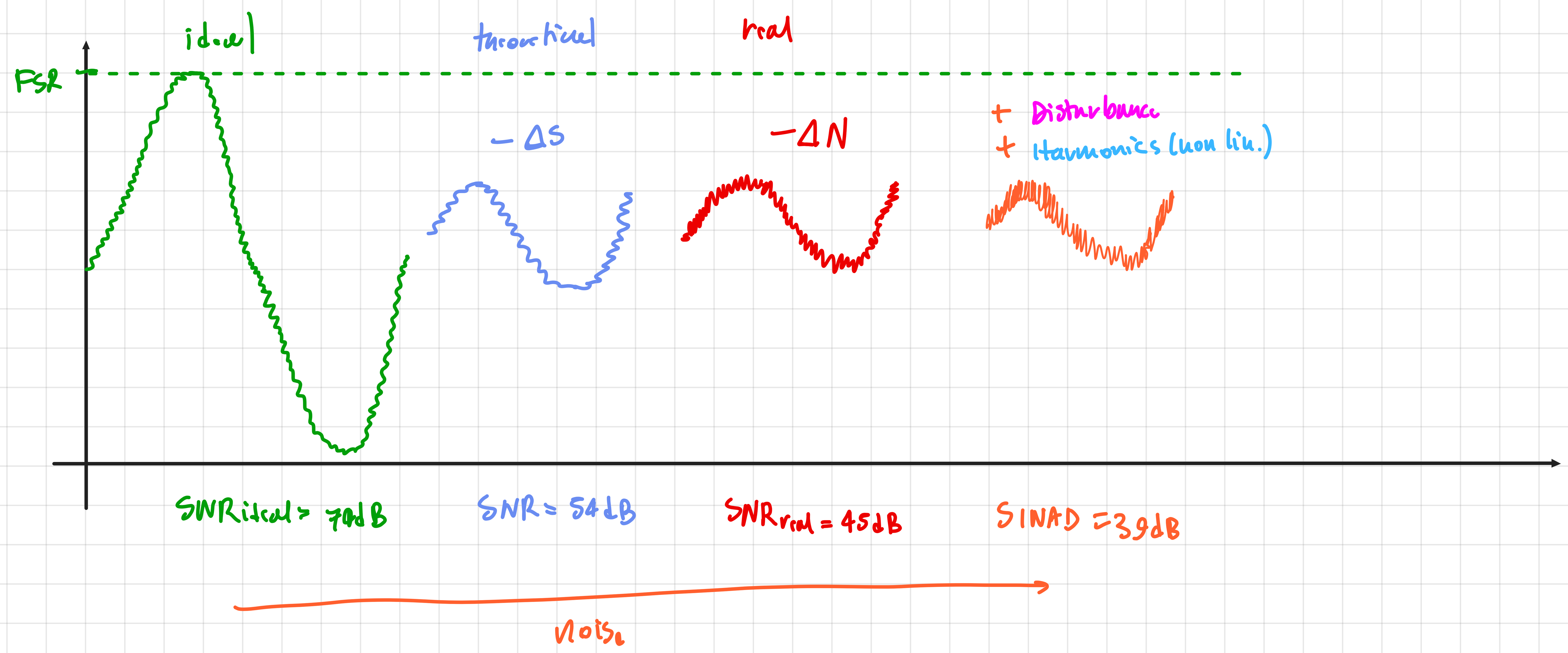
$$THD = \frac{H}{S_{real}} = -77\,dB_c - (-20\,dB_c) = 57\,dB$$

↳ We can also define the SINAD ratio:

$$SINAD = \frac{S}{N + D + H} = \frac{S_{real}}{N_{real} + D + H} = -20\,dB_c - \overbrace{10\log_{10}\left[10^{\frac{-65dB_c}{10}} + 10^{\frac{-60dB_c}{10}} + 10^{\frac{-77dB_c}{10}}\right]}^{+59dB_c} = 39\,dB$$

not a sum in dB_c

→ So representing the signal through the various noise considerations:

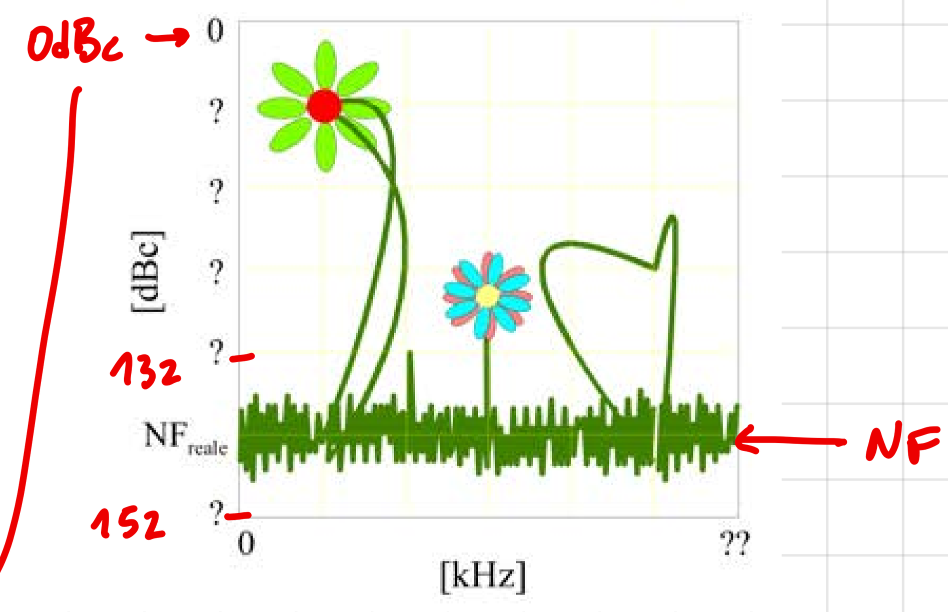


2

A 16bit DAC with FSR=5V receives a 2Msps stream of a sinusoidal signal at f_C=400kHz with 200mV$_{peak}$ amplitude. A noise is overimposed to the signal, thus lowering the SNR by 20dB. The number of samples used for the FFT is 512,000.

a) Compute SNR_{ideal}, SNR_{real}, ENOB and real NoiseFloor.

b) Draw the spectrum, properly quoted in [Hz] and [dBc], adding also a harmonic at $3 \cdot f_C$ due to a THD=-70dB.



$n = 16 \quad FSR = 5V \quad S_{max}^2 = \left(\frac{FSR}{2\sqrt{2}}\right)^2 = \ldots ? = 0dBc$

$SNR_{ideal} = 6.02\,n + 1.76 = 98dB$ $\quad \left(SNR_{ideal} = \frac{S_{max}}{N_{min}} \right)$

$N_{min} = N_{quant.} = \frac{LSB^2}{12} = \ldots ? = -98\,dBc$

$NF_{ideal} = \frac{N_{ideal}}{N_{sample}} = -98dBc - 10\log \frac{512000}{2} = -98dBc - 54dBc = -152dBc$

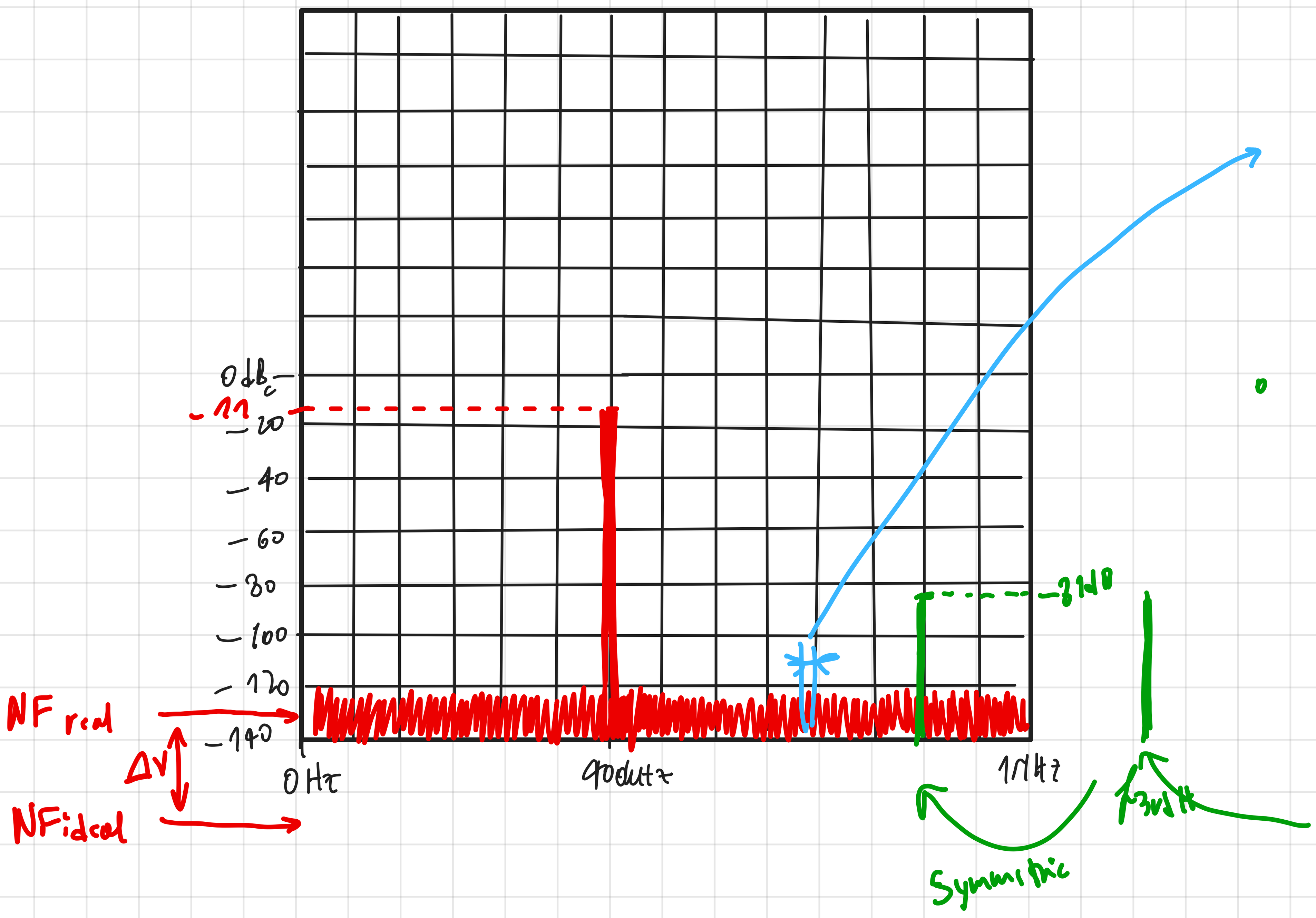
$\Delta N = ?$ $\quad NF_{real} = NF_{ideal} + \Delta N = -152\,dBc + 20\,dB = -132\,dBc$

$\Delta S = \frac{5_{pp}}{0.4_{pp}} = 11dB$

$SNR_{th} = SNR_{ideal} - \Delta S = 98\,dB - 11 = 87\,dB$

$SNR_{real} = SNR_{th} - \Delta N = 87\,dB - 20dB = 67dB$

$f_{in} = 400\,kHz \quad f_s = 2Msps \quad \frac{f_s}{2} = 1Msps$



$\text{bin-width} = \frac{f_s}{N_{sample}} = \frac{\frac{f_s}{2}}{\frac{N_{sample}}{2}} = \frac{2MHz}{512k}$

$ENOB = \frac{SNR_{real} + 1.76}{6.02} = \frac{67 + 1.76}{6.02} \simeq 11.4 \Rightarrow 12\text{ bits}$

$THD = \frac{H}{S_{real}} = -70dB$

$f_{3rdH} = f_{H3} = 3 \cdot f_c \to 1.2\,MHz$

$H3 = -11dBc - 70dB \to -81\,dBc$

Notes: On the computations:

$\frac{\text{Numerator}}{\text{Denominator}} = \frac{\text{Power}}{\text{attenuating factor}} = \frac{70dBc}{20\,dB} = 70dBc - 20\,dB = 50\,dBc$

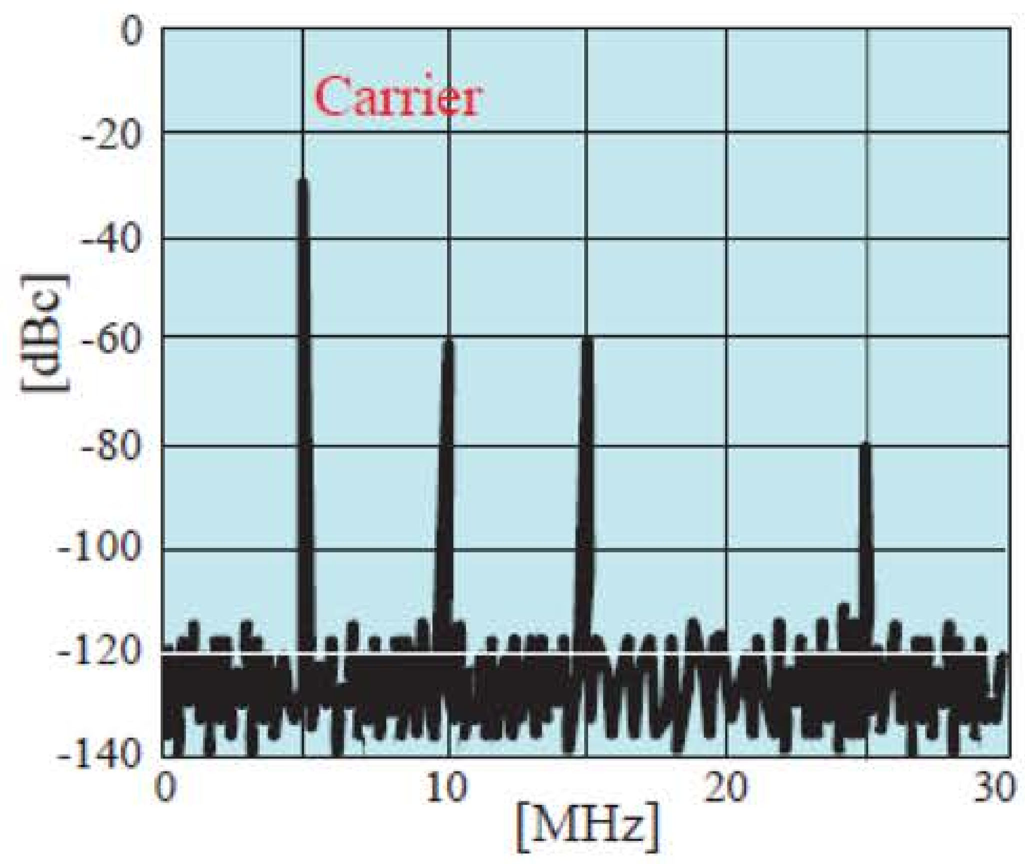
$H_1 + H_2 + D + N = -80dBc - 90dBc - 85dBc - 69dBc = 10\log\left[10^{-8} + 10^{-9} + 10^{-8.5} + 10^{-6.9}\right] = -65\,dBc$

(3)

14 bit ADC with 3.3V FSR, spectrum with 680ms acquisition.

a) Compute SNR_{ideal}, SNR_{th}, SNR_{real}, SiNAD, and THD.

b) In case the 4^{th} harmonic power is 10^6 lower than the carrier, compute the required duration of the acquisition stream for detecting the harmonic with an SNR=10dB over the noise floor.



(not done)

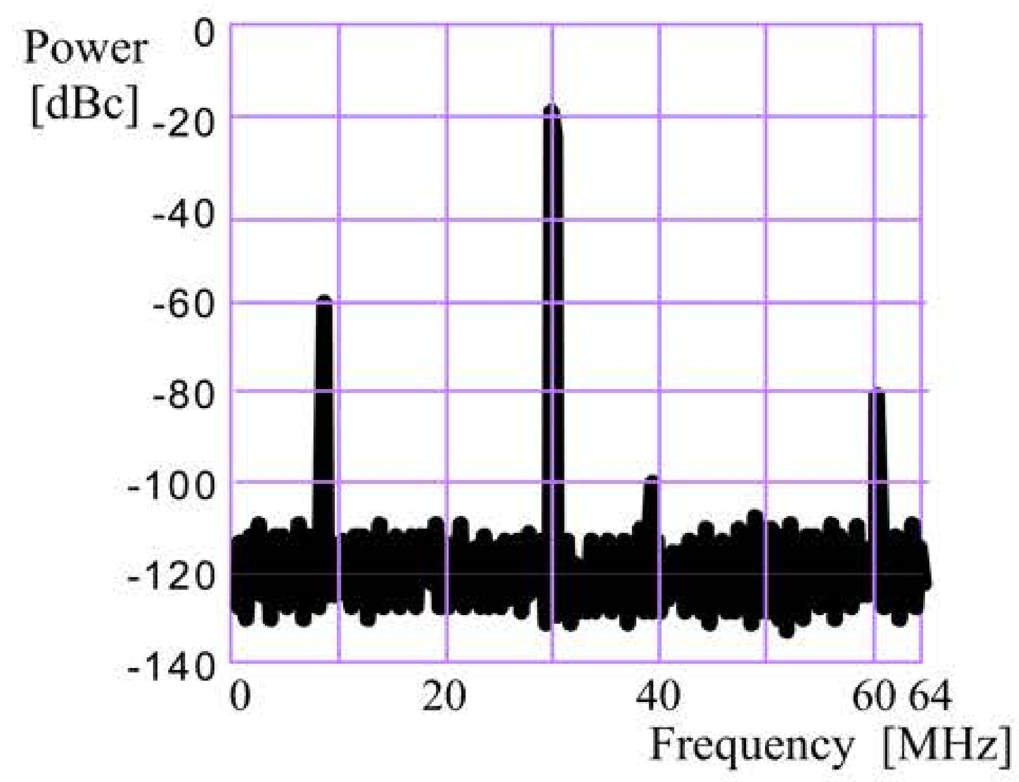
4

16bit ADC with +3.3V FSR. Measured output spectrum with 2kHz bin-widths. The signal is at 30MHz.

a) Compute SNR_{ideal}, SNR_{real} and the real noise (in V_{rms}).

b) Compute the THD and the SiNAD.

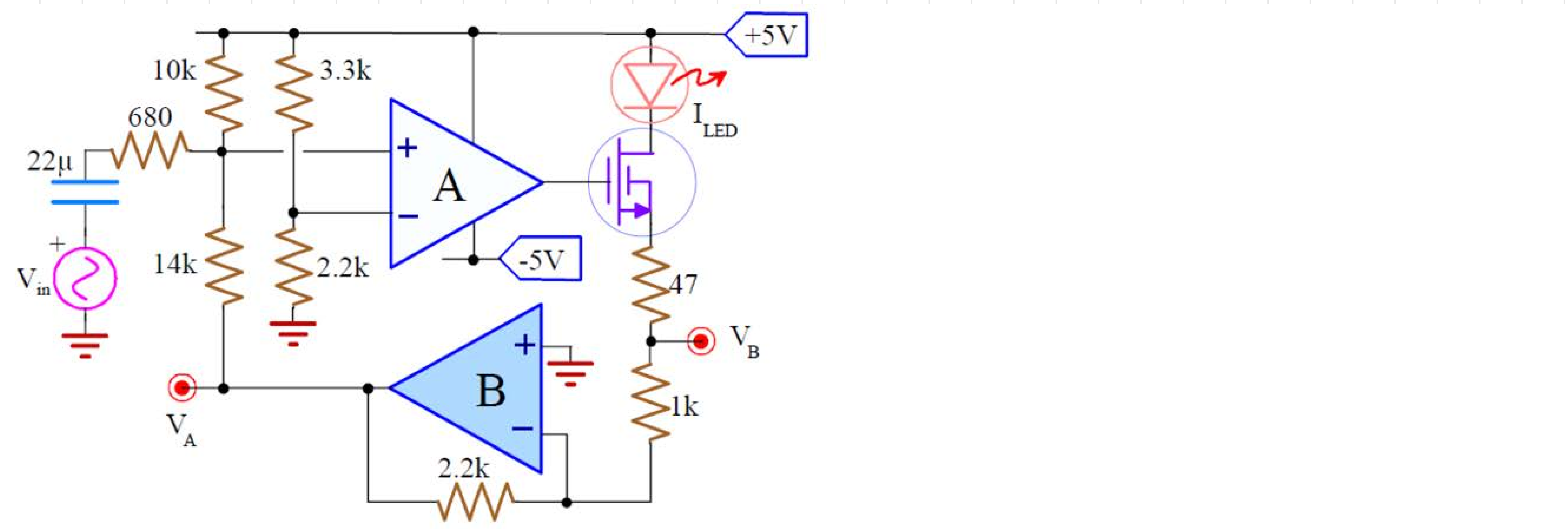
c) Compute the 3^{rd} harmonic rms and explain why it is at 38MHz.



(not done)

21/11/22

EX06_EXAMS



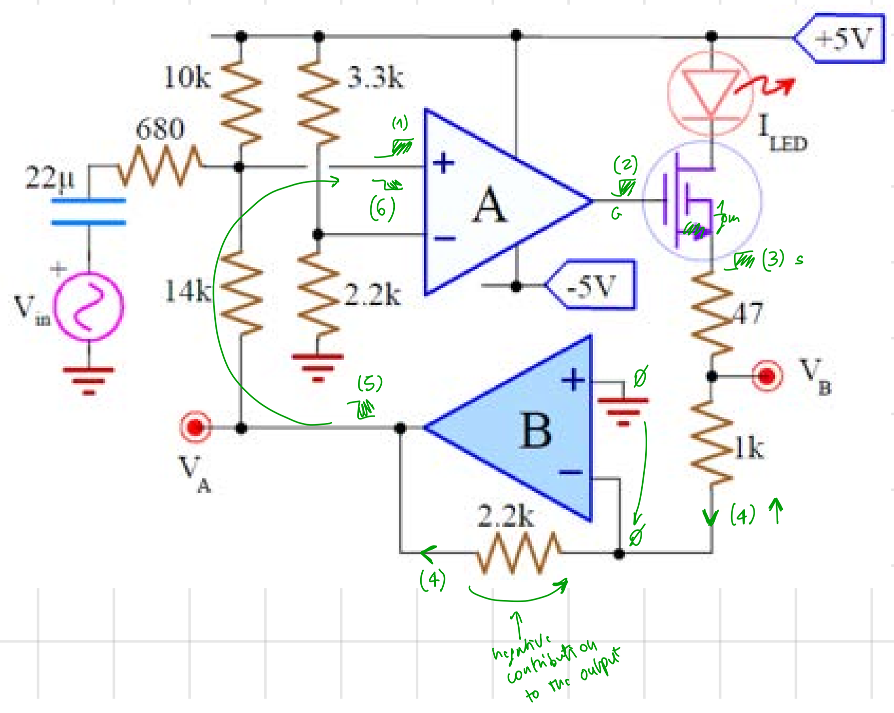
OpAmps with A_0=50V/mV, V_{OS}=5mV and I_B=200pA. MOSFET with k=10mA/V² and V_t=0.8V.

a) Compute the relationships of V_A, V_B and I_{LED} vs. V_{in}.

b) Compute the input pole and plot $V_A(t)$ and $I_{LED}(t)$ waveforms when the input is a high frequency 200mV$_{pp}$ sinusoid.

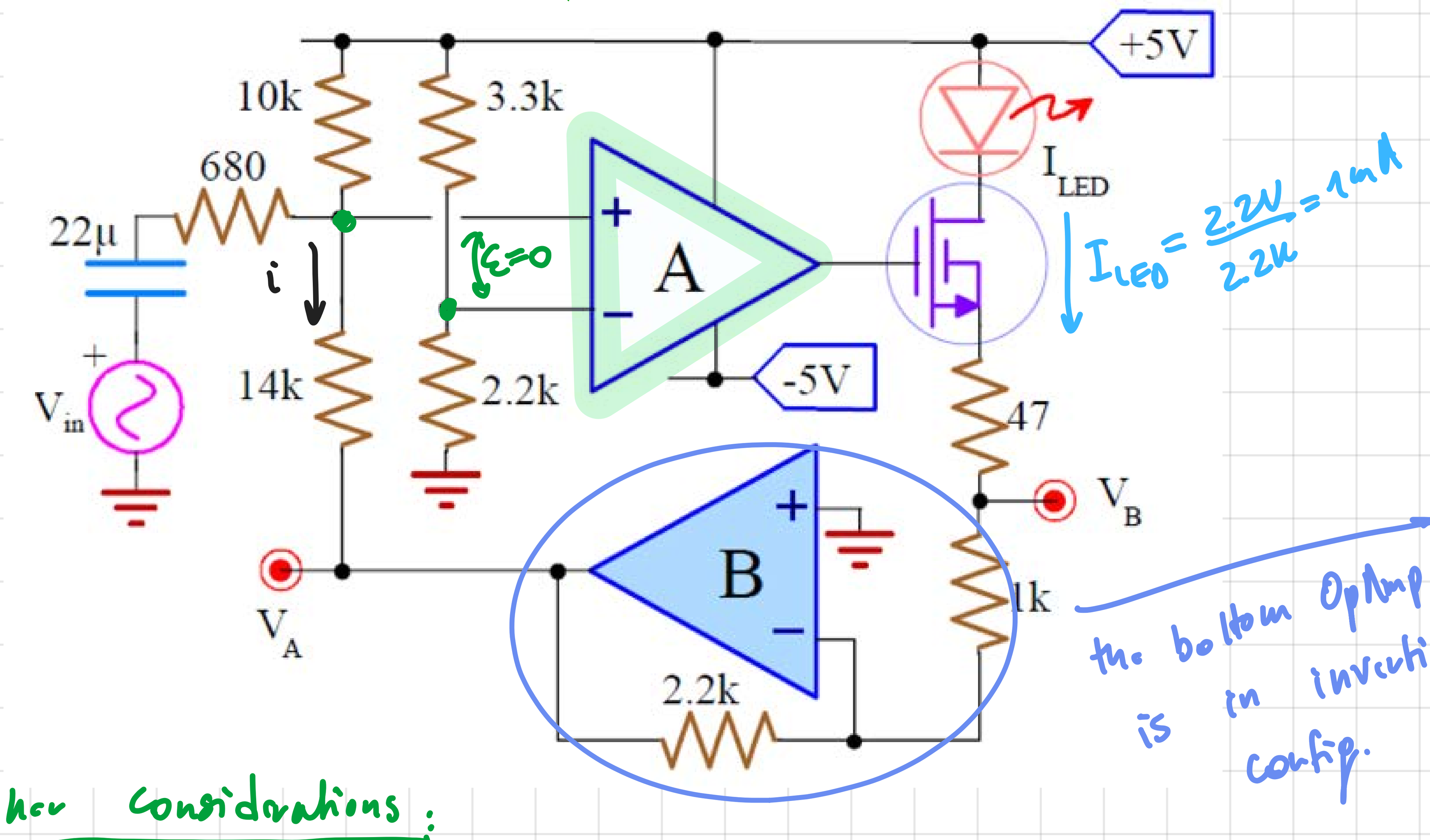
c) Compute the maximum V_A static error due to V_{OS} and I_B of the OpAmps.

a) (Negative feedback check)



→ Negative feedback → virtual ground ↓ so an OpAmp should have infinite gain

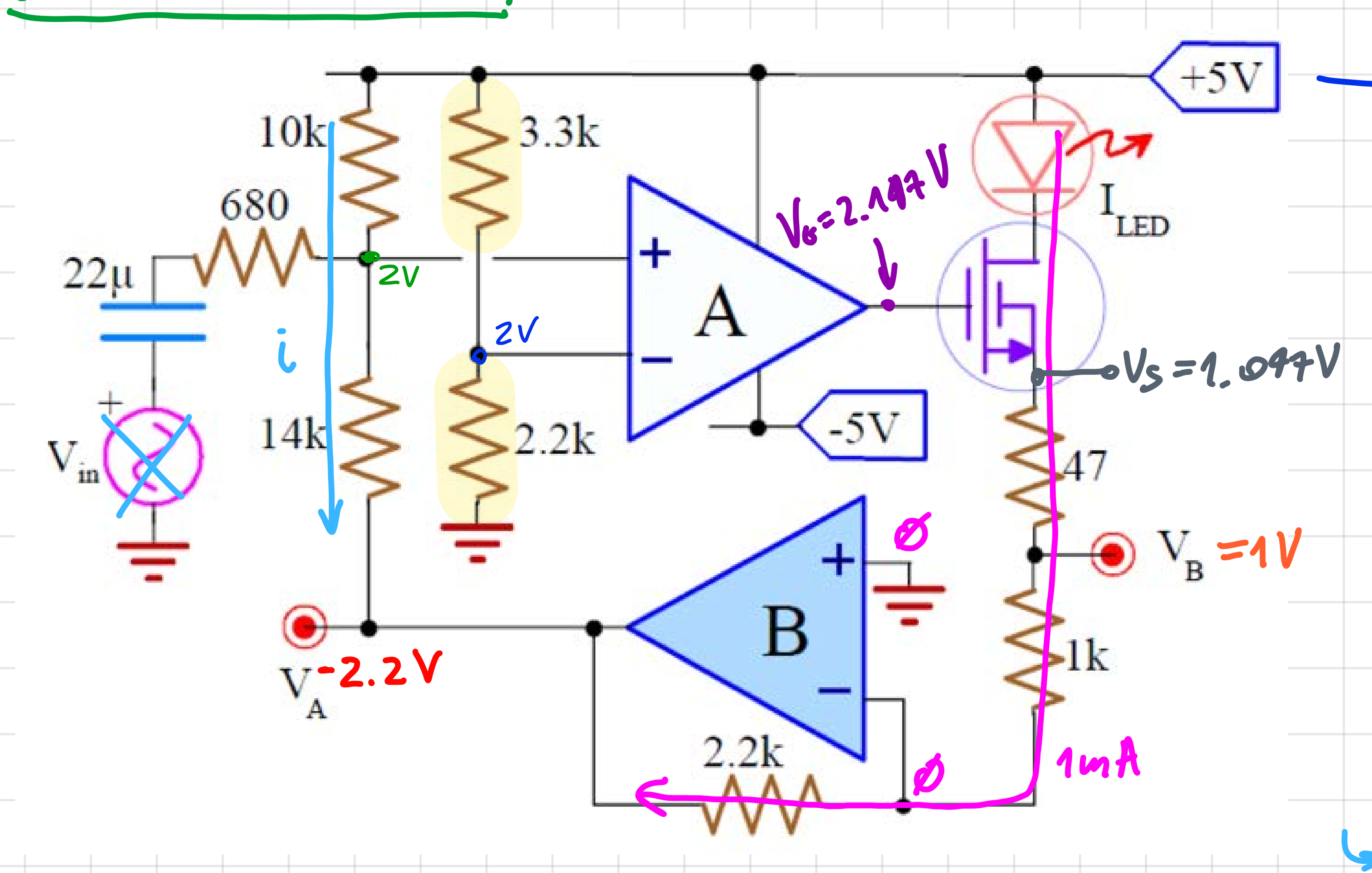
→ OpAmp A will provide infinite gain ↓ $\varepsilon = 0$ (VIRTUAL GROUND)



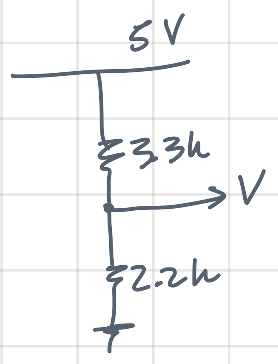
the bottom OpAmp B is in inverting config.

$G = -\frac{R_2}{R_1} = -\frac{2.2k}{1k+47}$ ← Finite gain

Other considerations:



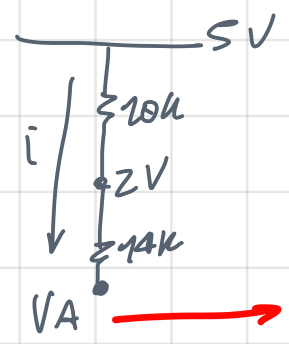
→ Due to the P.S., thanks to the resistors we reach a voltage on the ⊖ pin of 2V



$V^- = \frac{2.2k}{2.2k+3.3k} 5V = 2V$ (with $\frac{2.2k}{2.2k+3.3k} = \frac{2}{5}$)

↳ thanks to neg. feedback we'll have virtual ground $\varepsilon = 0$ so also on the ⊕ pin will have 2V

↳ At $\boxed{\text{DC (C open)}}$ we should have the same current i across the 10k and 14k resistors → $i = \frac{5-2}{10k} = 0.3m = 300\mu A$



→ so $V_A = 5 - i(10k + 14k) = -2.2V$

↳ in order to provide $V_A = -2.2V$ having virtual ground in OpAmp B in inverting config. it means we'll have a current across the 2.2k resistor (this current will pass also through the LED) so it is:

↳ $I_{LED} = \frac{2.2V}{2.2k} = 1mA$ → (LED is always ON to provide V_A)

↳ We can then compute also V_B as:

$V_B = 1k \cdot I_{LED} = 1V$ (At the MOS source → $V_S = 1.047V$)

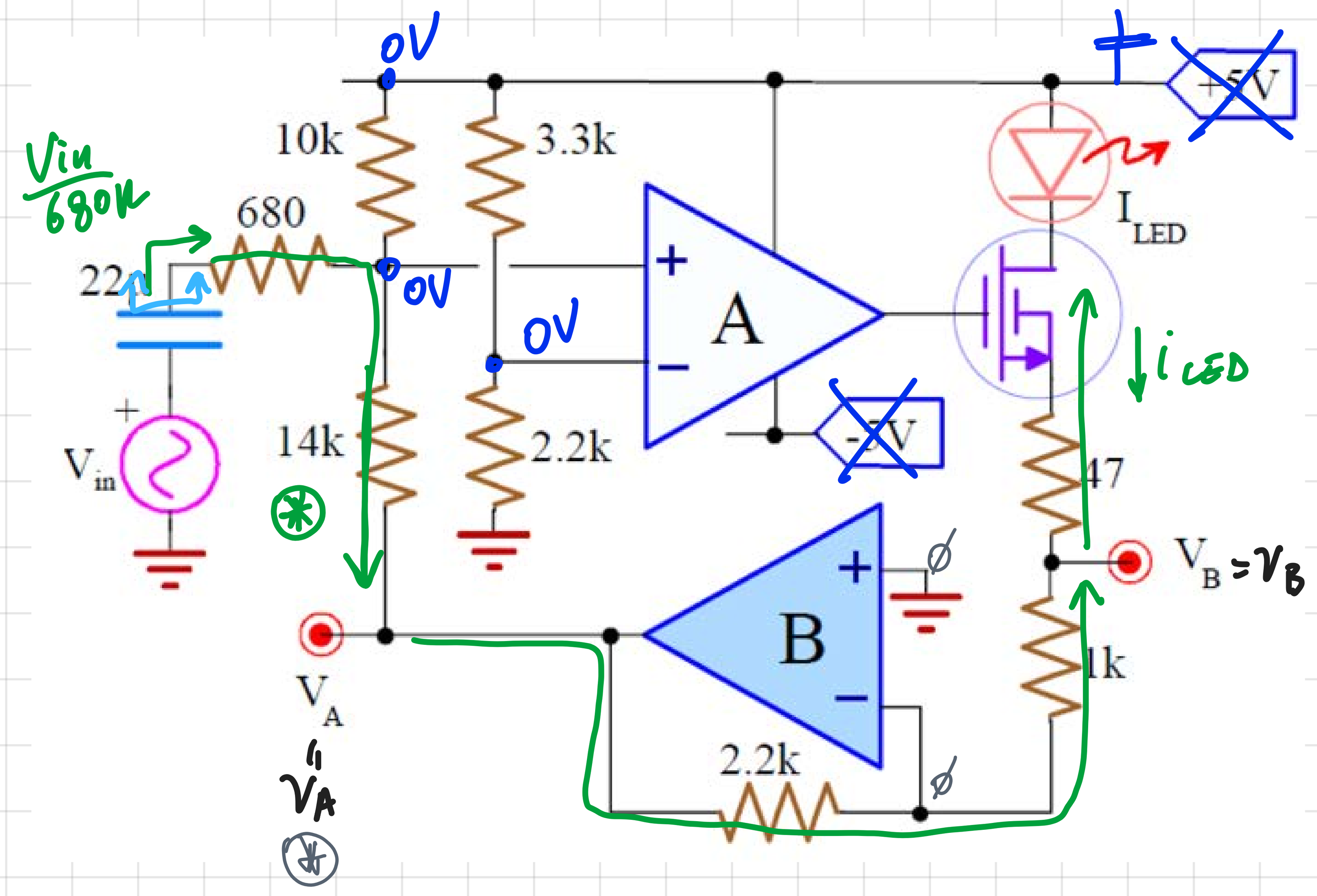
→ V_G (GATE MOS): From the eq. $I_D = k \cdot OD^2$ ($OD = V_{GS} - V_t$)

↳ $V_{GS} = \sqrt{\frac{I_D}{k}} = \sqrt{\frac{1mA}{10\frac{mA}{V^2}}} + 0.8V = 1.1V$ → $V_G = 2.147V$

⟹ DC
- $i = 300\mu A$
- $V_A = -2.2V$
- $I_{LED} = 1mA$
- $V_B = 1V$
- $V_S = 1.047V$
- $V_G = 2.147V$

→ Now we study the signal (so when C is not open)

We can consider the P.S. turned OFF → so at ⊖ and ⊕ are ∅



$$pol_{cin} = \frac{1}{2\pi \cdot 22\mu \cdot 680} = 10.6\ Hz$$

← since at pin ⊕ we have ∅ → $R_{eq} = 680k$

$Z_{cuoin} = \emptyset$ → the capacitor stops the DC ($\simeq 0$ Hz)

↑ so we can have 0 output applying $V_{in} \neq 0$ at 0 Hz freq. ⇓ zero in 0Hz!

→ since across 10k we'll have ∅ voltage ⇓ ∅ current → $\frac{V_{in}}{680k}$ goes all in one direction ⊛

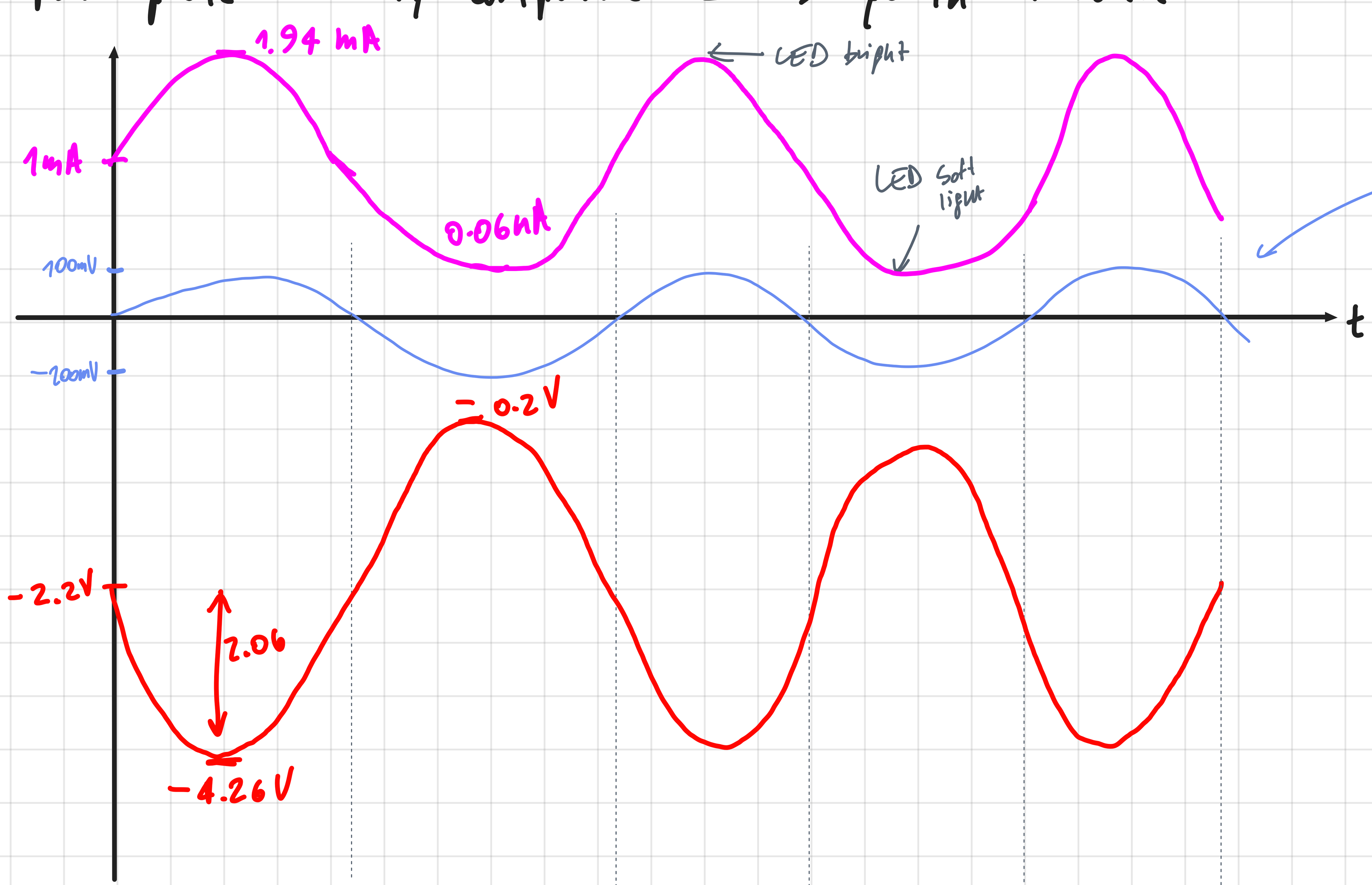
↳ $V_A = -\frac{V_{in}}{680} 14k \Rightarrow \boxed{\frac{V_A}{V_{in}} = -\frac{14k}{680} = -20.6}$

↳ $\underbrace{-V_B \cdot \frac{2.2k}{1k}}_{\text{Gain of opAmp B}} = V_A$ → $V_B = \frac{14k}{680} \cdot \frac{1k}{2.2k} V_{in}$ → $\boxed{\frac{V_B}{V_{in}} = \frac{14k}{680} \cdot \frac{1k}{2.2k} = 9.4}$

↳ $i_{LED} = -\frac{V_A}{2.2k}$ → $\boxed{\frac{i_{LED}}{V_{in}} = \frac{14k}{680} \cdot \frac{1}{2.2k} = 9.4\ \frac{mA}{V}}$

Note: Since we're analyzing just the signal contribution is better to write the voltages in small⊛ letters and use the capital one for the total signal that sums the signal + polarization (DC)

b) • input pole already computed → $pole_{in} = 10.6\ Hz$



input signal Vin

V_A = (−2.2V polarization) + signal contribution (Gain = −20.6)

↳ (peak −4.26 V is reachable with P.S. ±5V)

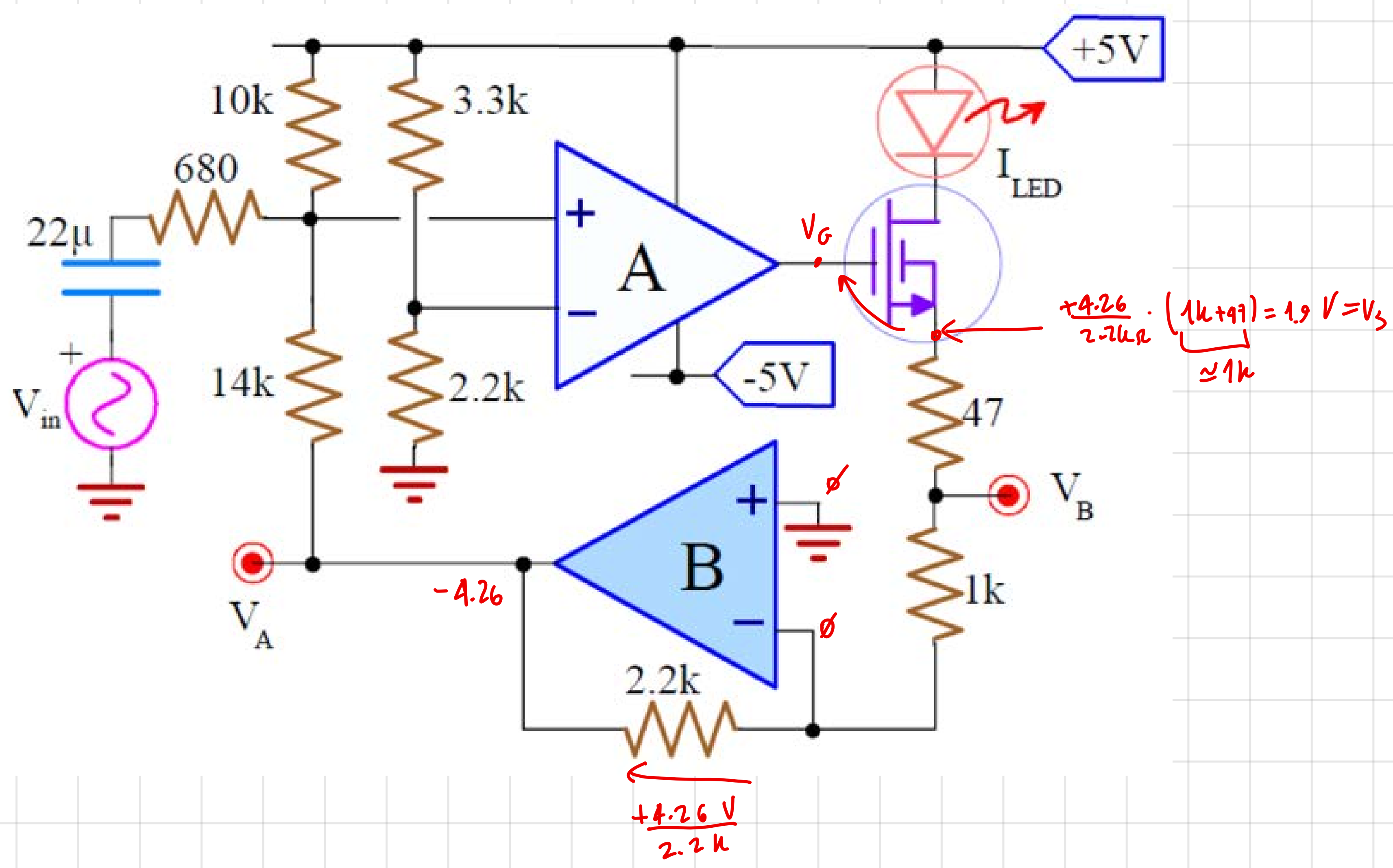
I_{LED} = (1mA polarization) + signal contribution (Gain = 9.4 mA/V)

↳ We should check if the LED saturates

↳ We check if we can actually reach $-4.26\,V$ and $1.94\,mA$

(From the previous plot)

When $V_A = -4.26$ $I_{LED} = 1.94\,mA$

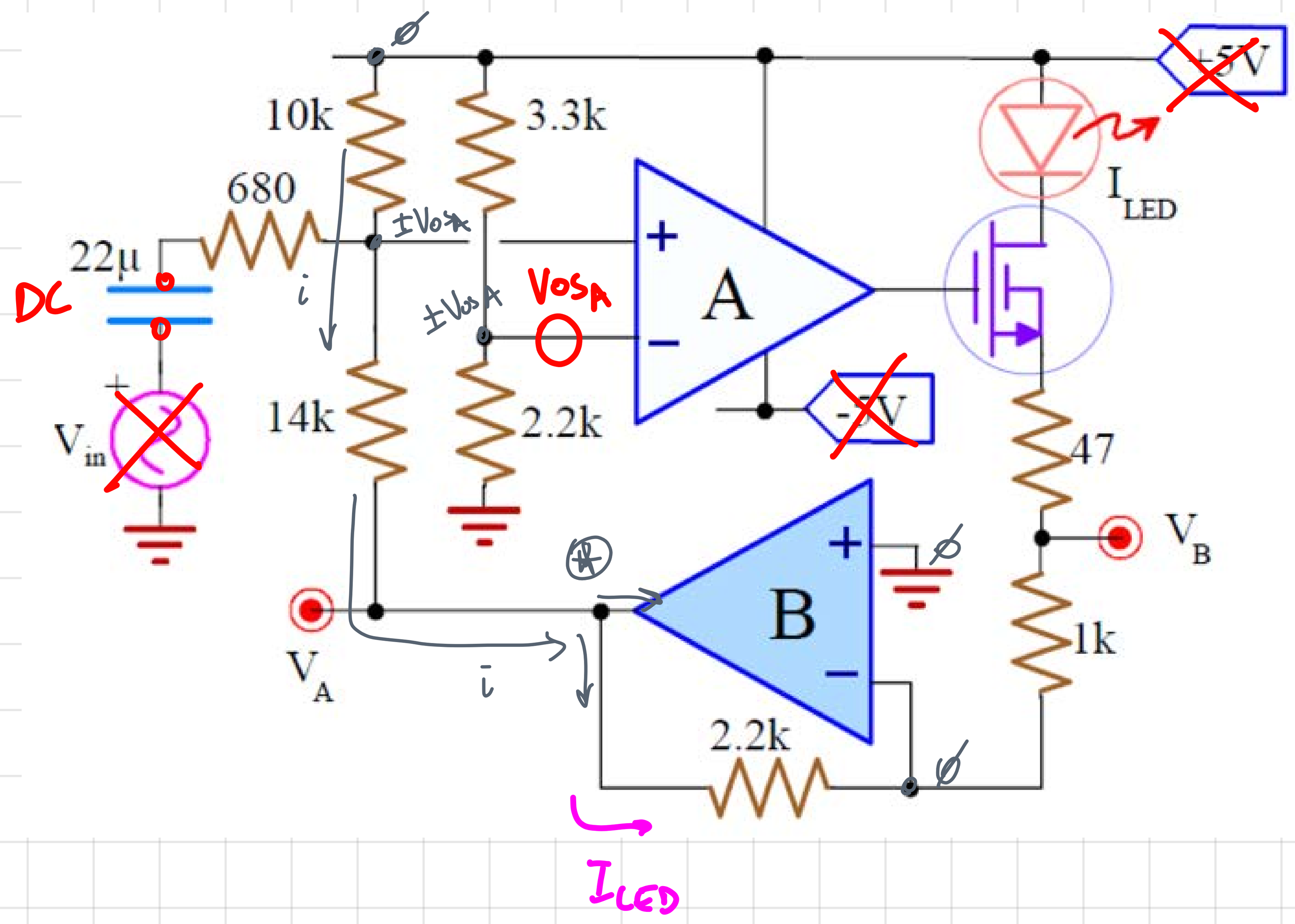


↳ $V_{GS} = \sqrt{\dfrac{I_{LED}}{k}} + V_t = 1.24\,V$

$V_G = 1.24 + \underbrace{1.9}_{V_S} = 3.14 < 5$ ✓

We should also check that we can reach $\simeq -0.2\,V$ and $0.06\,mA$ ⟶ they're both really low so the MOS will be near interdiction and $V_G \simeq V_t$ (reasonable V)

c)



V_{osA}

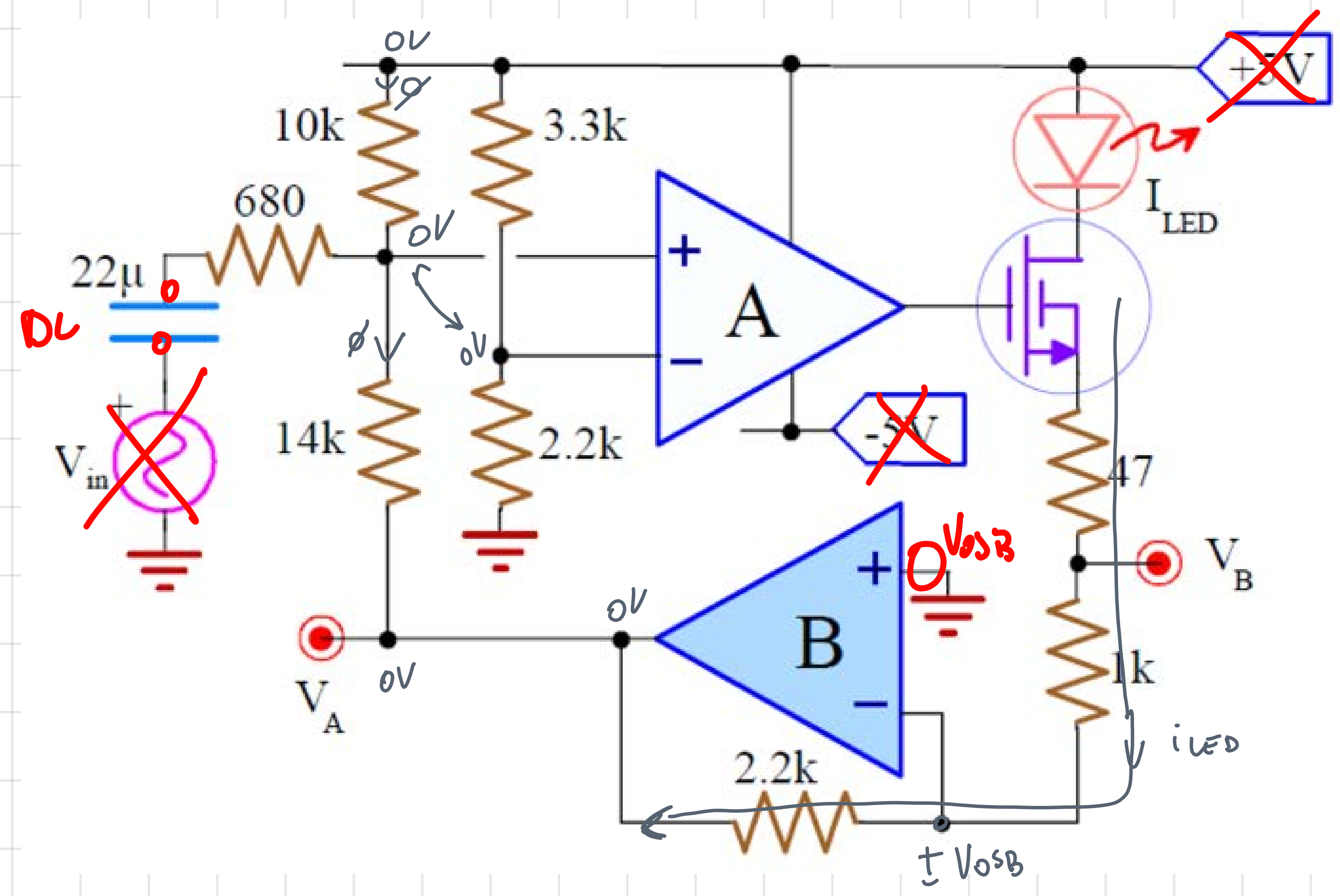
$i = \dfrac{\pm V_{osA}}{10k}$

- $V_A = \dfrac{\pm V_{osA}}{10k}(10k + 14k) = \pm V_{osA} \cdot 2.4 = \pm 12\,mV$

the offset is amplified

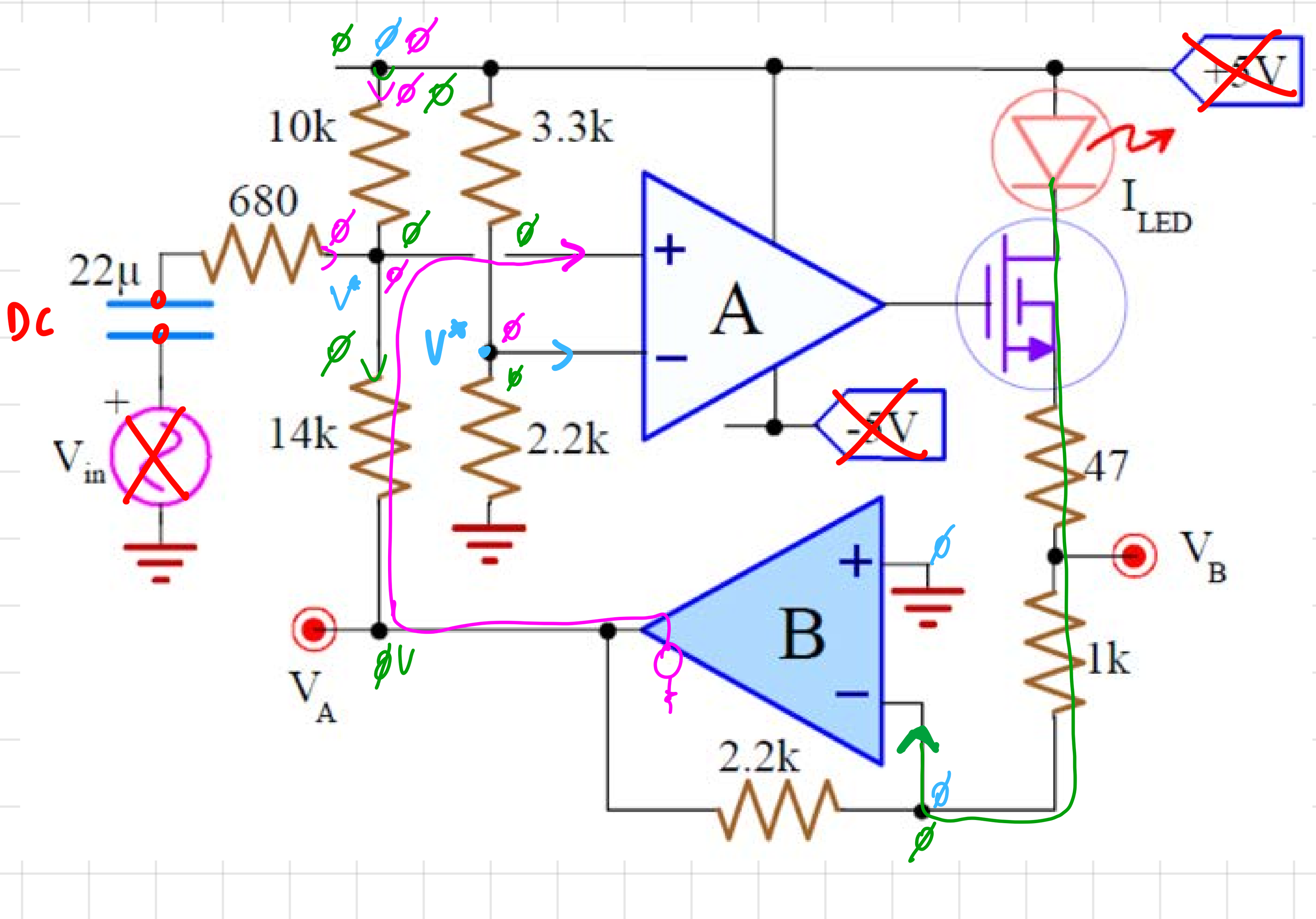
not that big compared to V_A values

- $i_{LED} \neq i$ ⟶ $i_{LED} = \dfrac{V_A}{2.2k} = \pm \dfrac{V_{osA} \cdot 2.4}{2.2k} = \pm 5\,\mu A$



V_{osB}

$i_{LED} = \dfrac{\pm V_{osB}}{2.2k} = 2.3\,\mu A$



I_B

I_{BA}^-

$V^* = I_{BA}^- (2.2k // 3.3k) = 264\,nV$

$V_A = \dfrac{V^*}{10k} \cdot 24k$

LOW VALUES

$i_{LED} = \dfrac{V_A}{2.2k} = \dfrac{264\,nV}{10k} \cdot \dfrac{24k}{2.2k} = 290\,pA$

I_{BA}^+

$V_A = I_{BA}^+ \cdot 14k$

$i_{LED} = \dfrac{V_A}{2.2k} = \ldots$

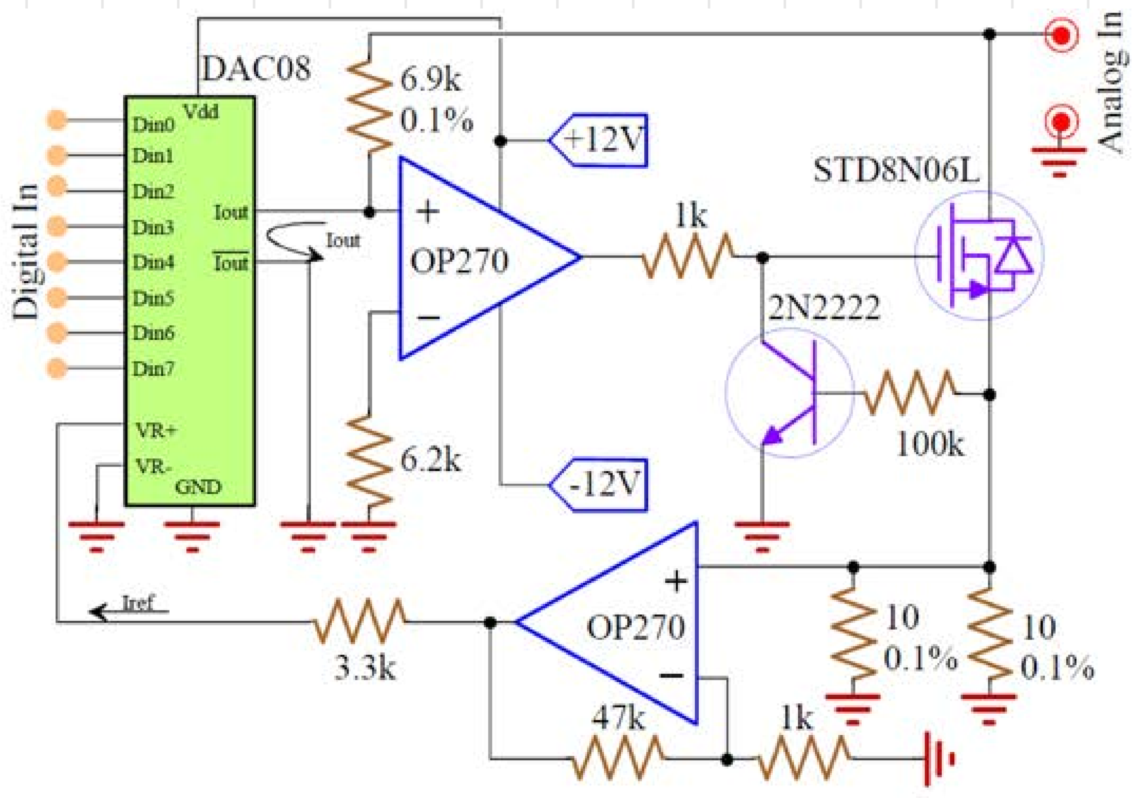
(I_{BB}^+ no effect)

I_{BB}^-

$i_{LED} = I_{BB}^- = 200\,pA$

(The sign of this contributions can be ±)

2

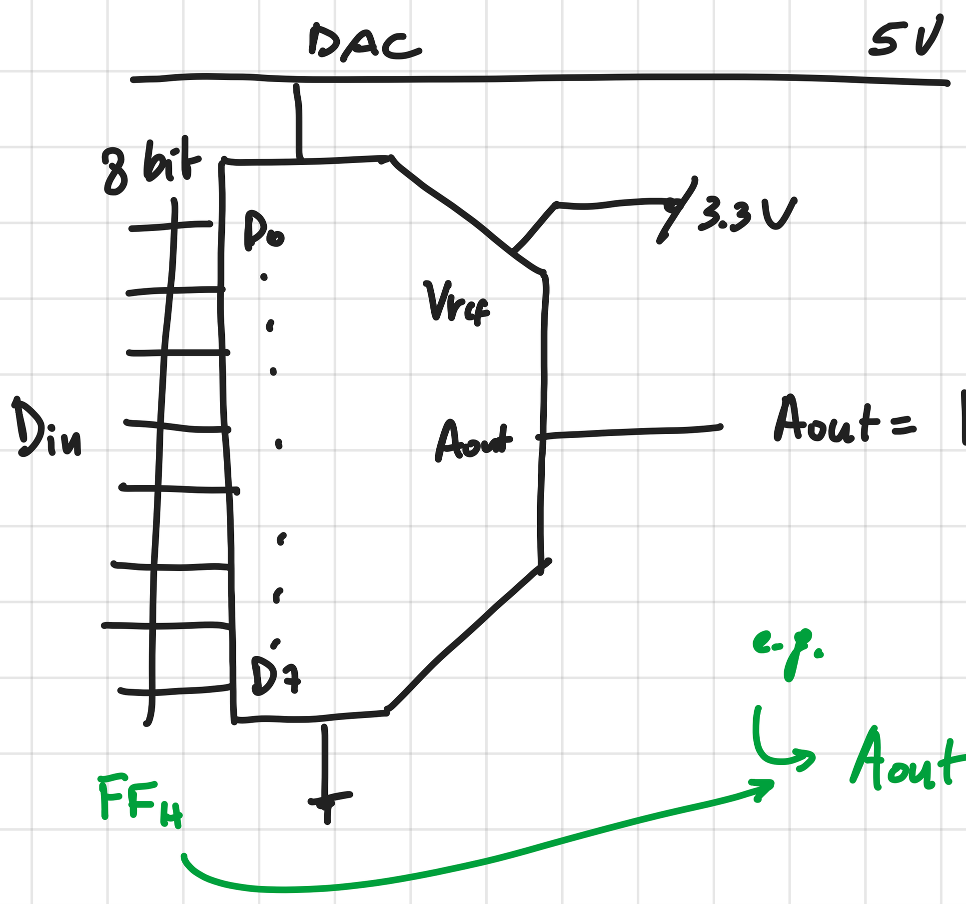


The DAC provides $I_{out}=I_{ref}\cdot D_{in}/256$ (D_{in} is the Digital In value) and **virtual ground** at its V_{R+} input. OpAmps have A0=1500V/mV and GBWP=5MHz. A voltage generator is applied at the Analog Input.

a) Obtain the analytical relationship V_{in}/I_{in}, as a function of N.

b) Reckon if the stage is stable or not when D_{in} =255. Moreover, tell if stability improves by reducing D_{in}. (hint: assume $1/g_{mMOS}$=495Ω and ignore the role of 2N2222 BJT).

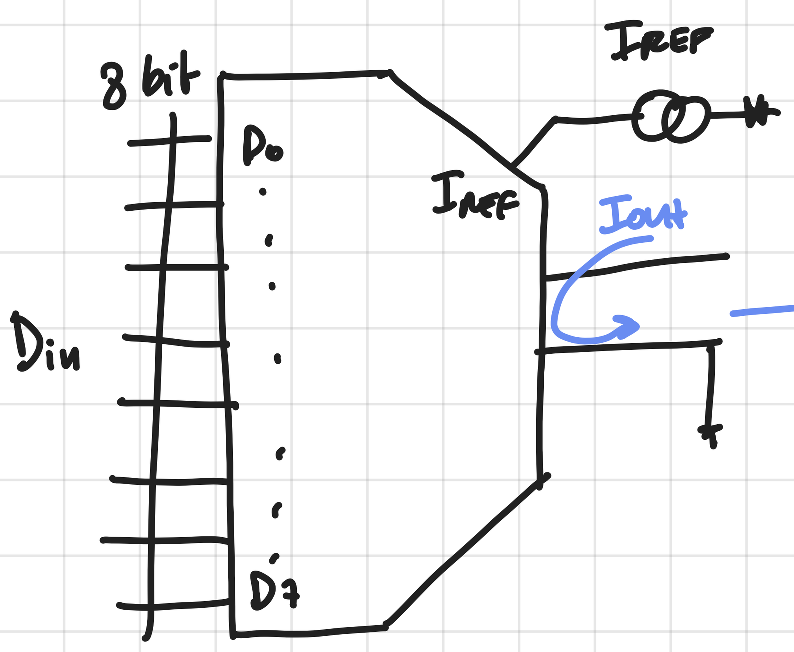
Note For DAC:



$A_{out} = V_{ref} \cdot \frac{D_{in}}{2^8}$

in this ex. we have an output current (not a voltage)

We consider

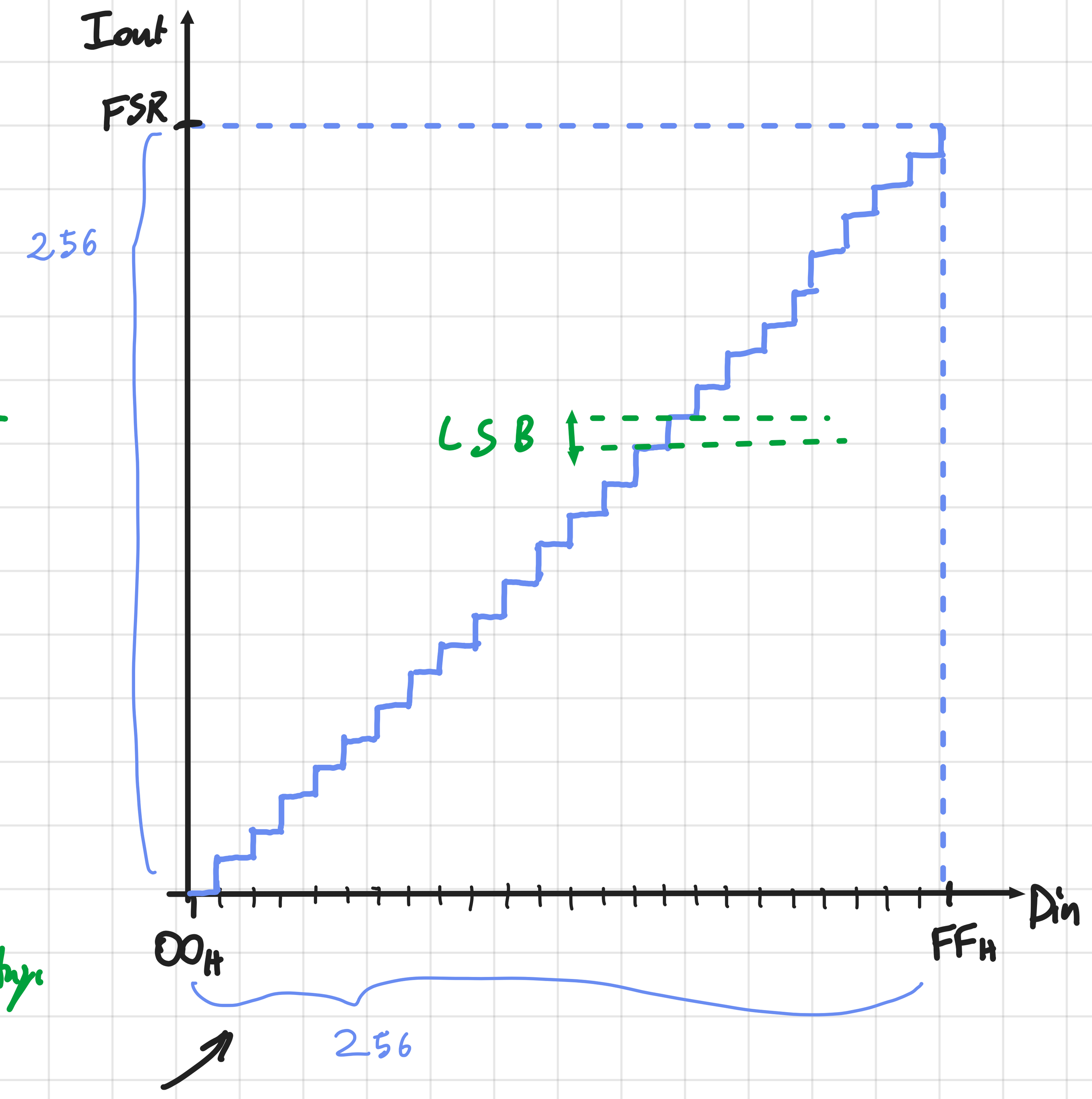


$I_{out} = I_{REF} \cdot \frac{D_{in}}{2^8}$

e.g.

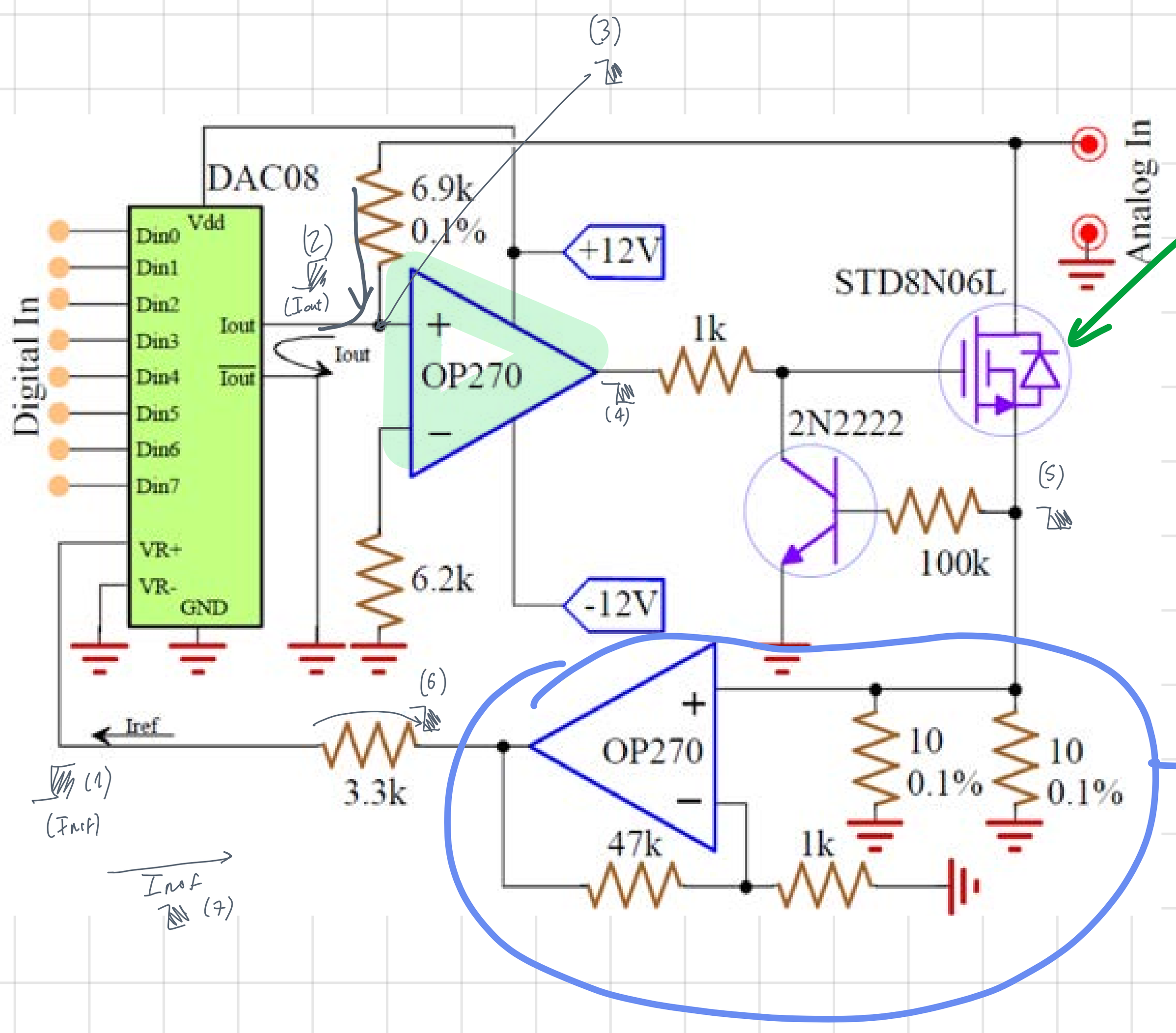
$A_{out} = 3.3 \cdot \frac{255}{2^8} = 3.3 \cdot \frac{255}{256} \simeq 3.3V$

with



$LSB = \frac{FSR}{2^n} = \frac{5V}{2^8} = 19mV$

a)



this is a voltage follower

From what we've seen:

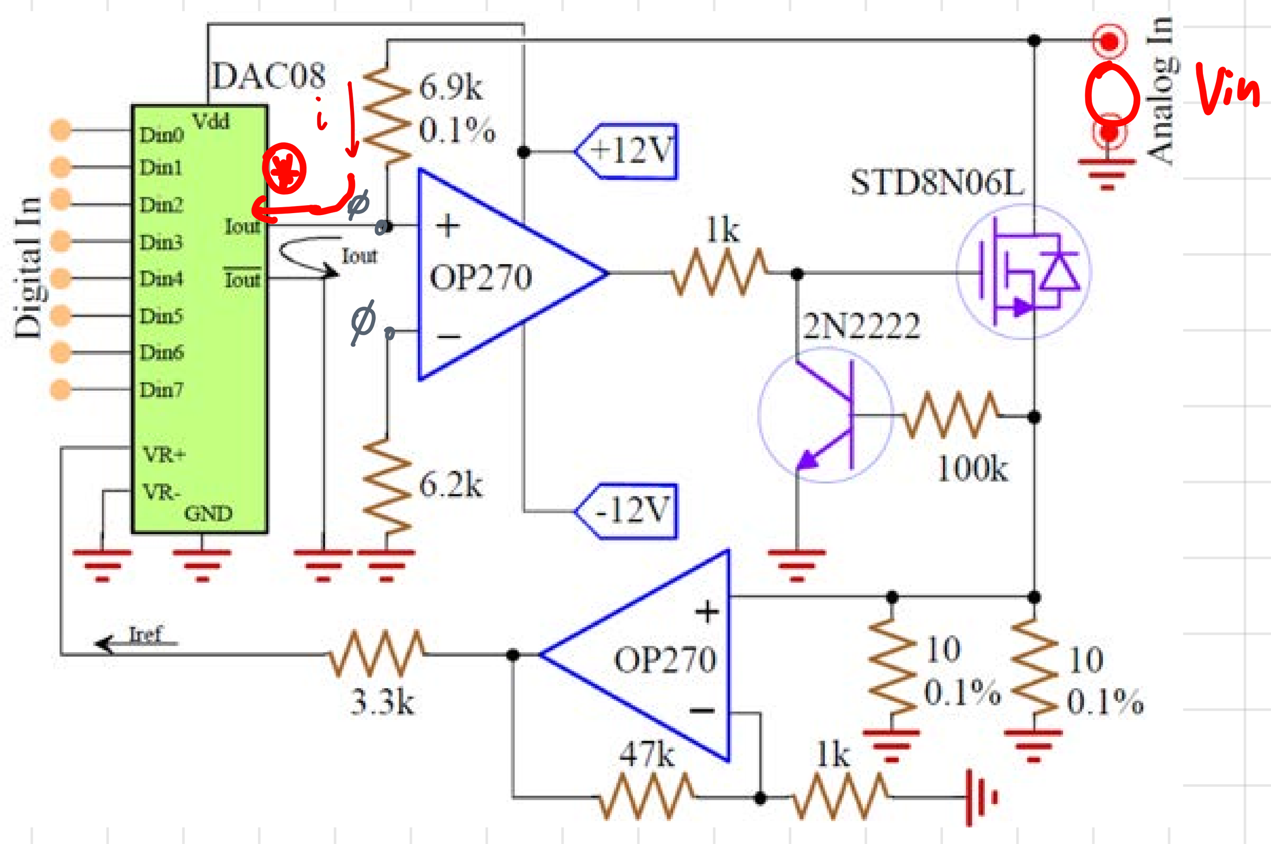
$I_{out} = I_{ref} \cdot \frac{D_{in}}{2^8}$

→ (negative feedback check)

Gain: $1 + \frac{47k}{1k} = 48$

this has finite gain → this OpAmp will have high gain

So consider the signal

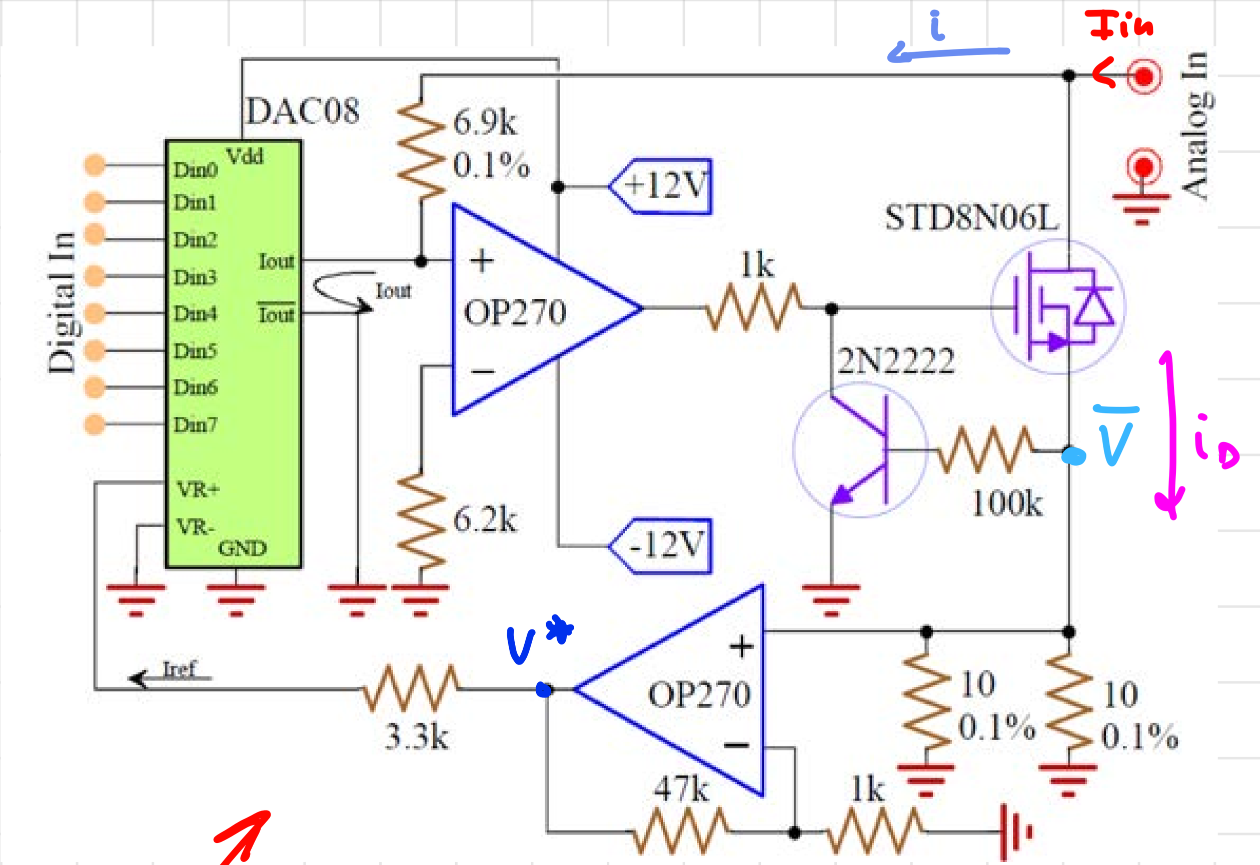


→ Usually we cannot force a current into the DAC because that Iout is the output current of the DAC, so it's like a current generator, BUT with the same considerations done for the negative feedback check we can see that i will increase the voltage on pin +, so the output of that OpAmp, so the input of the second OpAmp, so its output, so i_{ref}, so iout → eventually, thanks to neg. feedback, the DAC output will be:

$i_{out} = i = \frac{V_{in}}{6.9k}$

Given that:

$$\begin{cases} i_{out} = i_{ref} \dfrac{D_{in}}{2^8} \\ i_{out} = \dfrac{V_{in}}{6.9k} \end{cases} \longrightarrow i_{ref} = \frac{V_{in}}{6.9k} \cdot \frac{2^8}{D_{in}}$$



$\rightarrow V^* = i_{ref} \cdot 3.3k$

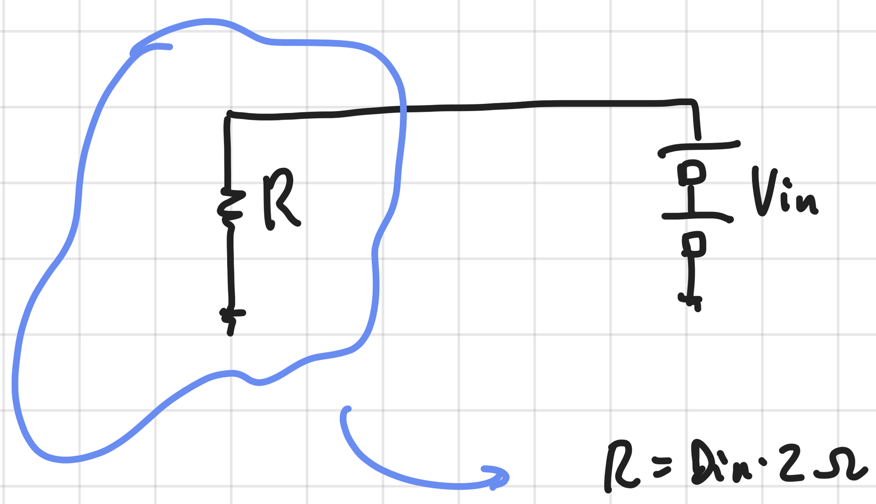
$\rightarrow \bar{V} \cdot 48 = V^* = i_{ref} \cdot \dfrac{3.3k}{48}$

$\rightarrow i_D = \dfrac{\bar{V}}{5\Omega} = \dfrac{3.3k}{5 \cdot 48} \cdot \dfrac{2^8}{6.9k} \cdot \dfrac{V_{in}}{D_{in}} = V_{in} \cdot \dfrac{0.5}{D_{in}} \dfrac{A}{V} = \dfrac{V_{in}}{2\Omega\, D_{in}}$

So consider that $I_{in} = i_{in} + i_D = \underbrace{\cancel{\dfrac{V_{in}}{6.9k}}}_{\text{negligible}} + \dfrac{V_{in}}{2\Omega \cdot D_{in}} \Longrightarrow \dfrac{V_{in}}{I_{in}} = 2\Omega \cdot D_{in}$

It's like a PROGRAMMABLE RESISTOR through D_{in}

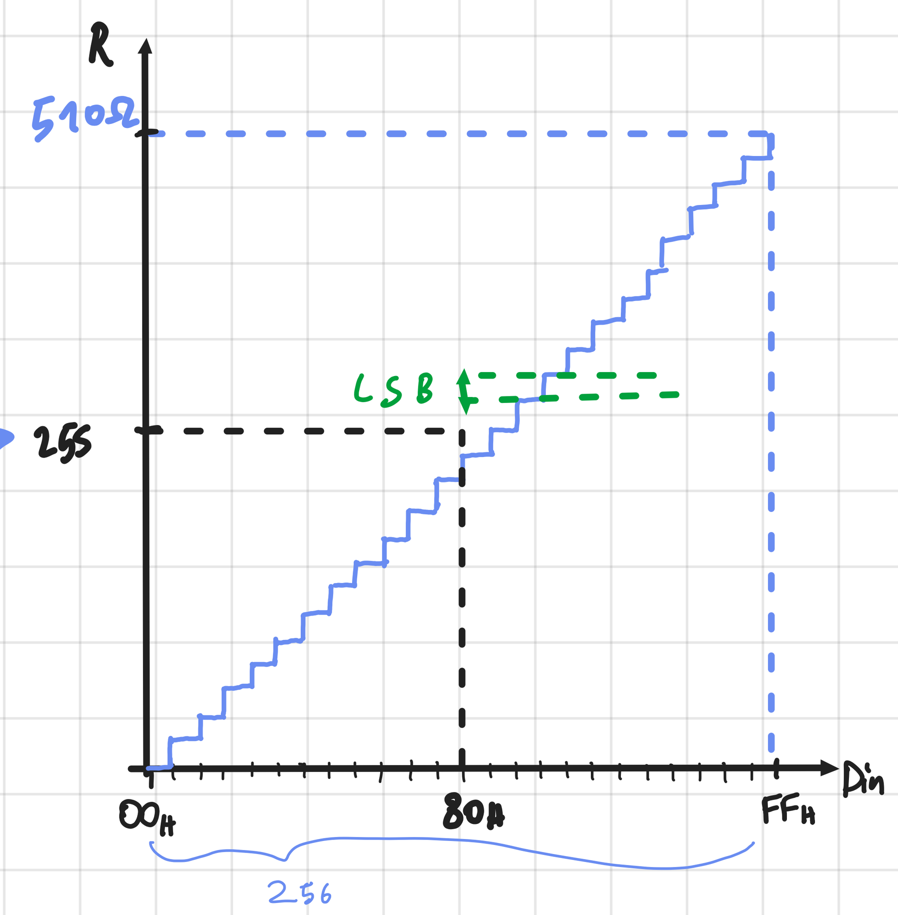
ex.



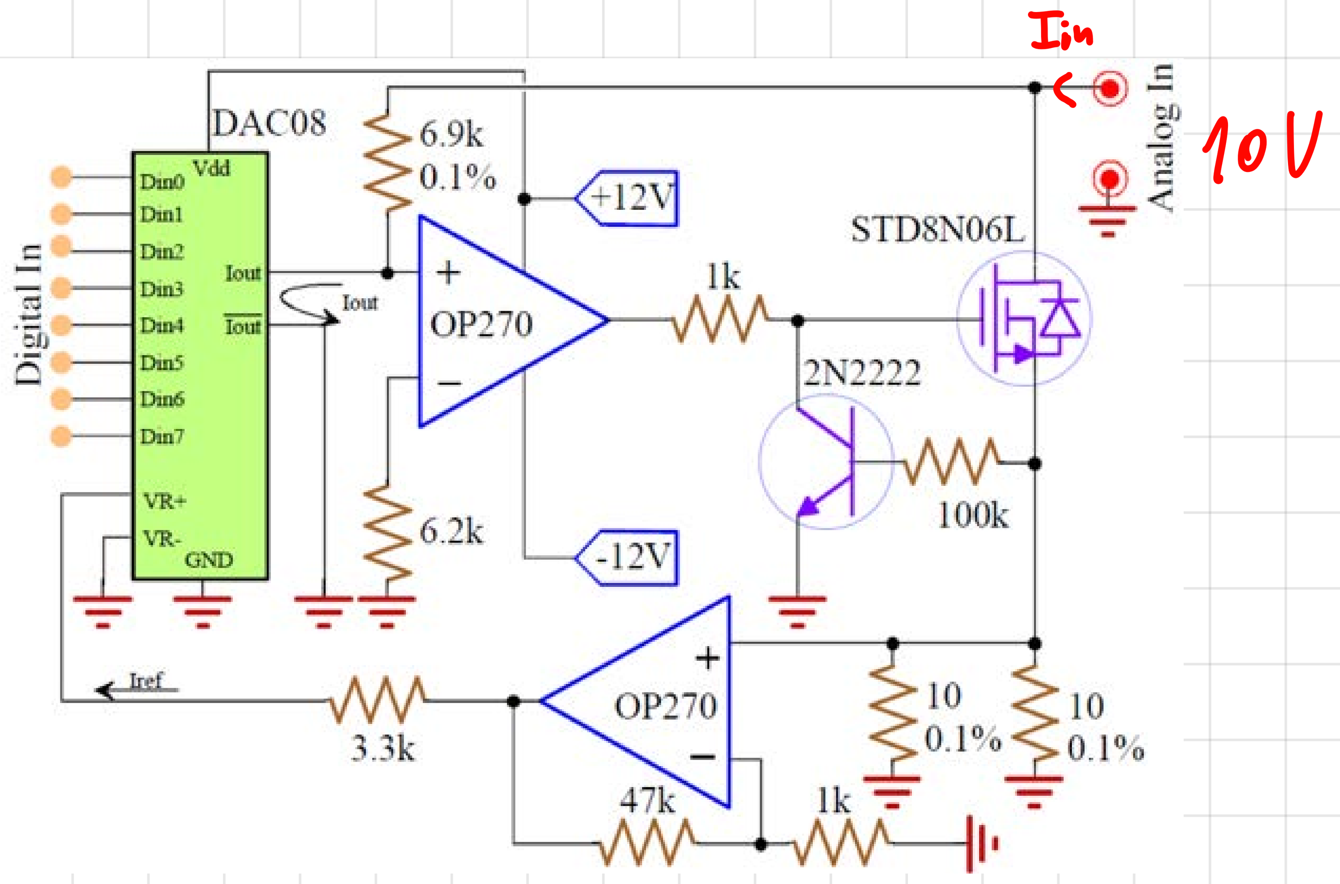
$R = D_{in} \cdot 2\Omega$

R	D_{in}
⌀	00_H
2Ω	01_H
4Ω	02_H
⋮	⋮
510Ω	FF_H

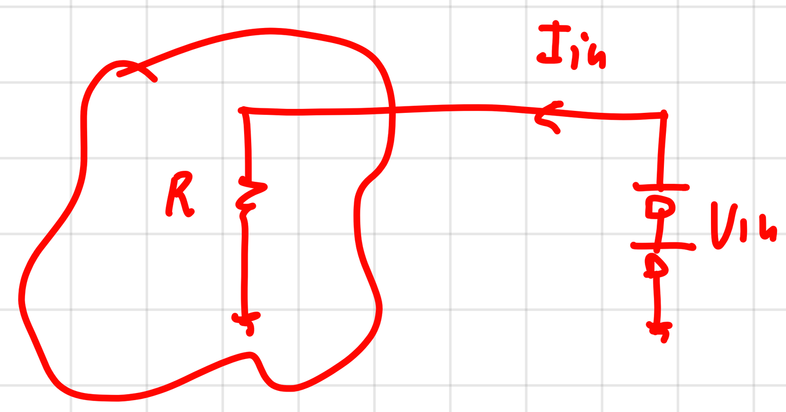
$(2 \cdot 255)$



Let's check if for an input of 10V the circuit is feasible:



$\equiv$

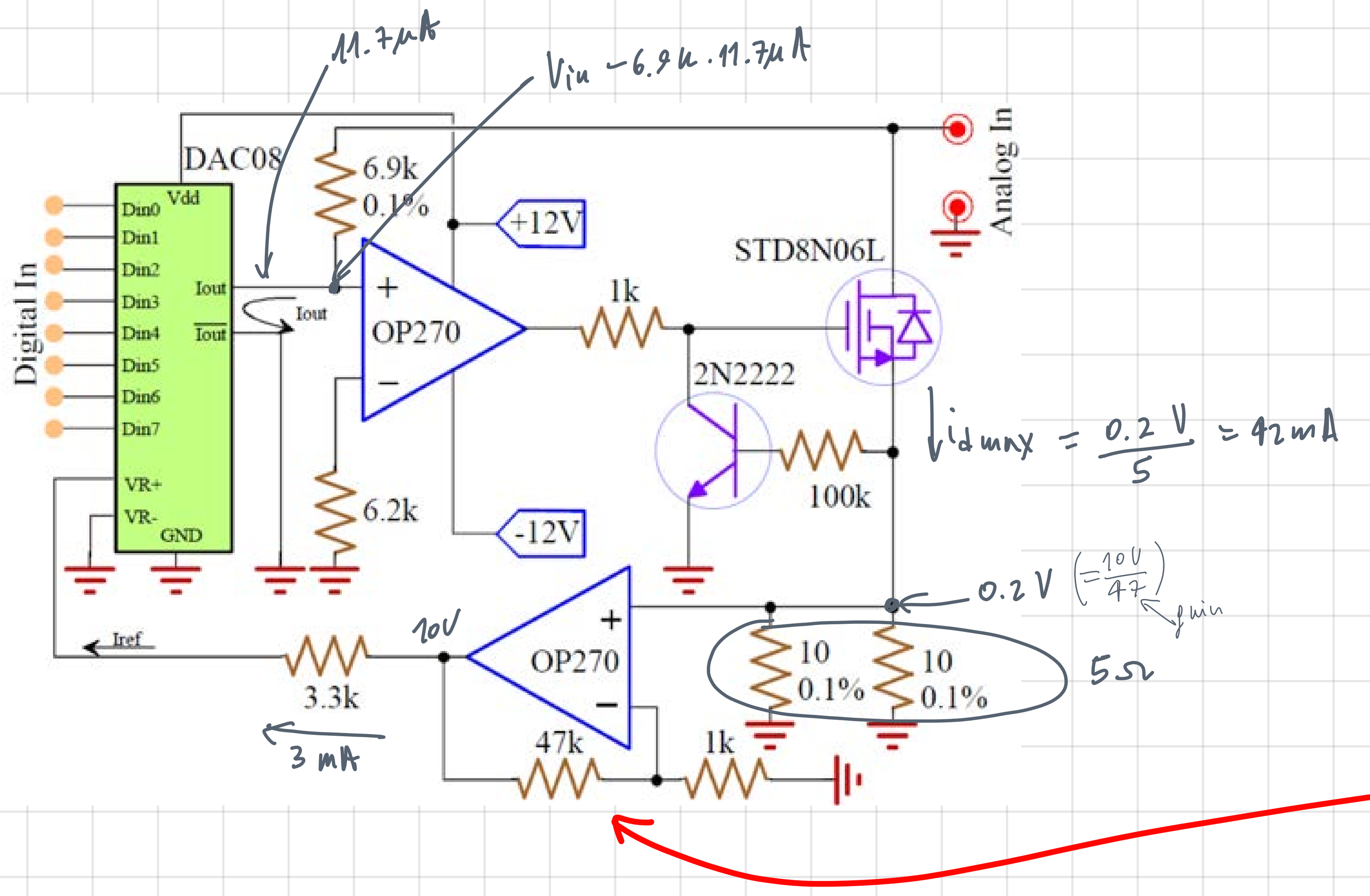


$I_{in} = \dfrac{10V}{255\Omega} = 39mA$ (e.g. for $D_{in} = 80_H$)

↳ we should check the V_{GS} of the MOS is reasonable and if the OpAmp on the TOP can provide it within the saturation

e.g. Consider:

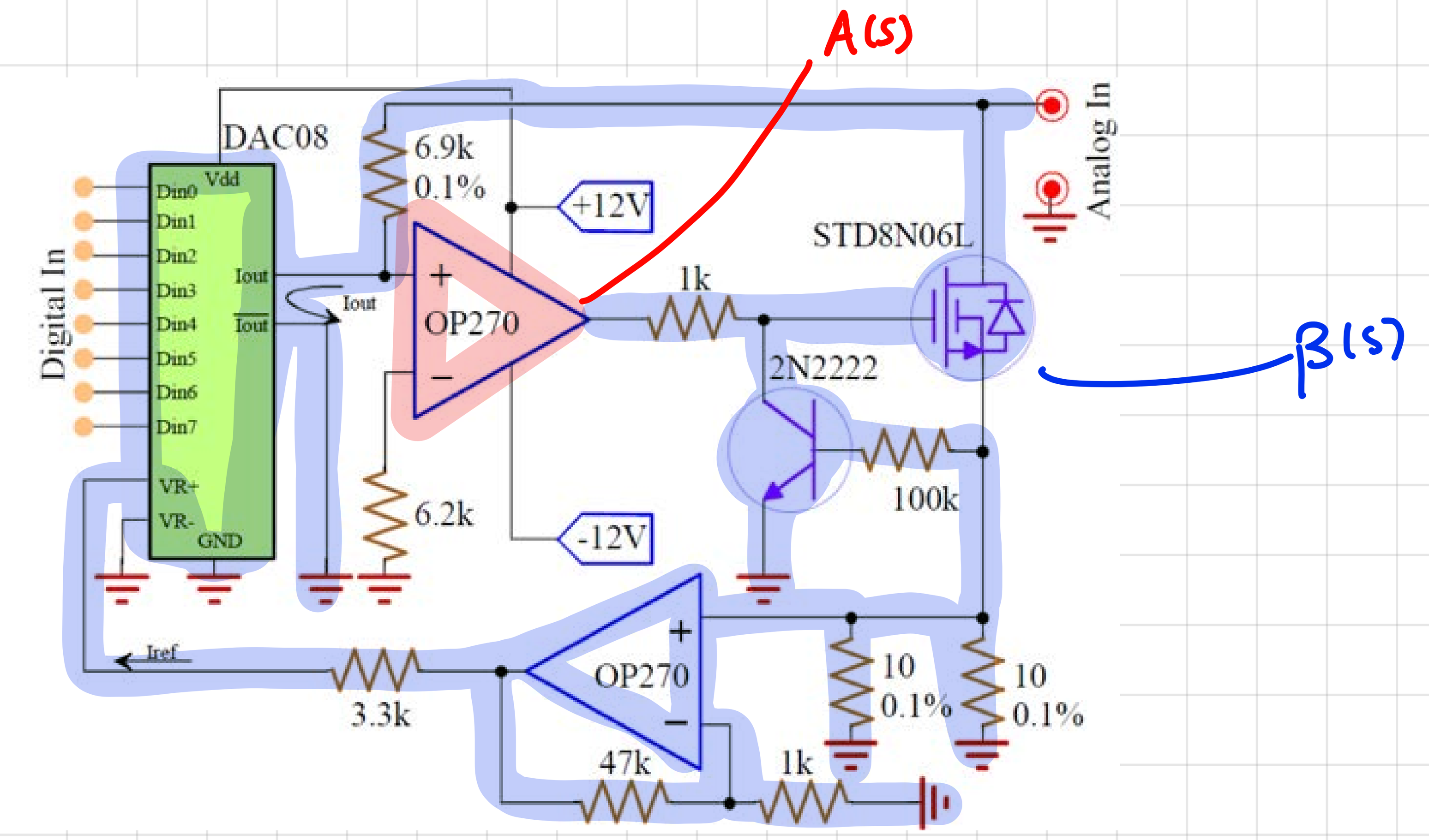
$D_{in} = 01_H$



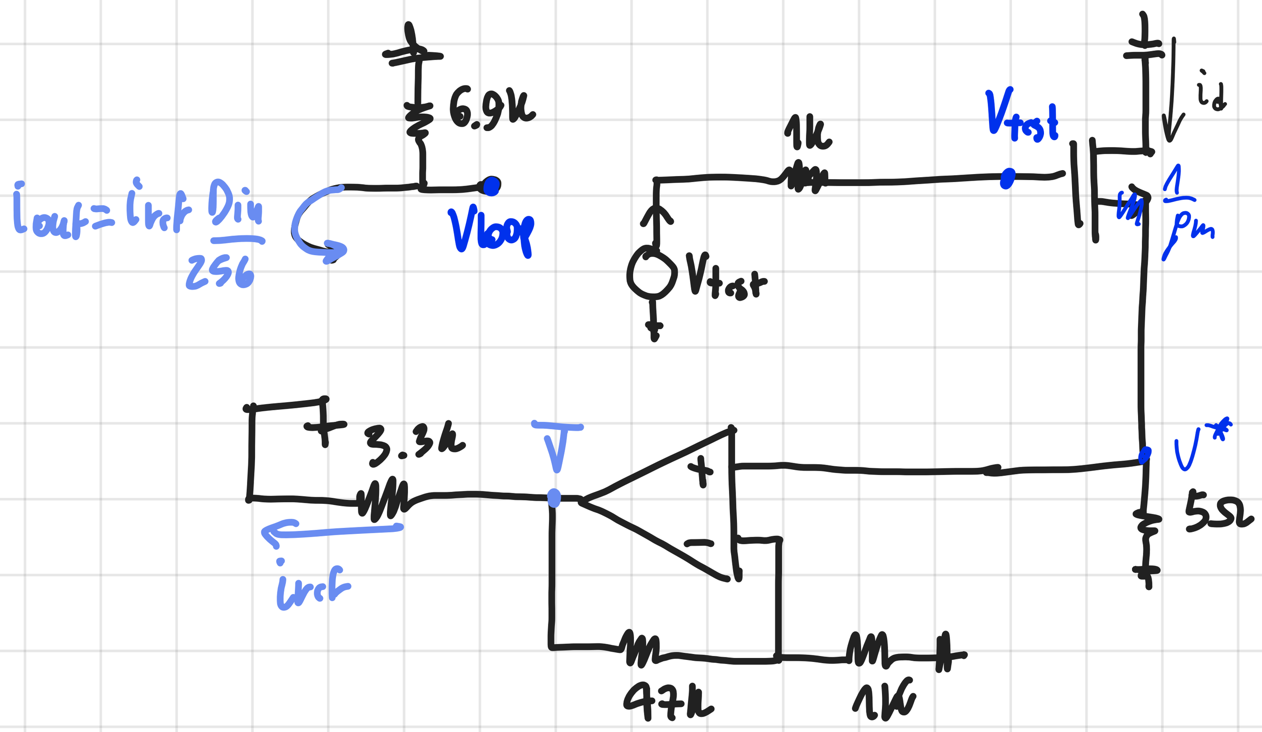
$i_{d\,max} = \dfrac{0.2\,V}{5} = 42mA$

Low if we want a higher max we can reduce the resistors

b)



$\beta(s)$



$$\beta(s) = -\underbrace{\frac{5\Omega}{5\Omega + \frac{1}{g_m}}}_{\text{negligible}} \cdot \frac{48}{3.3k} \cdot \frac{D_{in}}{256} \cdot 6.9k = -0.392 \cdot D_{in}$$

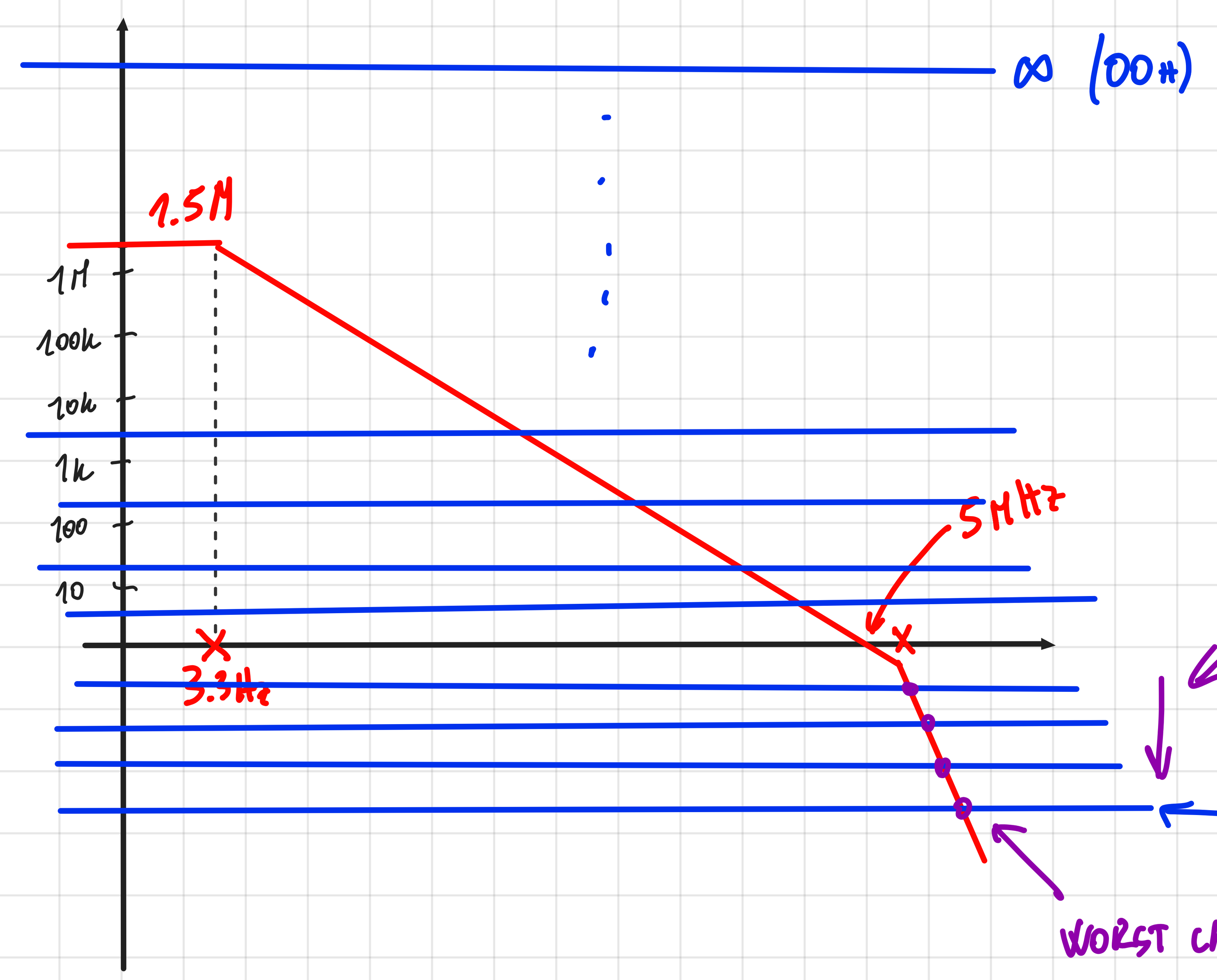
From:

- $V^* = \frac{5\Omega}{5\Omega + \frac{1}{g_m}} V_{test}$ ↳ depends on i_d
- $\bar{V} = V^* \cdot 48$
- $i_{ref} = \frac{\bar{V}}{3.3k}$
- $i_{out} = i_{ref} \cdot \frac{D_{in}}{256}$
- $V_{loop} = i_{out} \cdot 6.9k$

$\hookrightarrow \frac{1}{\beta} = \frac{2.55}{D_{in}}$

$D_{in} = 00_H \to \infty$
$01_H \to 2.5$
⋮
$FF_H \to 0.01$

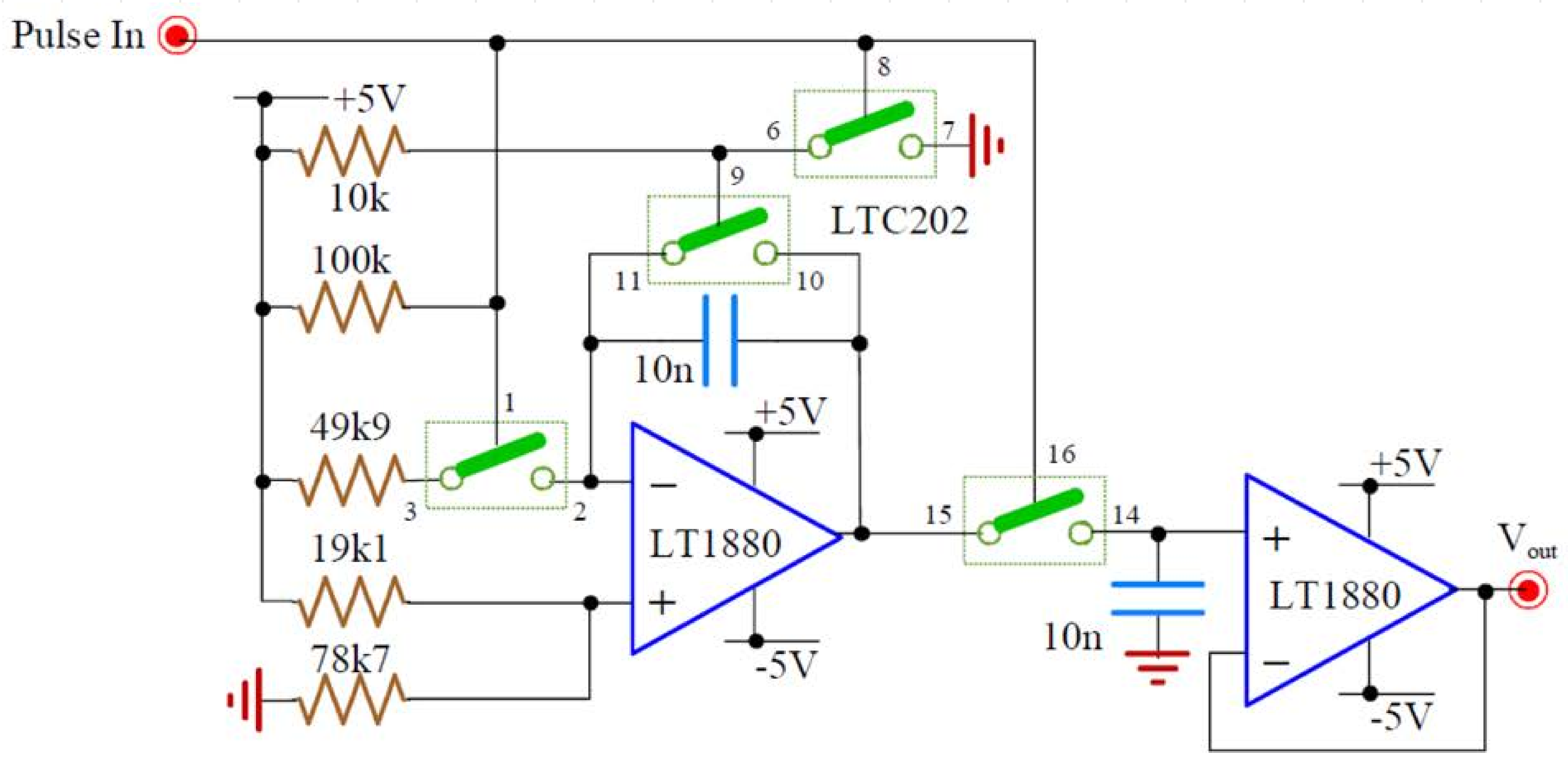
Bode:



from here the circuit becomes unstable

↪ so we have to work with D_{in} small to be stable

③

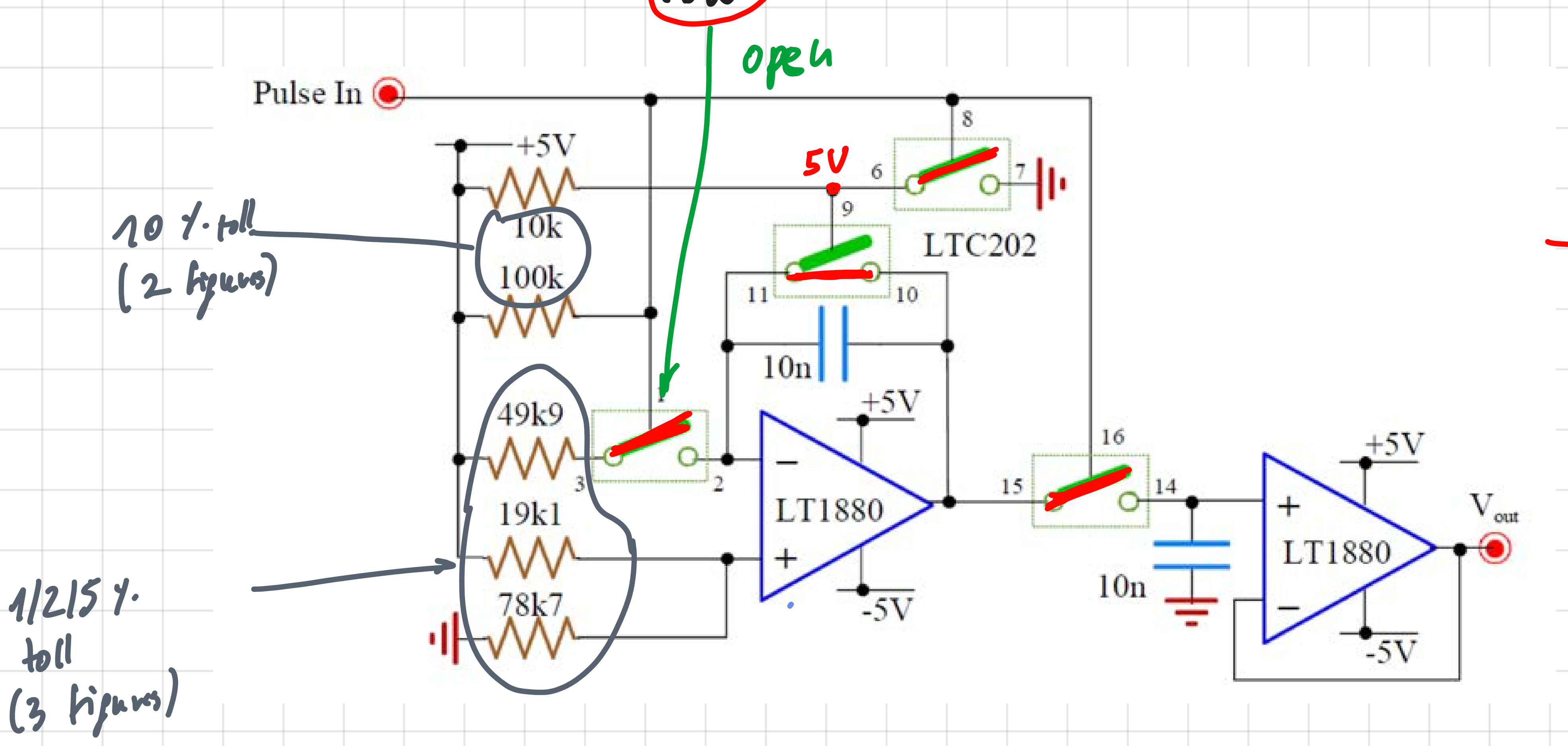


The LTC202 is a quad analog switch (closed when control pin is high). The input is a pulse, whose width T_{high} is in 1ms÷2ms range. The OpAmps have I_B<1.5nA in the -40°C÷+85°C range.

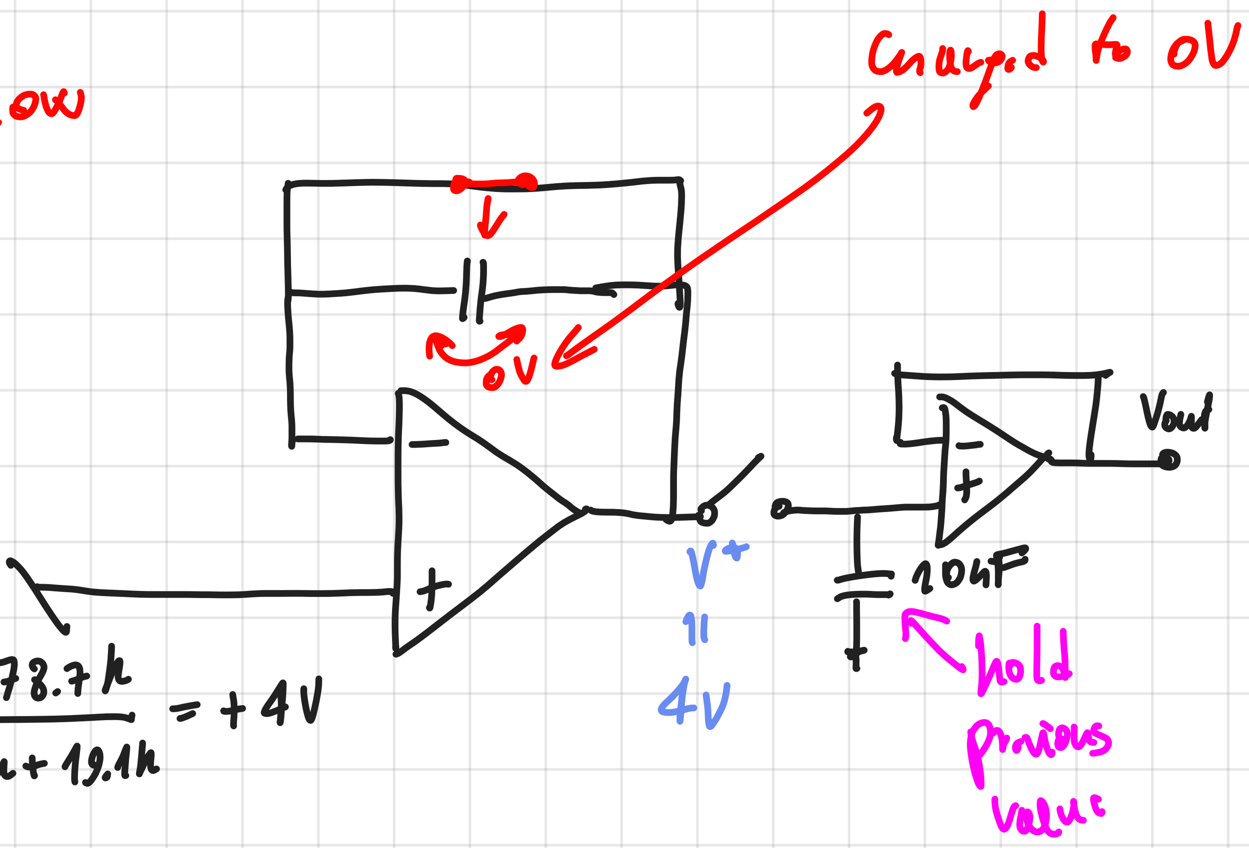
a) Compute V_{out} as a function of T_{high}.

b) Reckon the min T_{low} that guarantees a precision of 1µs.

a) • Consider Pulse In = low

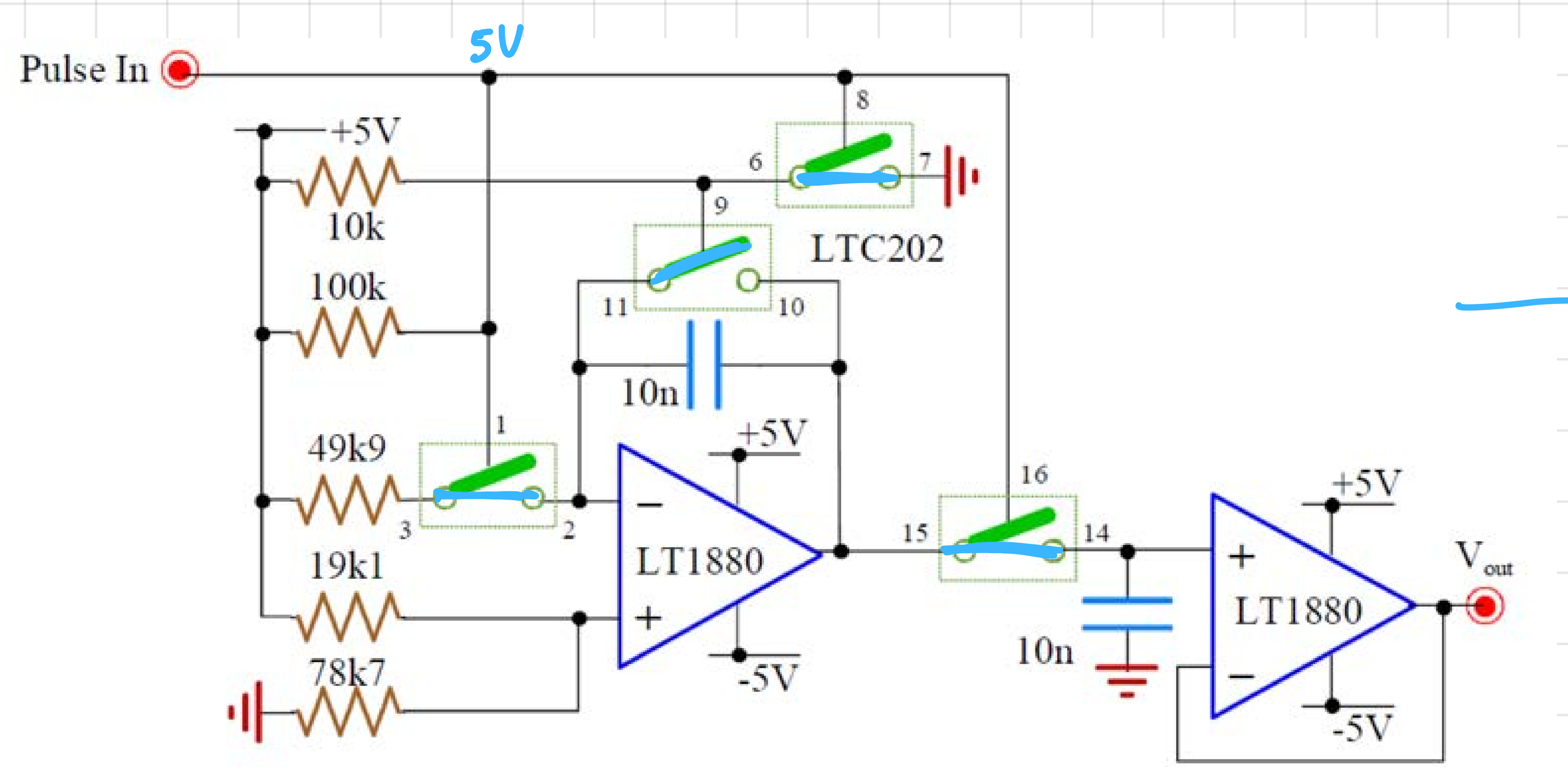


Pulse In = Low

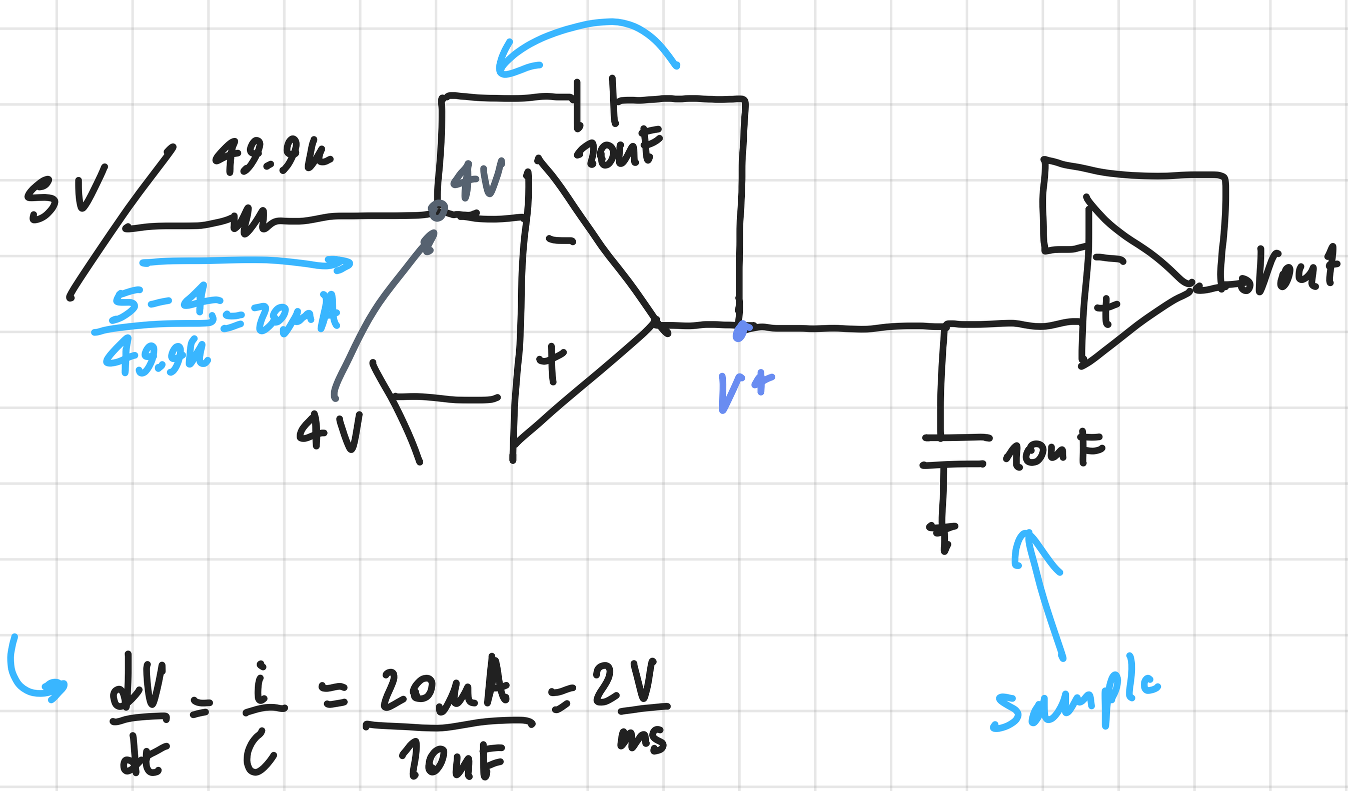


$$V_{ref} = \frac{5V \cdot 78.7k}{78.7k + 19.1k} = +4V$$

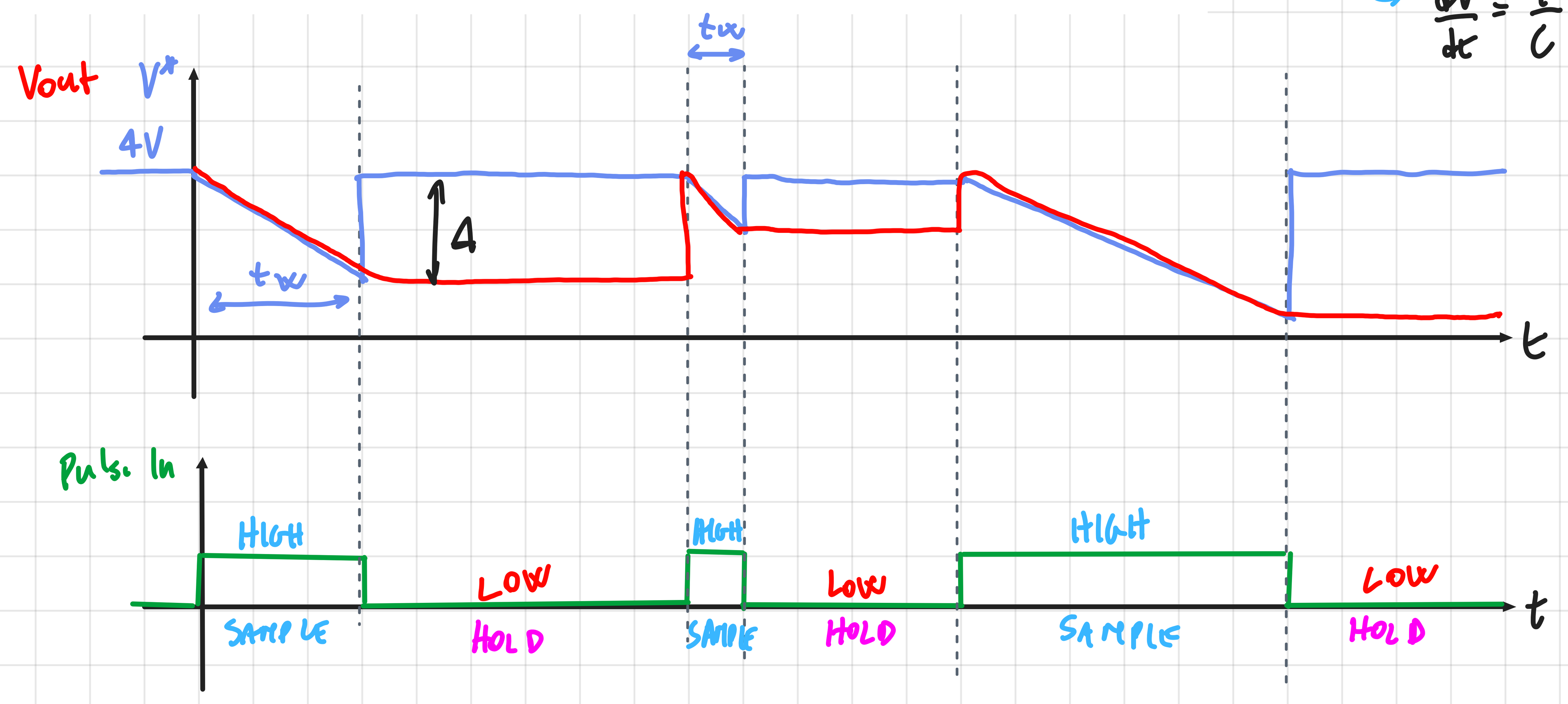
• Consider Pulse In = high (e.g. 5V)



Pulse In = HIGH



$$\frac{dV}{dt} = \frac{i}{C} = \frac{20\mu A}{10nF} = 2\frac{V}{ms}$$



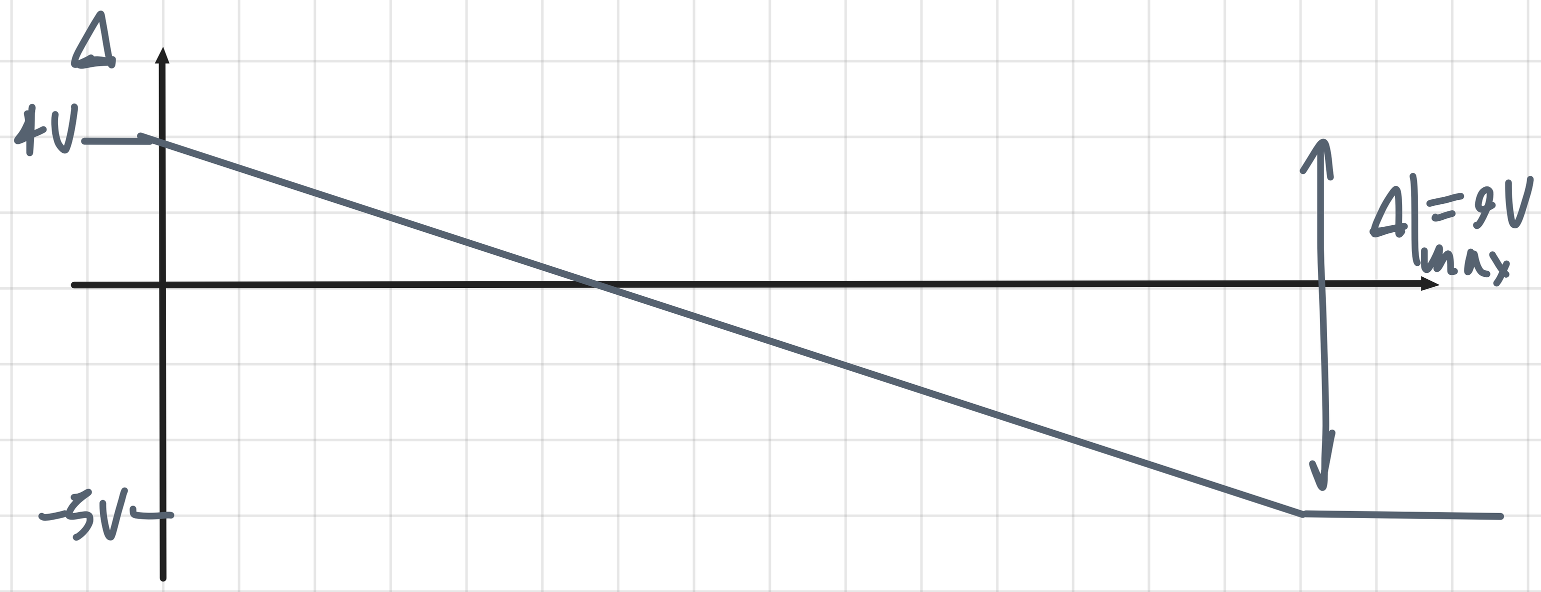
$$\Delta = \frac{dV}{dt} \cdot \underset{(T_{high})}{t_w} = 2\frac{V}{ms} \cdot t_w$$

e.g.
- $t_w = 0$ $\Delta = 0$ → $V_{out} = 4V$
- $t_w = 1ms$ $\Delta = 2V$ → $V_{out} = 2V$
- $t_w = 2ms$ $\Delta = 4V$ → $V_{out} = 0V$

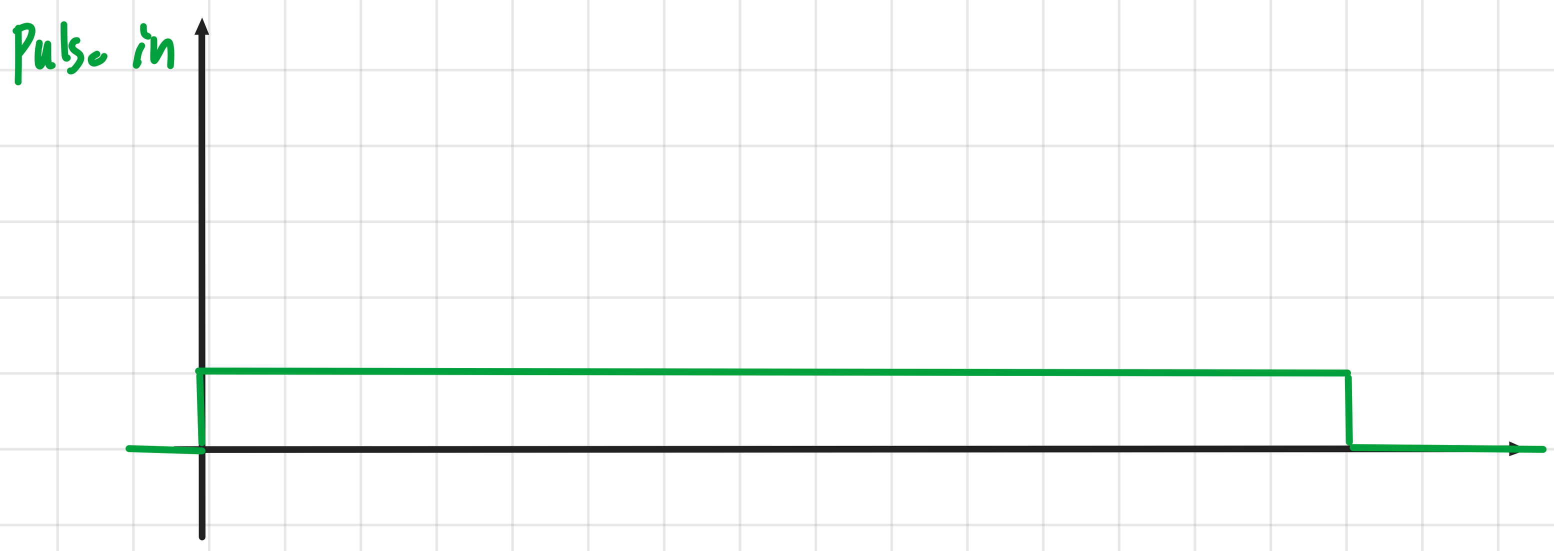
↳ low pulse In ⇒ low Vout

Note: V^+ can go to negative value → If the sample phase is very long

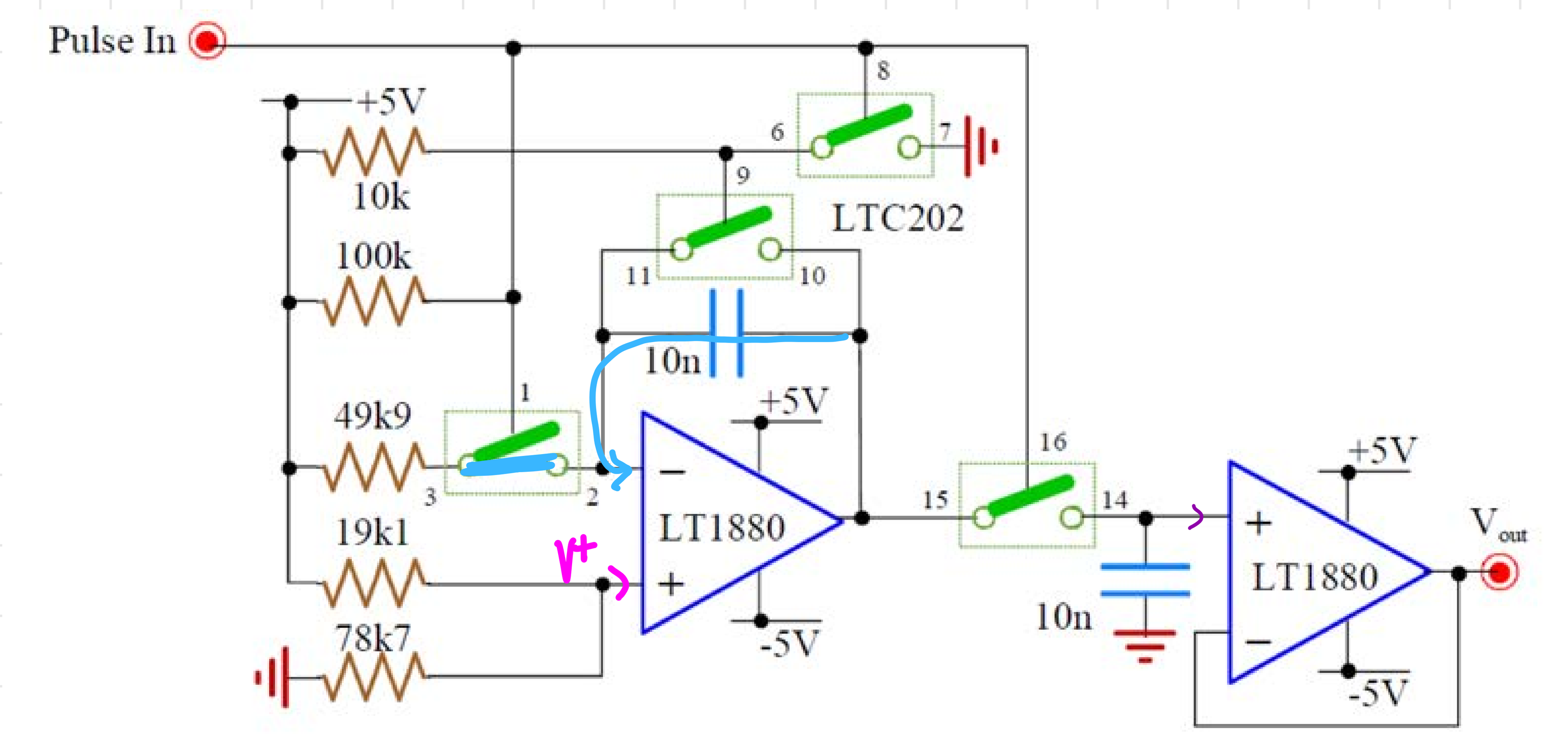
↑ but can't go lower than −5V



→ $t_{width\,max} = \frac{9V}{\frac{dV}{dt}} = \frac{9V}{2\frac{V}{ms}} = 4.5\ ms$



b) Consider the possible errors and tolerances



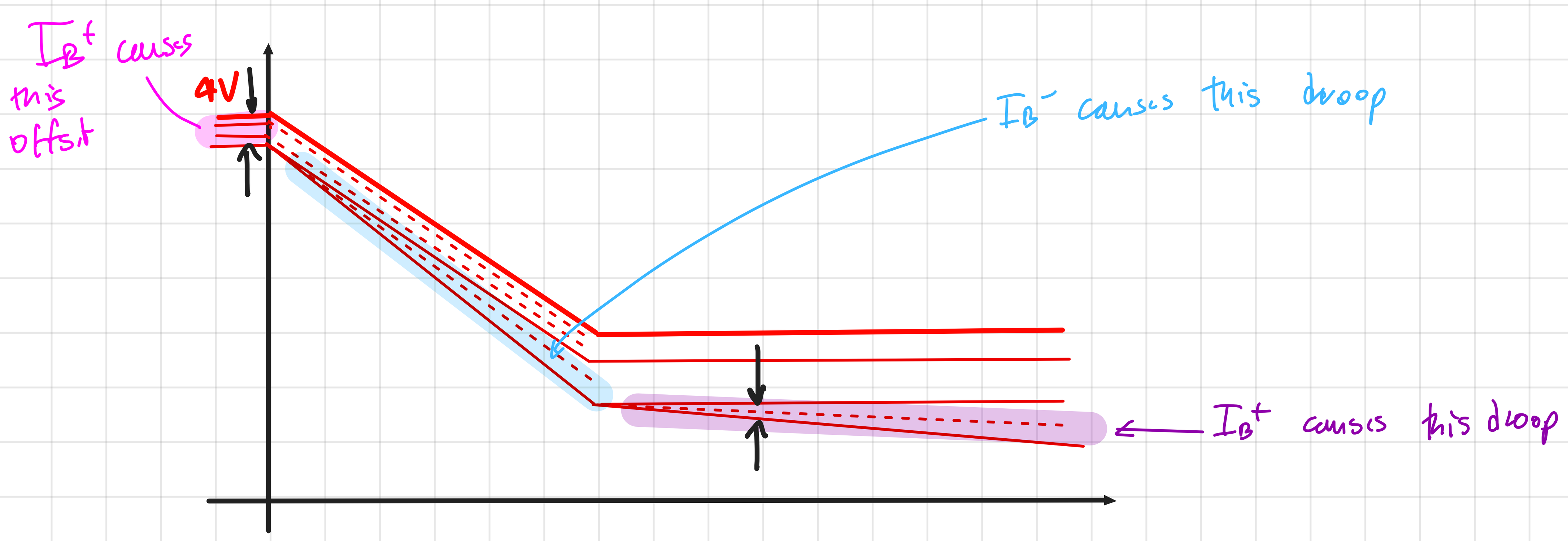
I_B

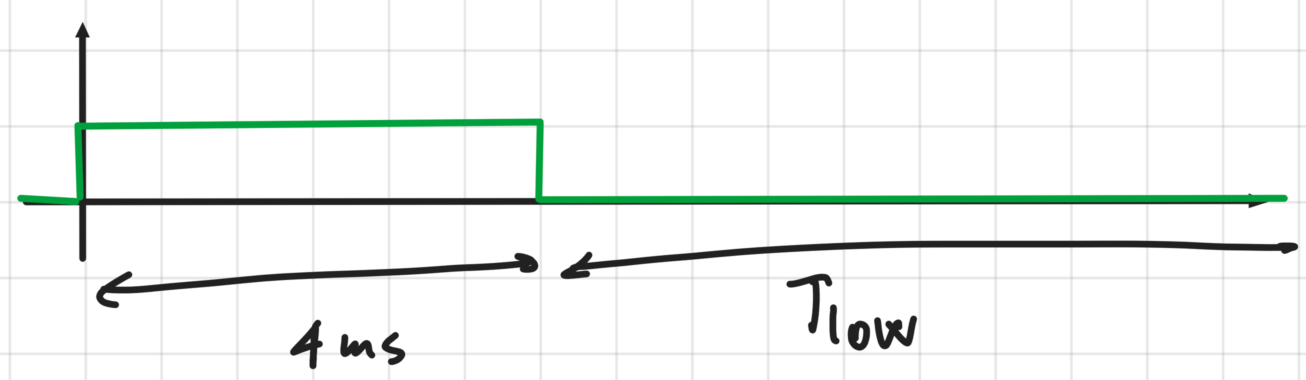
I_B^+ → $V^+ = \mp 4V \underbrace{- I_B(19.1k \,//\, 78.7k)}_{\text{const. error}}$

I_B^- → discharges the capacitor (during SAMPLE)

I_B^+ → discharges the capacitor (during HOLD)

So we'll have:





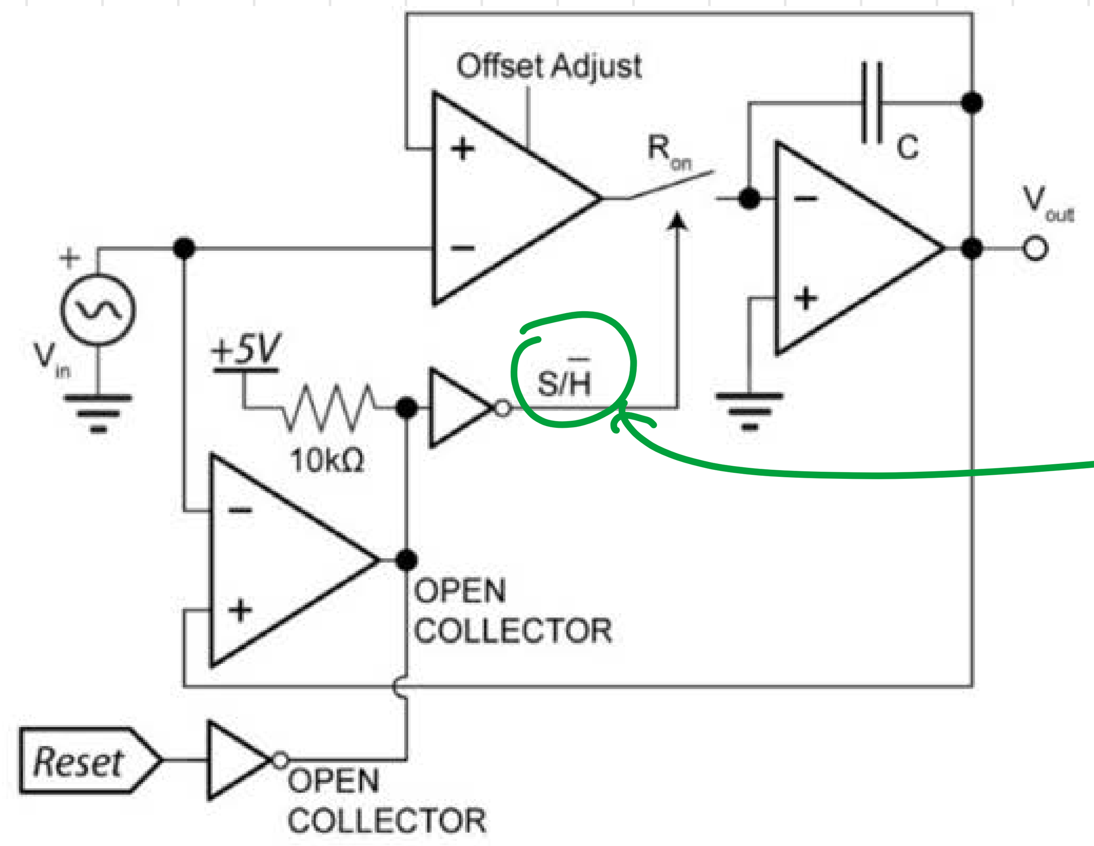
During T_{low} we have I_B^+ and I_B^+ errors must be limited in order to have a precision of $1\mu V$

↳ so error$(T_{on}) \leq 1\mu V$

↑

To DO AT HOME

④



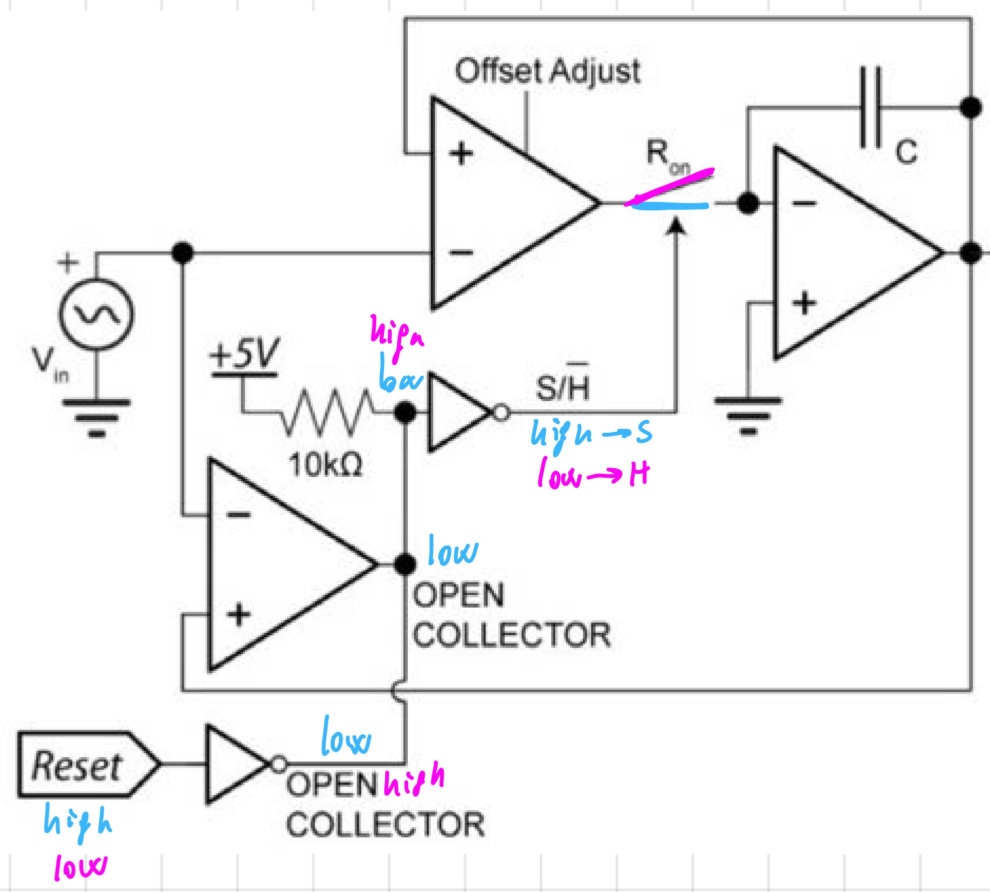
This simbol means is in S when the signal is HIGH
H when the signal is LOW

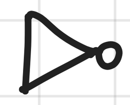
The Offset Adjust pin in set in order to provide a +10mV output offset. $R_{on}=10\Omega$, $C_H=1nF$, GBWP=10MHz. The comparator has open-collector output.

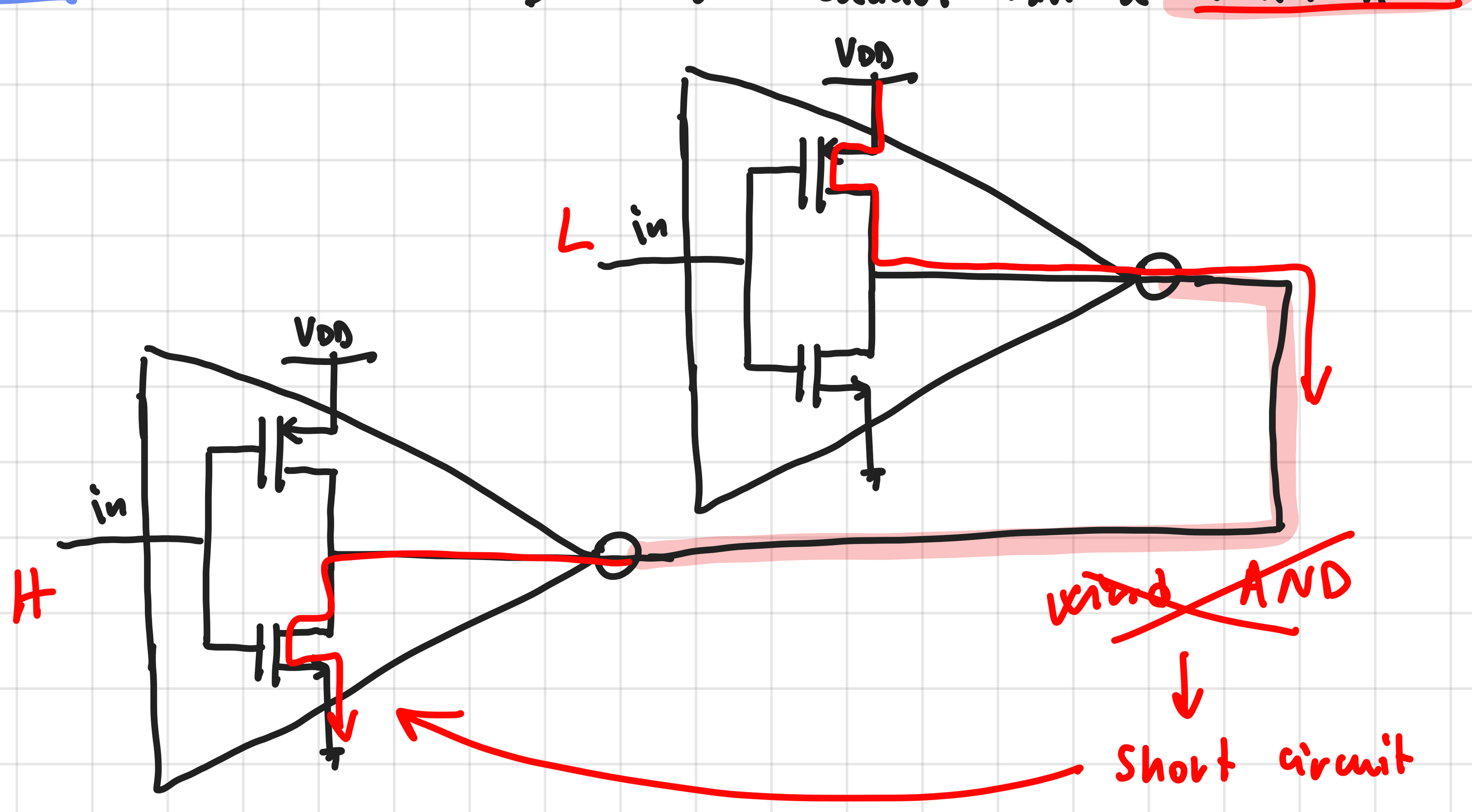
a) Draw the quoted waveforms at all nodes when a triangular input from 0V to 2V is applied at V_{in}, with 1ms period, and a reset pulse of 50% duty-cycle is applied every 1.5ms.

b) Explain the circuit behavior and the role of the offset adjust.

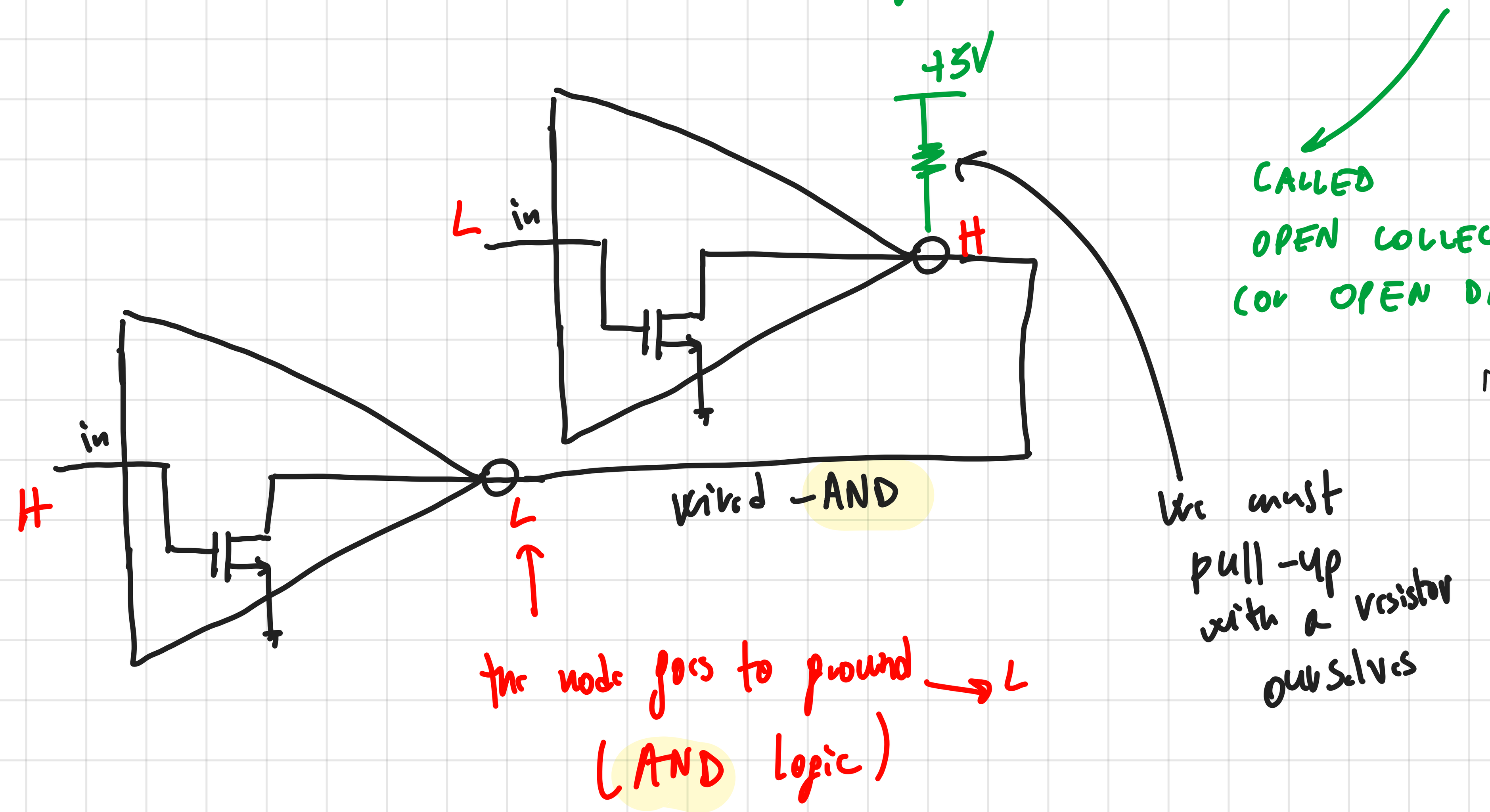
c) Compute the max input frequency that ensures an error lower than 1LSB for a 10bit ADC with FSR=5V.



Note For the inverter  we cannot have a wired-AND



What can we do → we can use drains without the pull-up (p-channel)



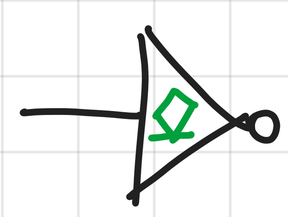
CALLED OPEN COLLECTOR (or OPEN DRAIN)

BJT

MOS

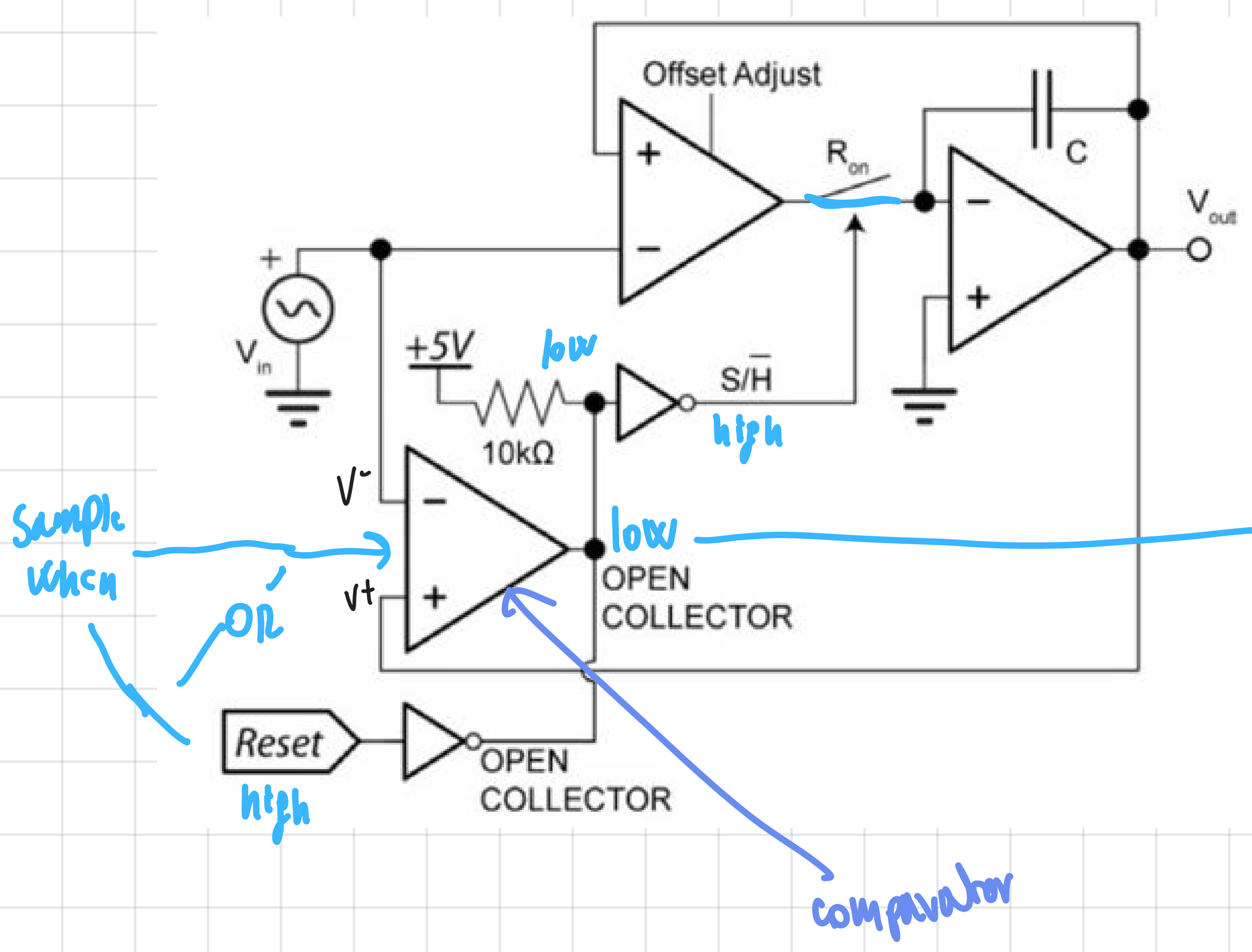
→

Symbol



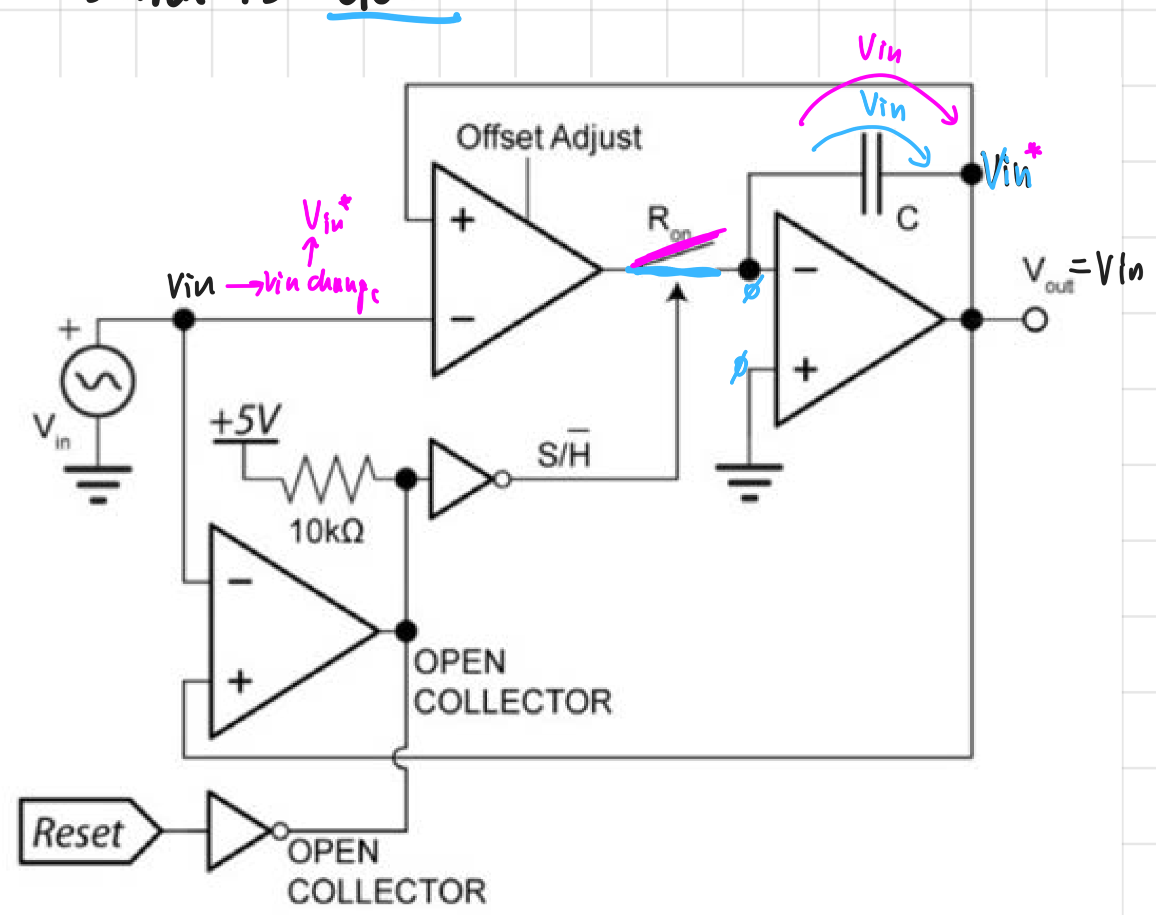
≡ OPEN COLLECTOR GATE

So now let's consider the circuit:

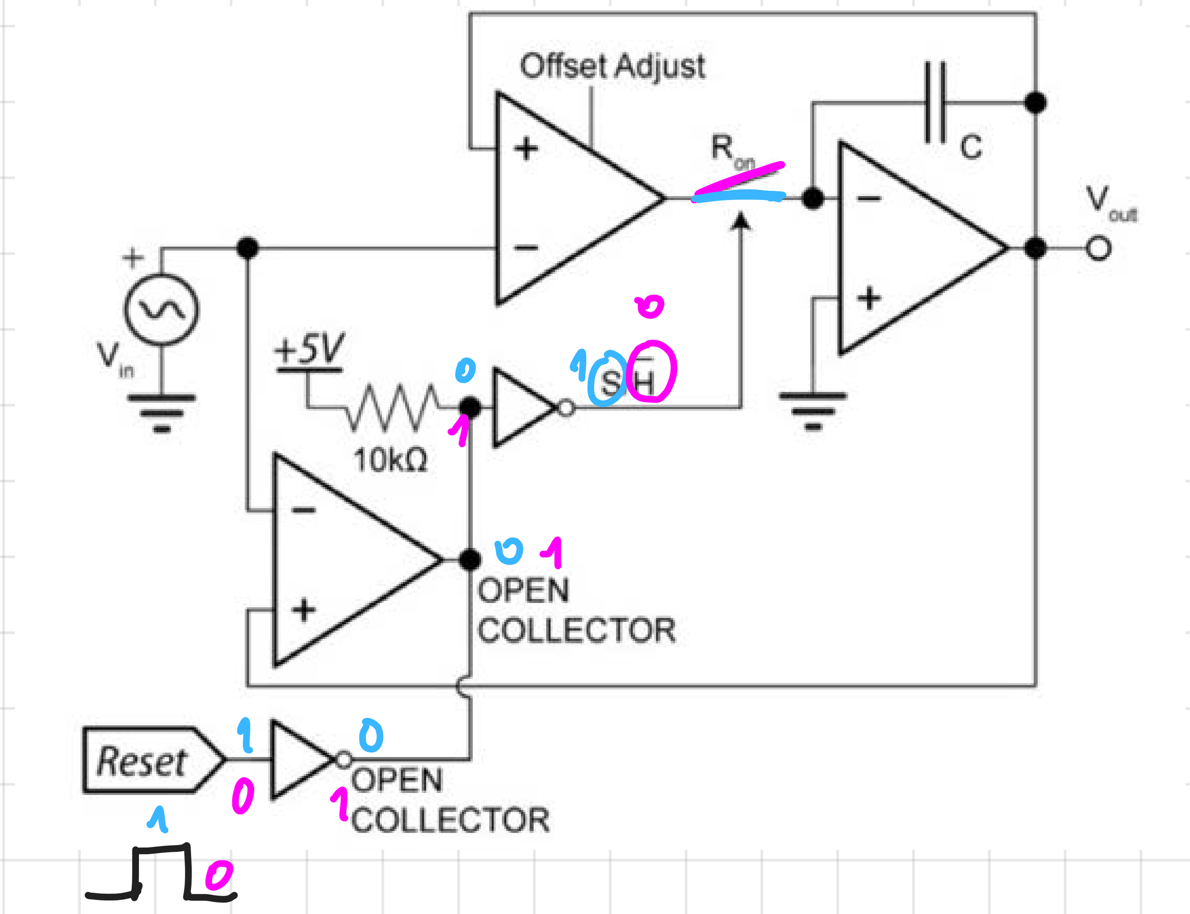


when $V_{in} \; V_{out}$
$V^- > V^+ \Rightarrow V_{in} > V_{out} \rightarrow S$

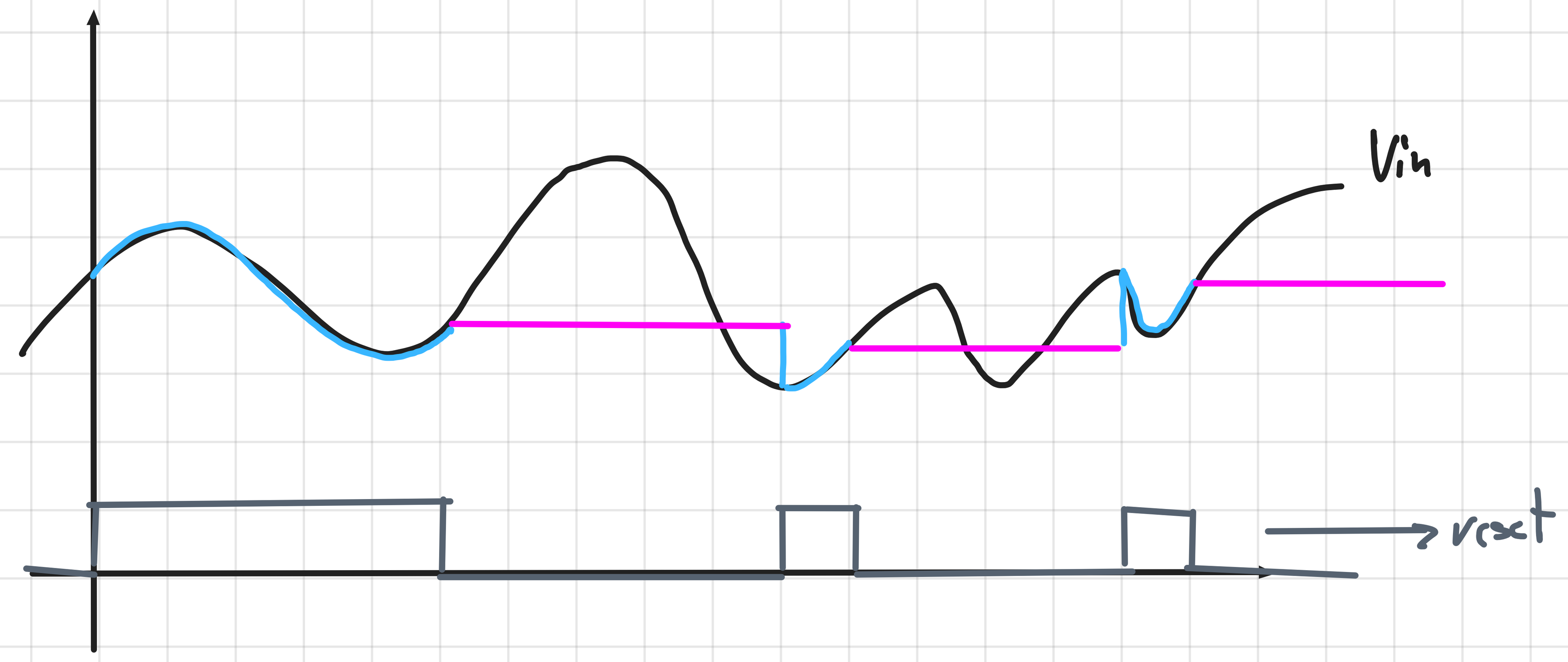
If the switch is close



a)



(Considering without the comparator)



Vout → Vout(S)
Vout(H)

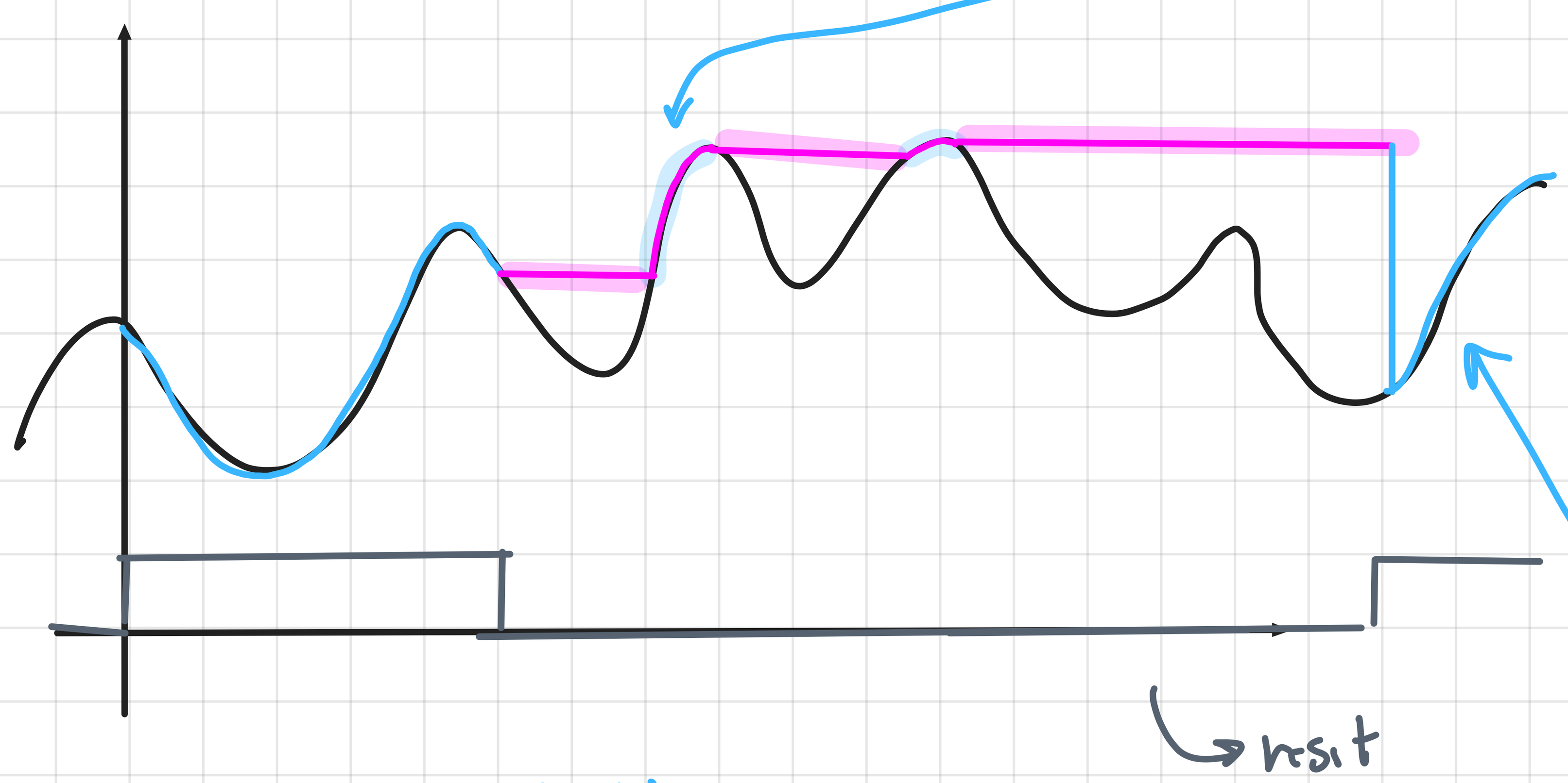
(1=high)
(0=low)

Now consider with comparator $\begin{cases} V_{out} < V_{in} \to S \\ V_{out} > V_{in} \to H \end{cases}$

AND logic that command the switch

b)

↳ So



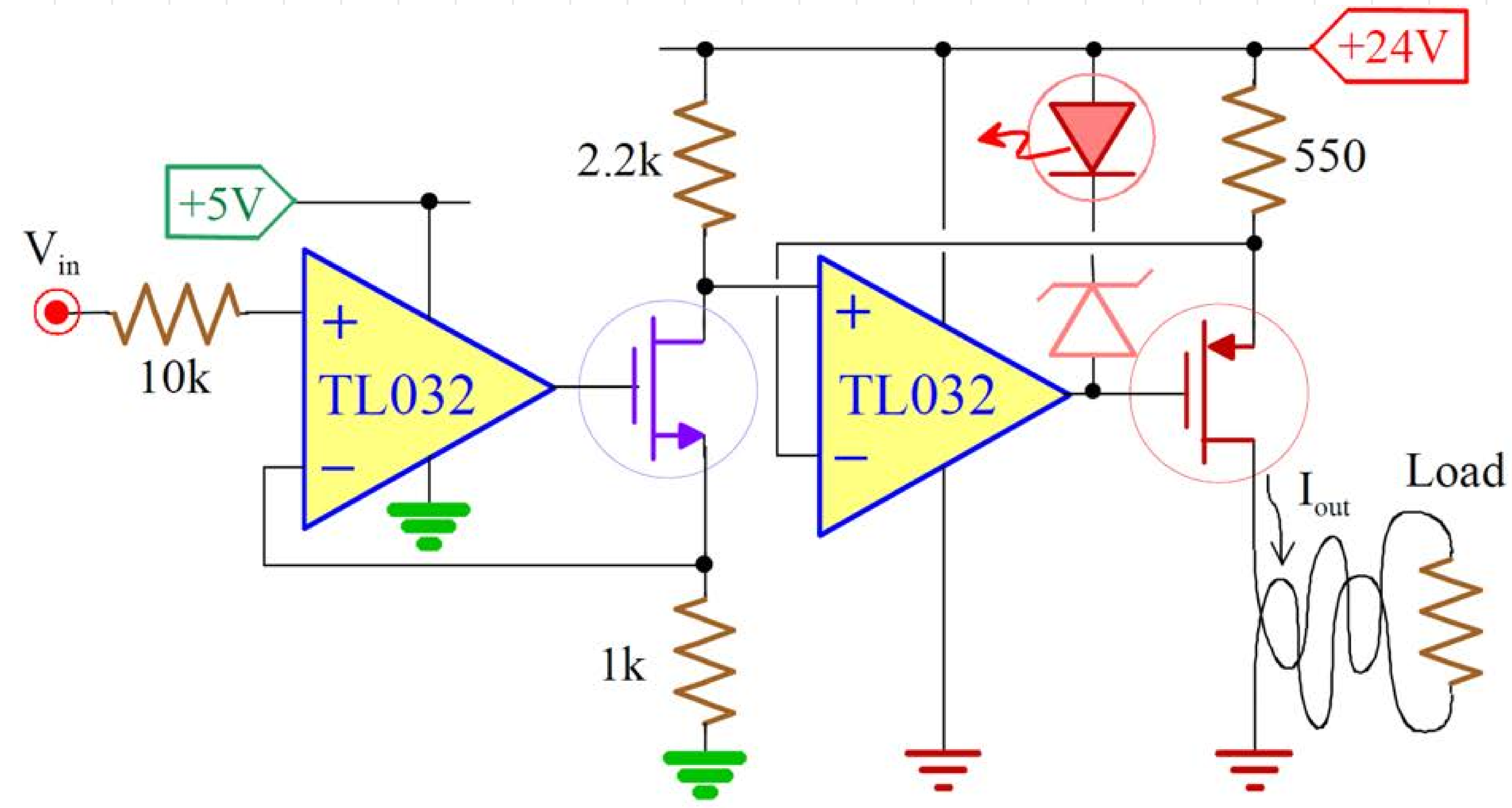
Vout → Vout(S)
Vout(H)

⟹ It's a peak-detector

↓

the reset is useful to reset to sampling values lower than the peak we reached

5



A 5V zener is in series to a 1.5V LED. MOSFETs have V_T=1V and $k=\frac{1}{2}\mu C_{ox}W/L$=2.5mA/V².

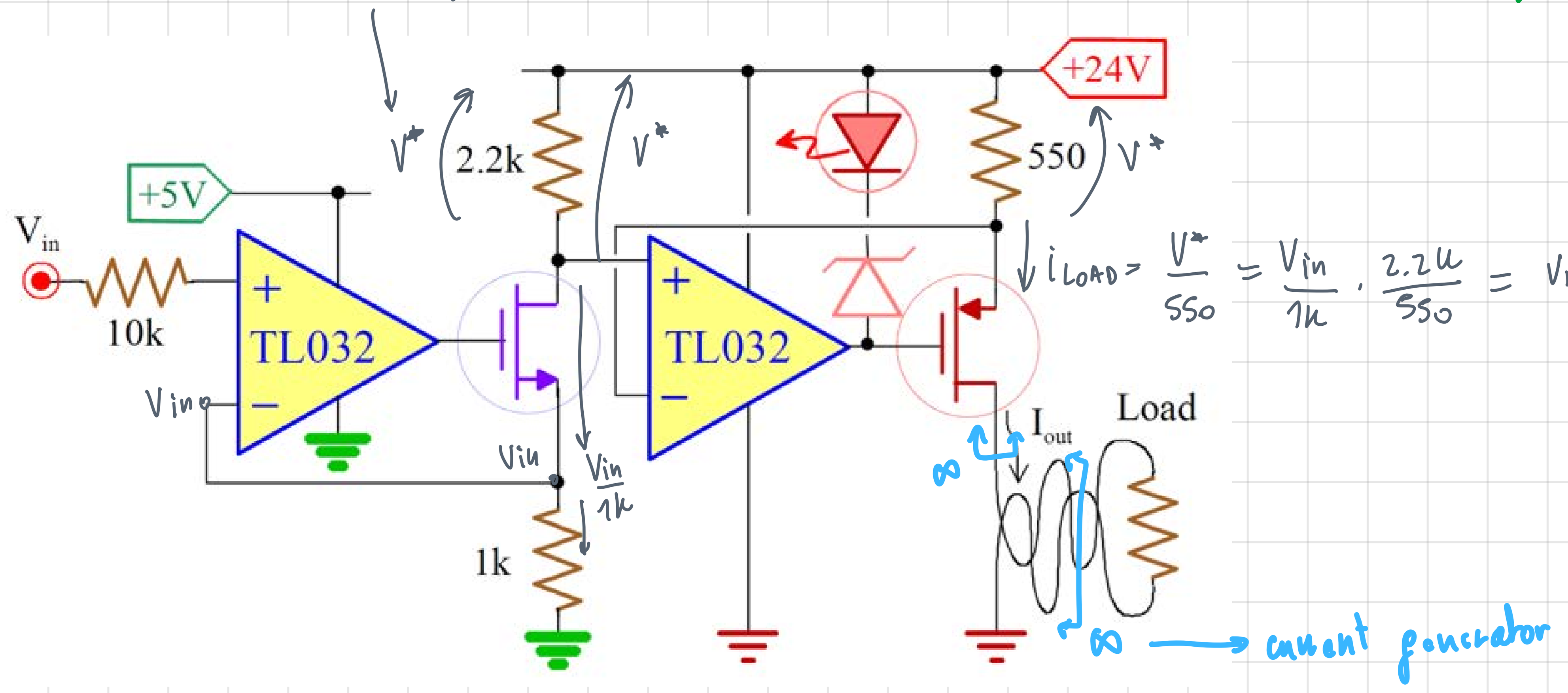
a) Find the relationship I_{out}/V_{in} and the Vin,max that ensures linear behavior for rail-to-rail OpAmps.

b) Change the first stage in order to employ the same +5V power supply, but providing a $V_{in,max}$=+5V.

c) Tell in which conditions the LED will light up and why the circuit is prone to burnings.

(negative feedback check) for both OpAmp

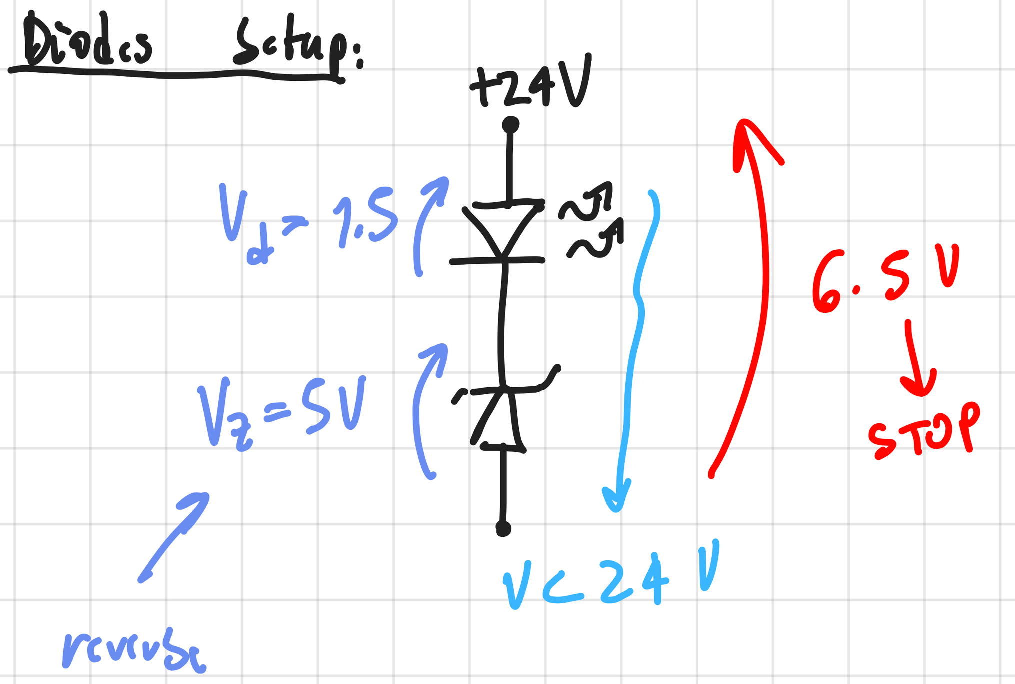
$V^* = \frac{V_{in}}{1k} \cdot 2.2k$



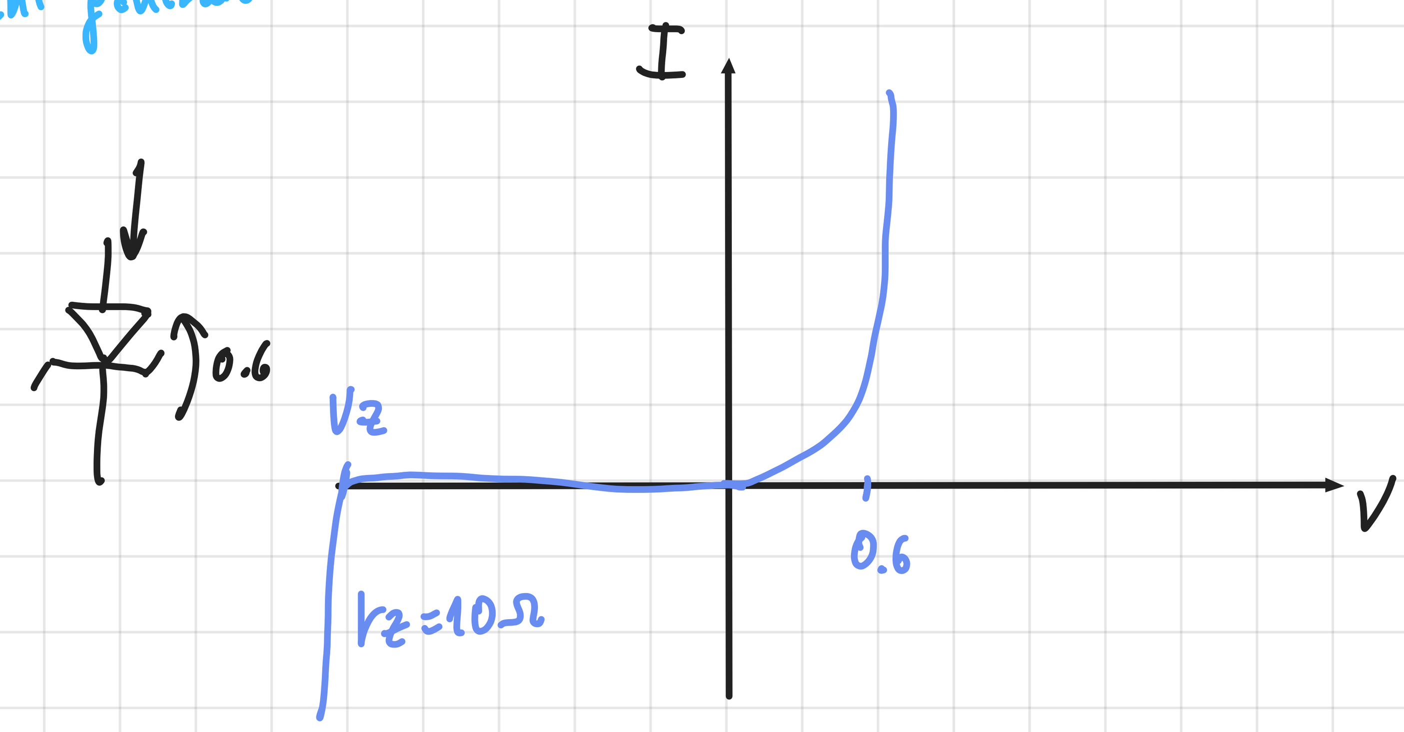
$i_{LOAD} = \frac{V^*}{550} = \frac{V_{in}}{1k} \cdot \frac{2.2k}{550} = V_{in} \cdot \frac{4mA}{mV} \rightarrow \frac{I_{out}}{V_{in}} = \frac{4mA}{mV}$

→ current generator

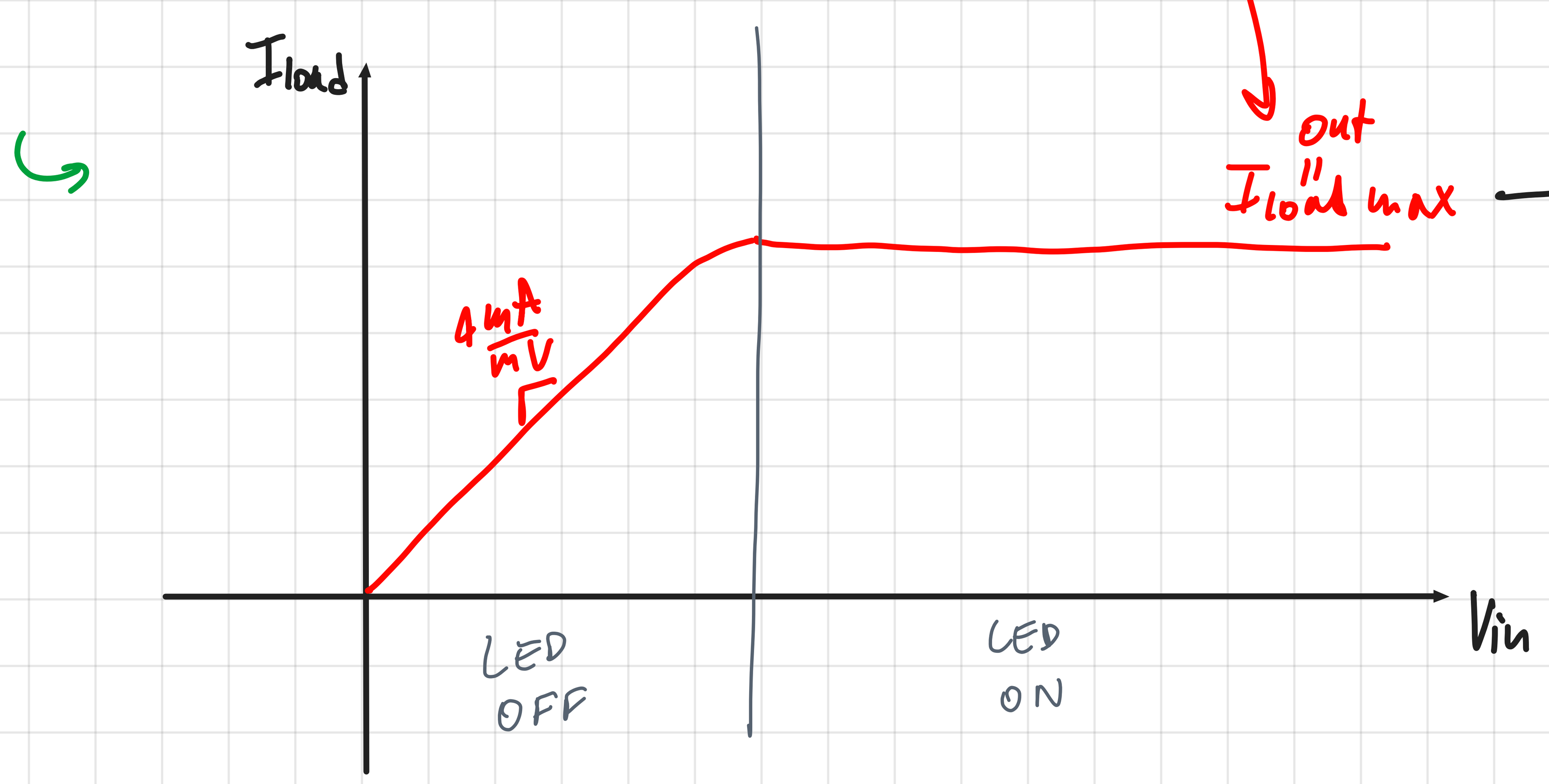
↳ Diodes setup:



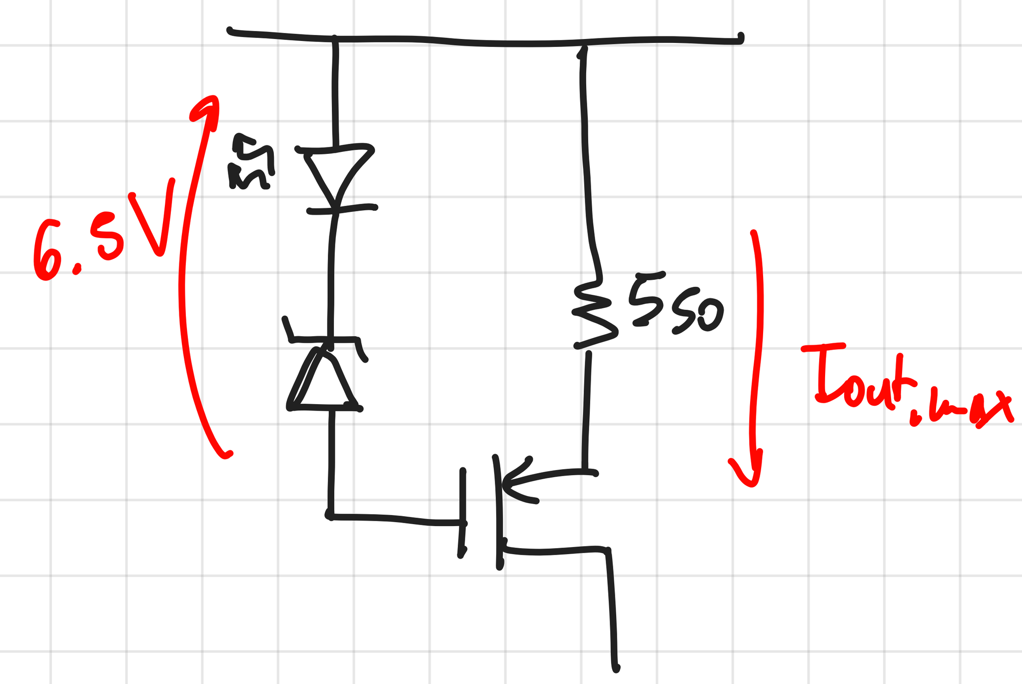
Zener:



when



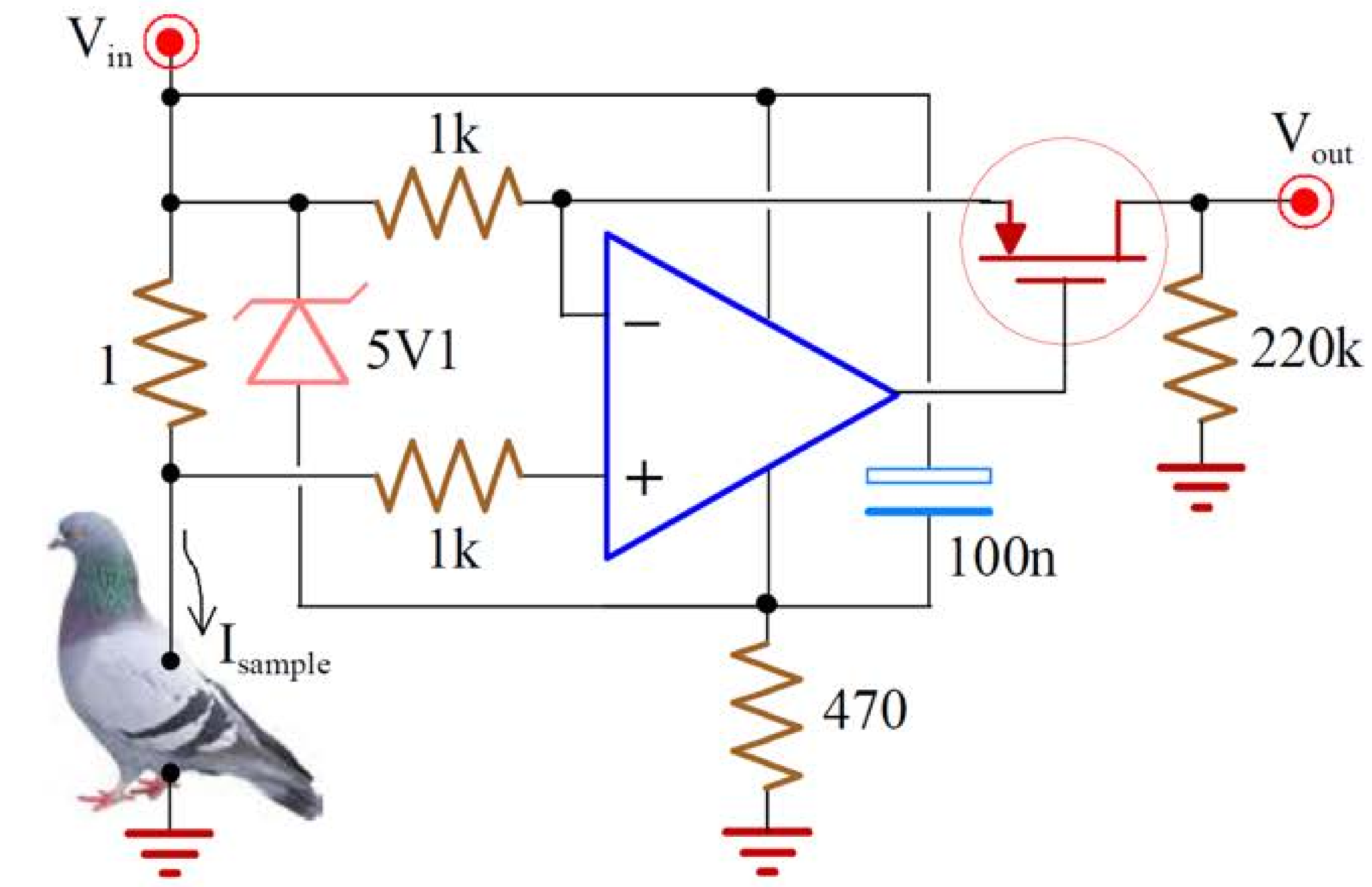
→ To compute it:



$$I_{outmax} = k \cdot OD^2 = k\,(\underbrace{6.5V}_{V_G} - 550 \cdot \underbrace{I_D}_{I_{outmax}} - V_t)^2$$

↳ solve this 2nd order eq. ⟹ I_{outmax}

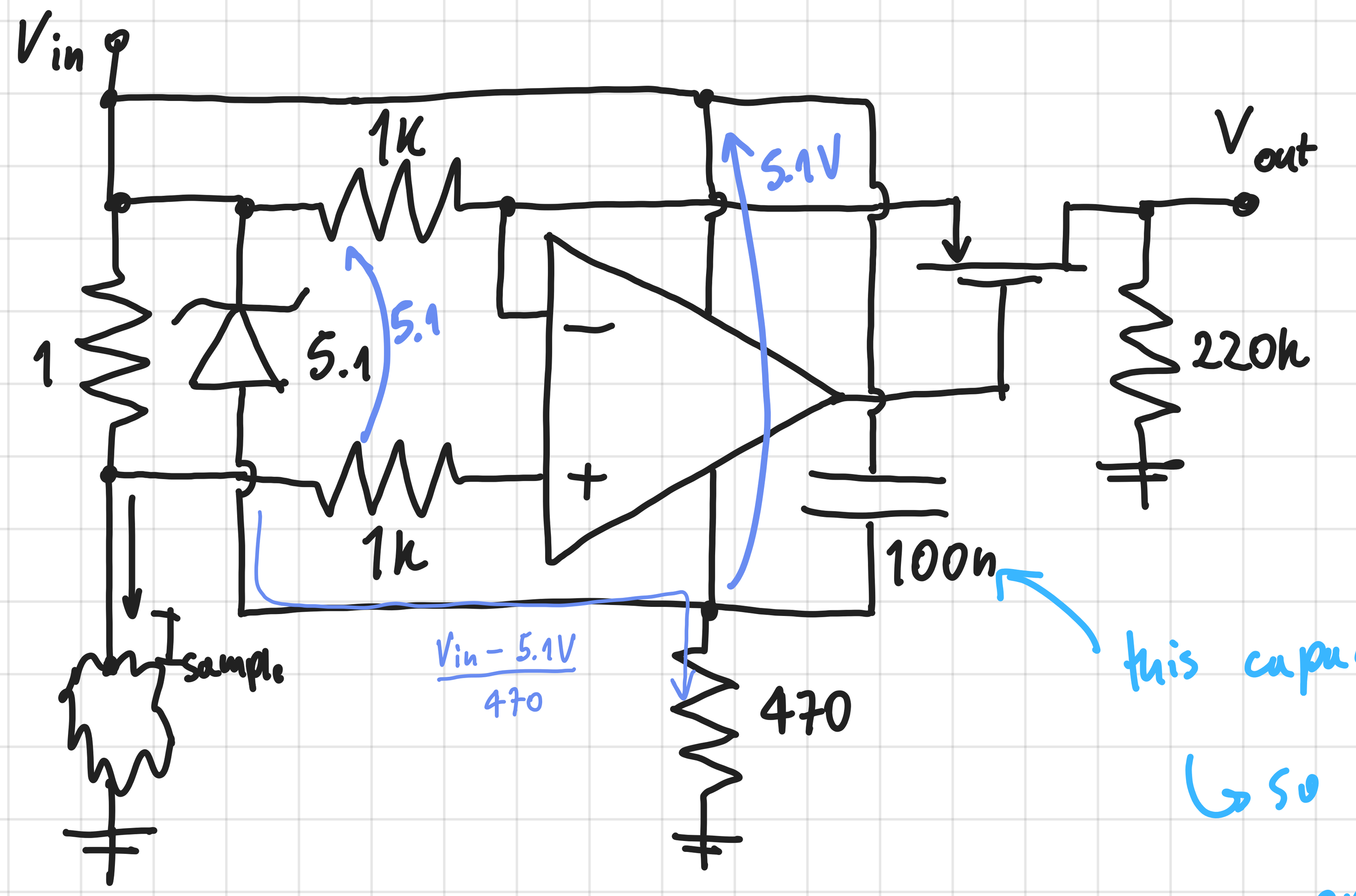
(6)



a) Compute the relationship between Vout and Isample.

b) Design a new stage employing OpAmps that instead forces a constant current I_{sample}=10mA through the sample and measures the voltage developed across it with a gain of +20.

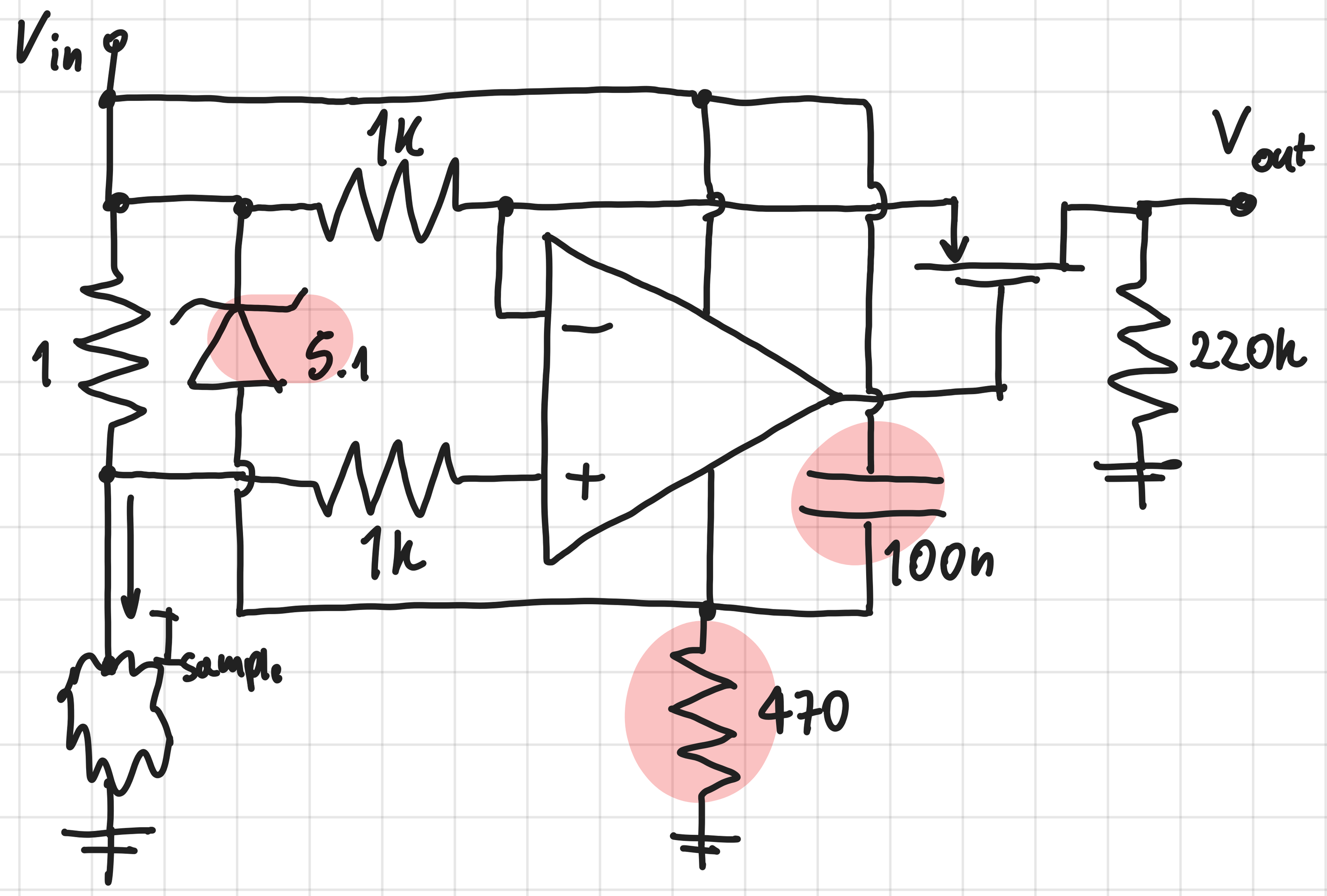
a)

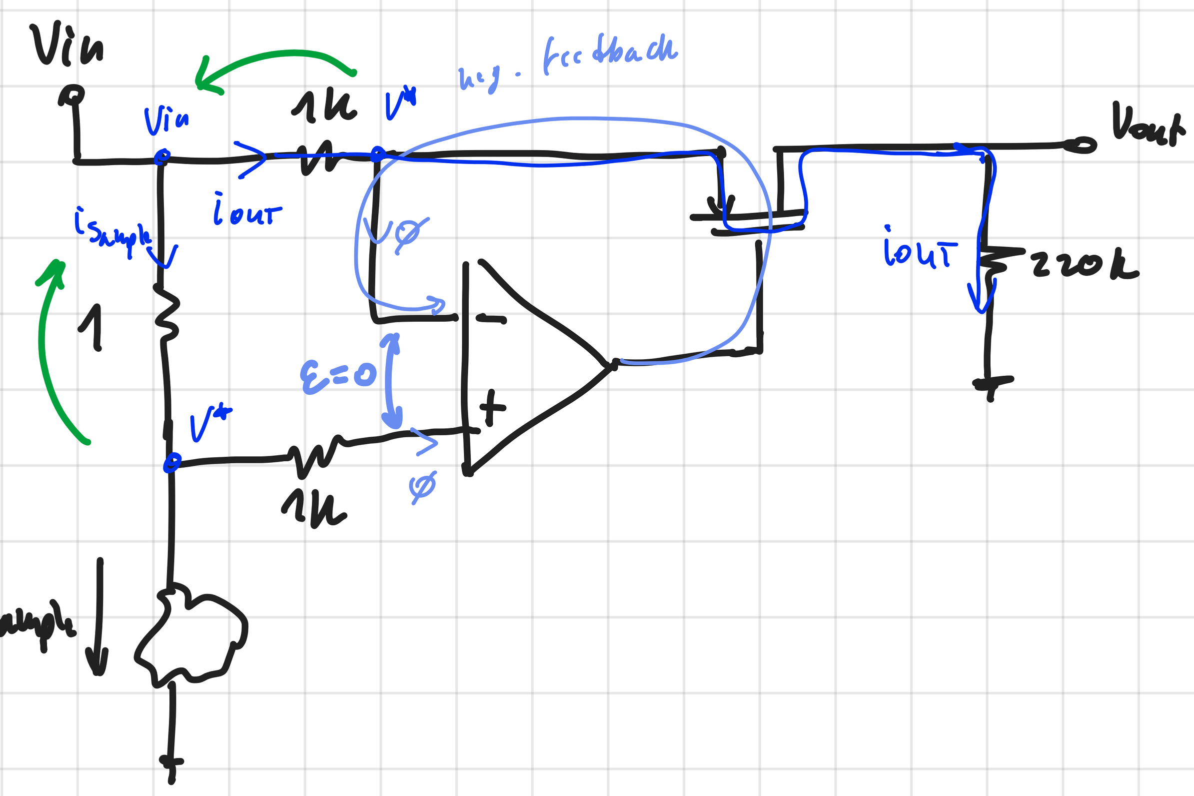


→ if $V_{in} > V_Z = 5.1V$ ⟷ guarantee a 5.1 P.S. to the OpAmp

this capacitor (connected bw the P.S.)
↳ so it's needed for stabilization or noise/dist. reduction

↳ If we remove the zener diode, the capacitor and the resistor





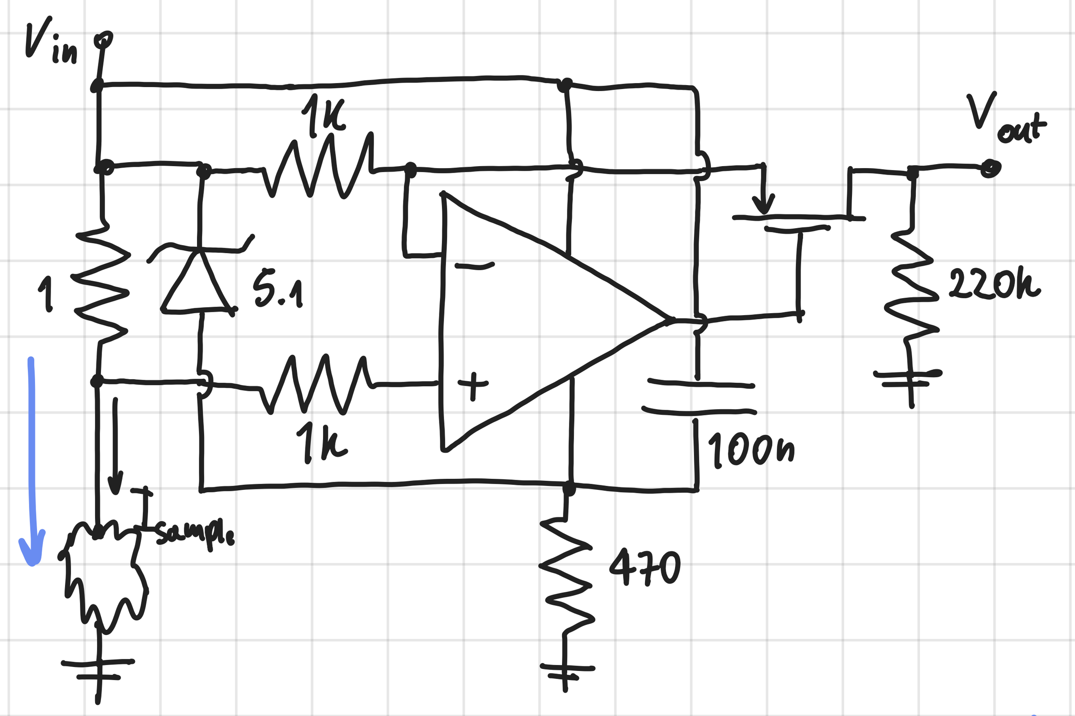
↳ Compute the ideal Gain ($\varepsilon = 0$):

↳ $i_{sample} \cdot 1\Omega = i_{out} \cdot 1k$

$$V_{out} = 220k \cdot i_{out} = 220k \frac{1\Omega}{1k} i_{sample}$$

I to V converter → ↳ $\frac{V_{out}}{i_{sample}} = 220 \frac{mV}{mA}$

b) Up to now the circuit was a current reader

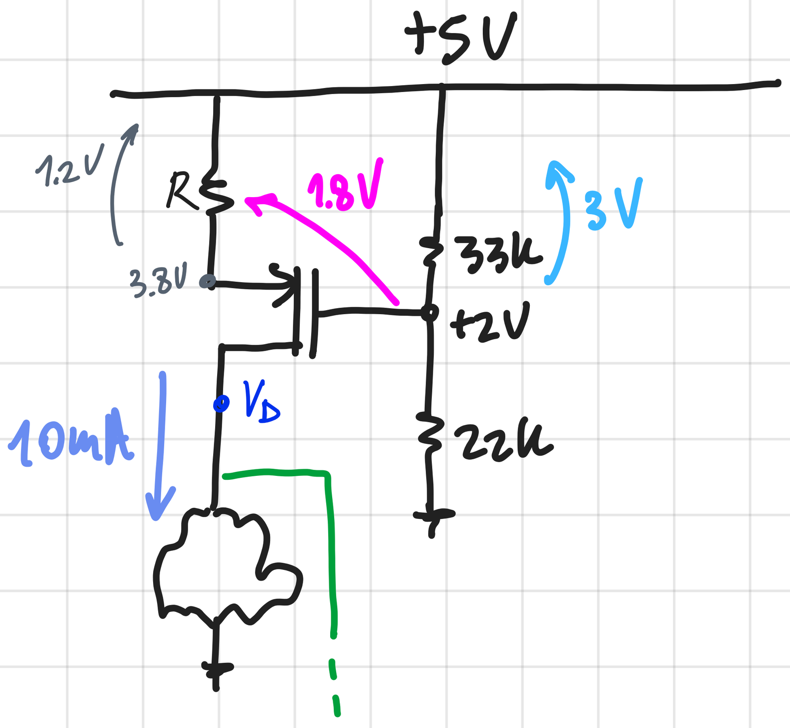


the current flows through the sample and provides a signal which is "proportional" to the current

↳ Now the signal does not vary anymore 'cause we're forcing a constant current i_{sample} through the sample

↳ $i_{sample} = 10\,mA$

e.g. stage design:



easy current generator

$V_t = 0.8\,V$

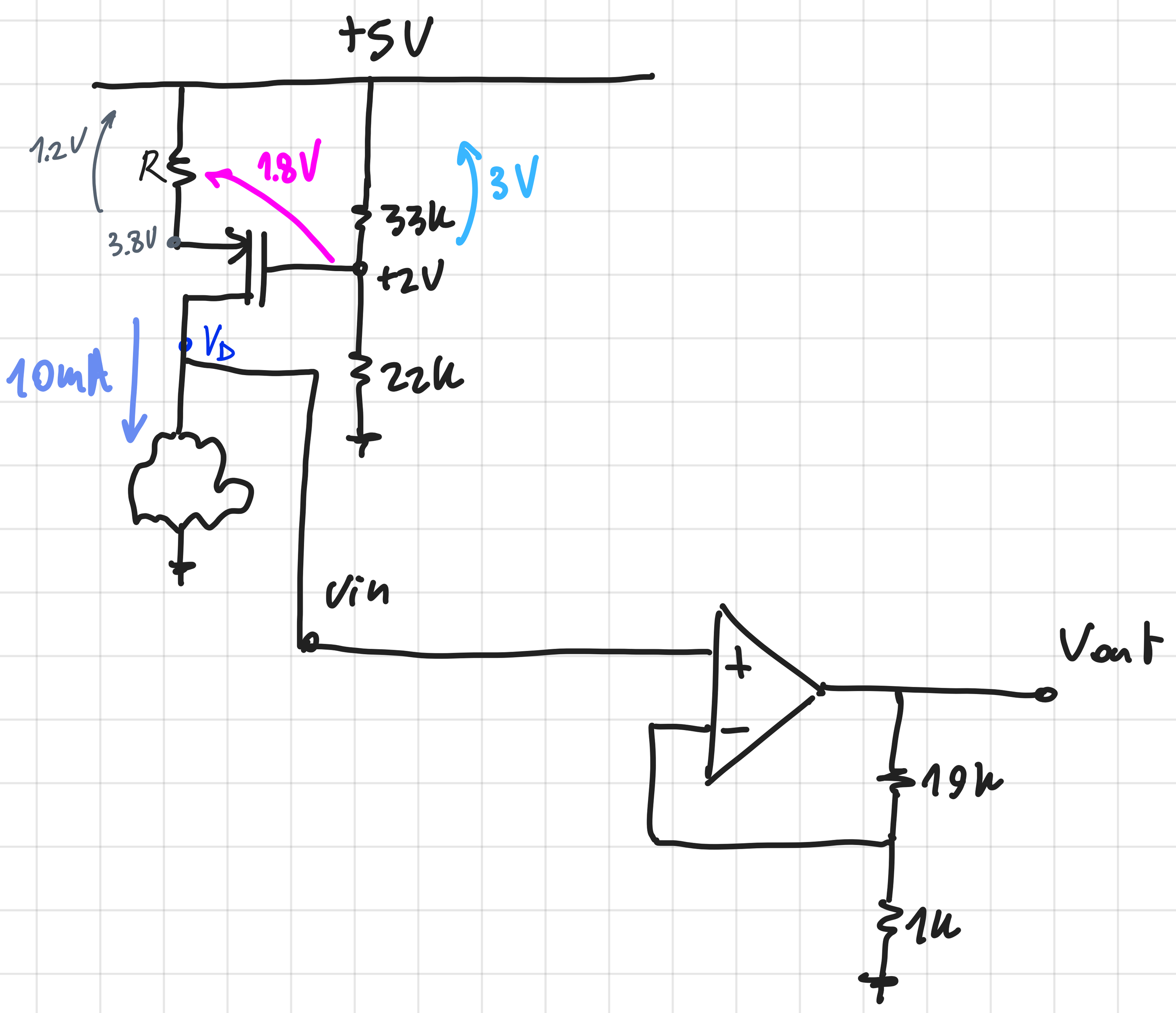
$k = 10\,\frac{mA}{V^2}$

$$\hookrightarrow V_{GS} = V_t + \sqrt{\frac{i_{sample}}{k}} = 0.8 + \sqrt{\frac{10\,mA}{10\,\frac{mA}{V^2}}} = 1.8\,V$$

$$\hookrightarrow \underset{V_S - V_D}{V_{DS}} \geq \underbrace{V_{OD}}_{\text{overdrive}} = V_{GS} - V_t = 1\,V$$

$\hookrightarrow V_D \leq 3.8\,V - 1\,V = 2.8\,V$

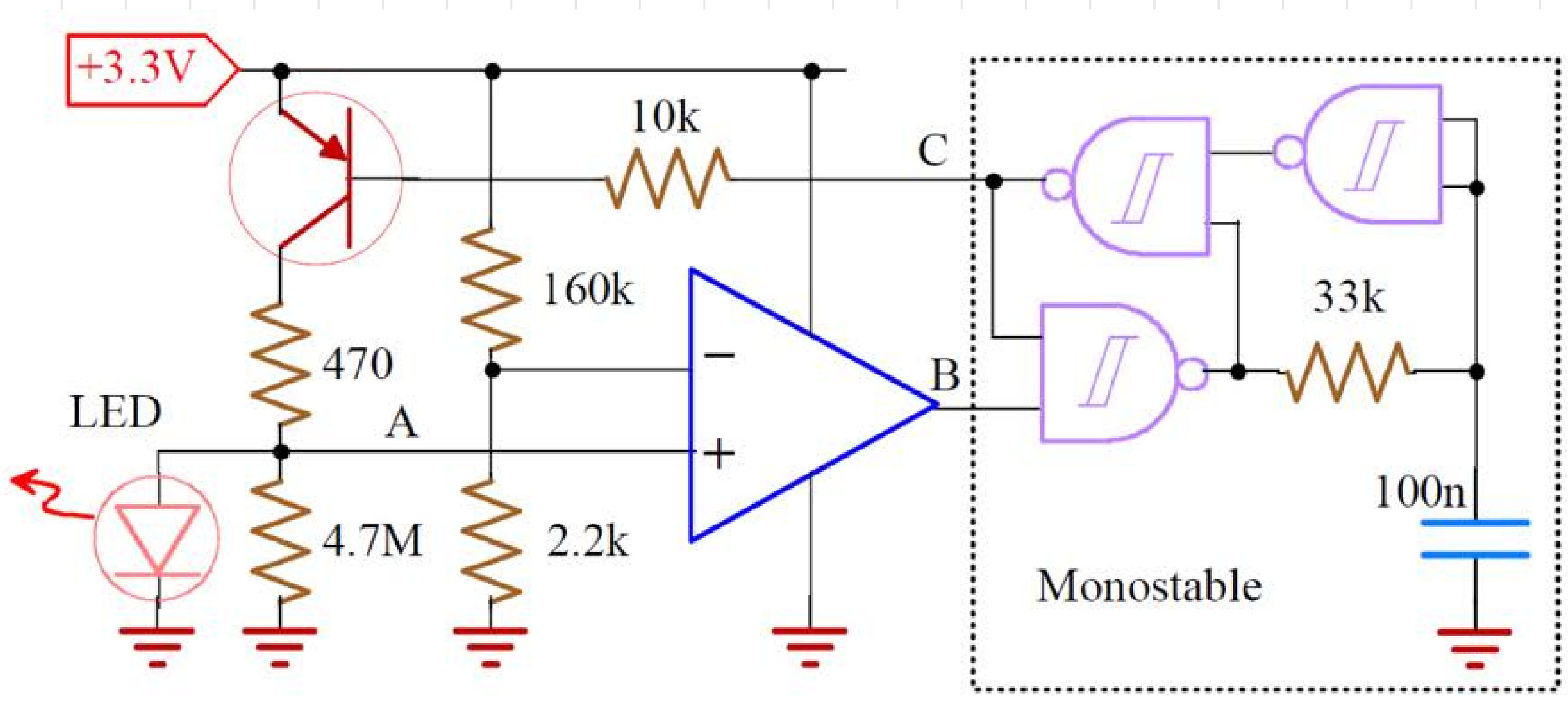
Then to measure it with a gain of 20 we should add an amplifier:

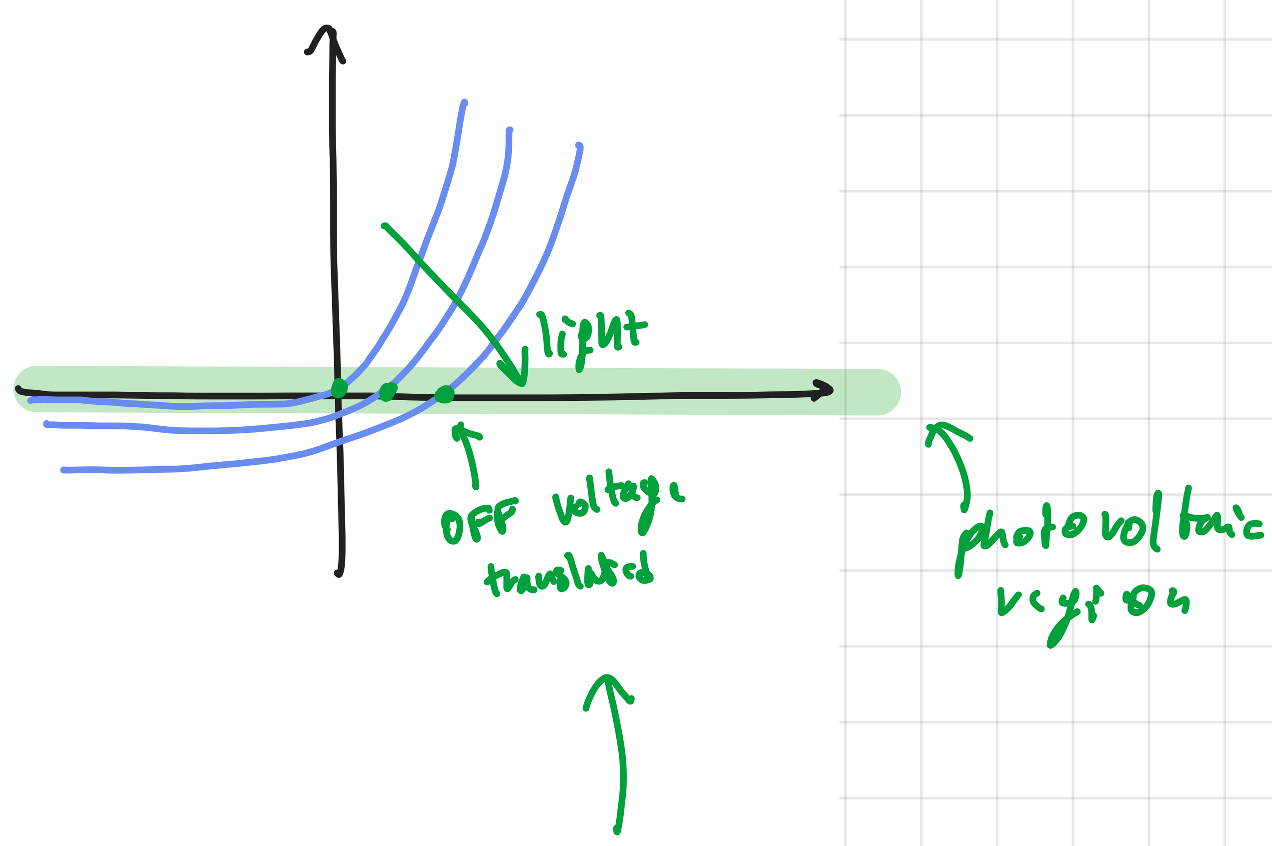


$$\rightarrow G = \frac{V_{out}}{V_{in}} = 1 + \frac{19k}{1k} = 20 \checkmark$$

⑦ (OF Es.16 slides → to solve at home)

⑧

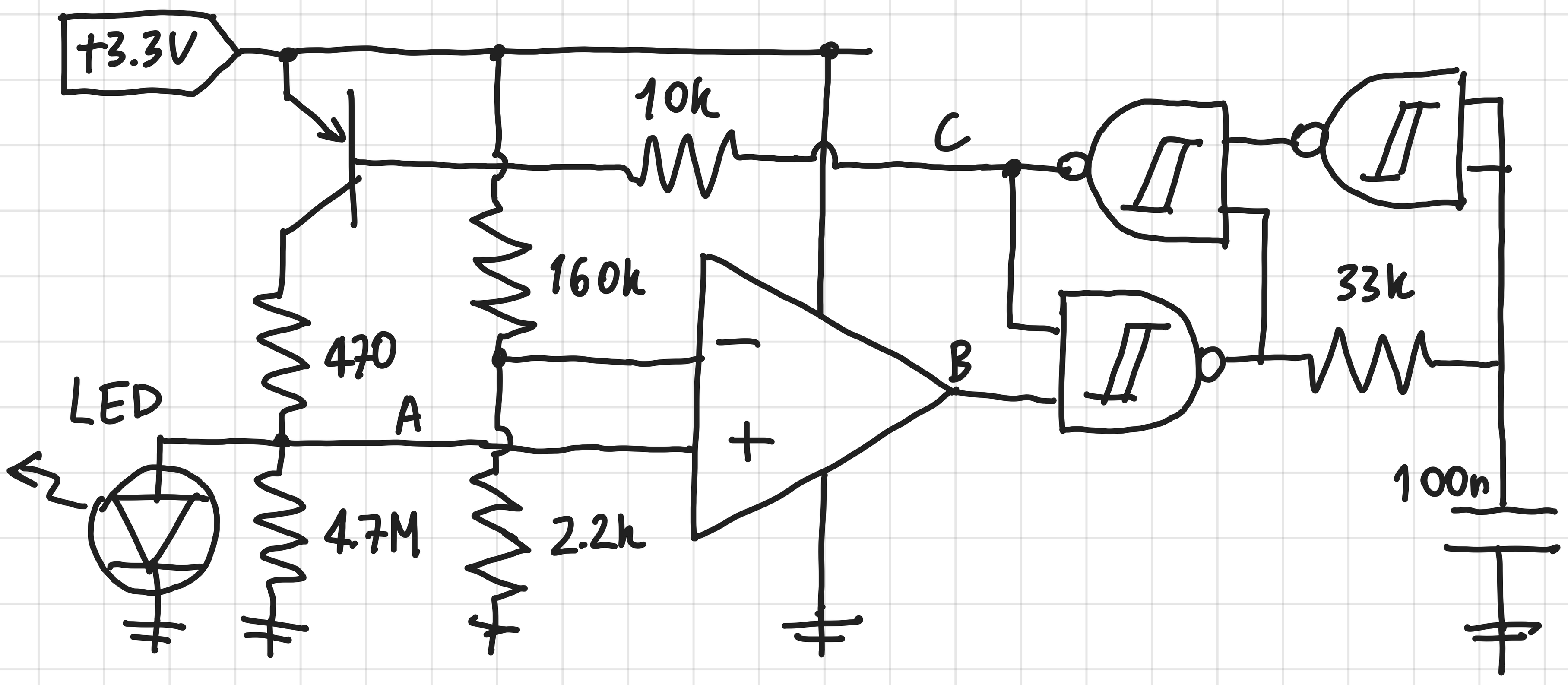




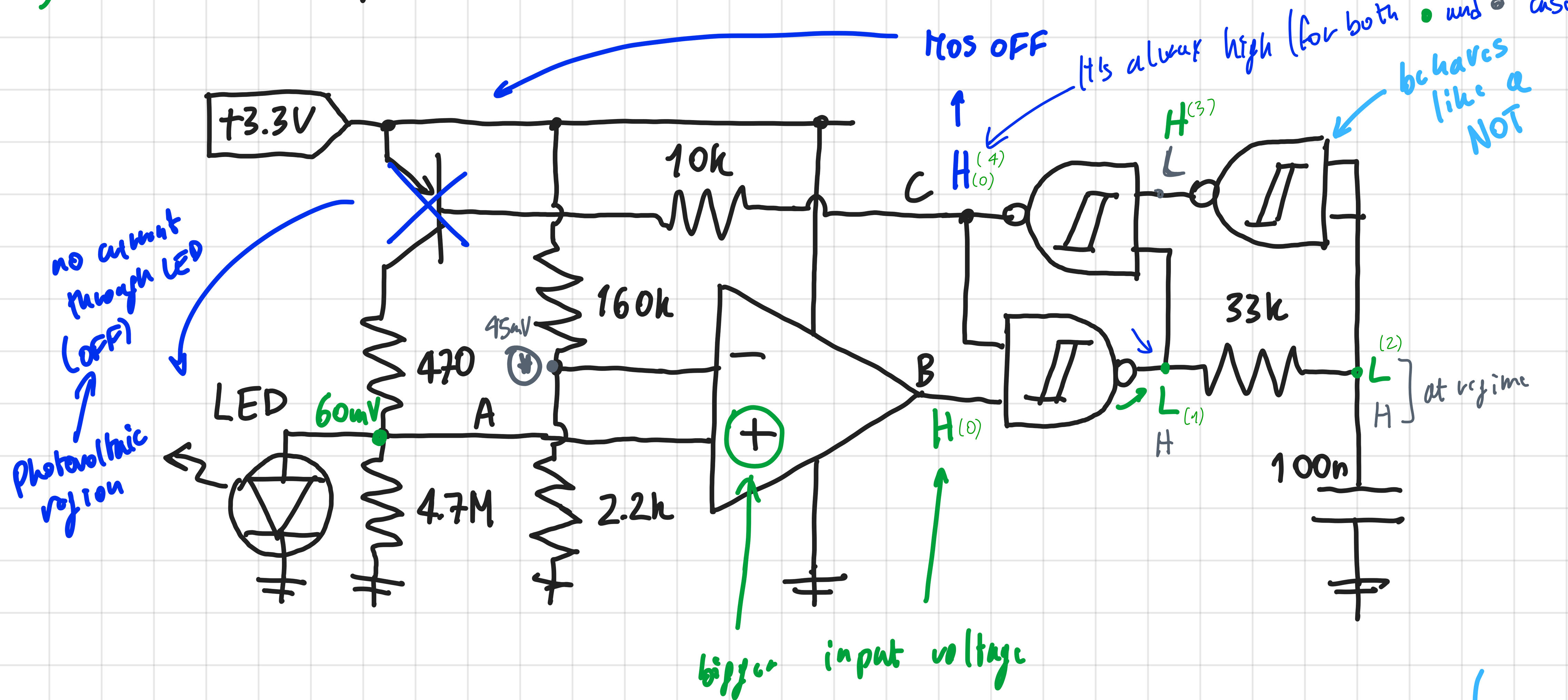
The circuit switches on/off the LED if there is dark/light, without using any other photodiode, but exploiting the photovoltaic effect of the LED itself (with no voltage applied and in light condition it produces 60÷90mV).

a) Plot all voltage waveforms **with light**, explaining circuit behaviour.

b) Plot all voltage waveforms **with no light**, explaining circuit behaviour.

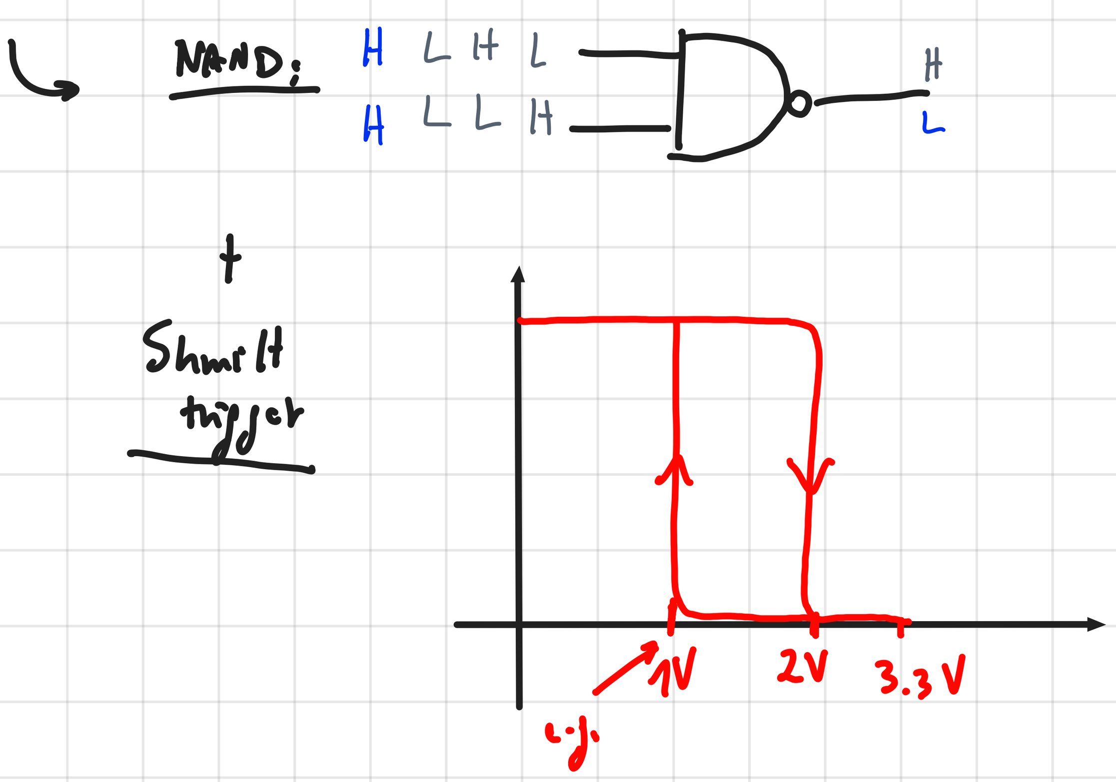


a) If there's light on the LED even if is OFF it's in the photovoltaic region → it has voltage ≠ 0 across it



$$3.3\,V \cdot \frac{2.2k}{2.2k + 160k} = 45\,mV$$

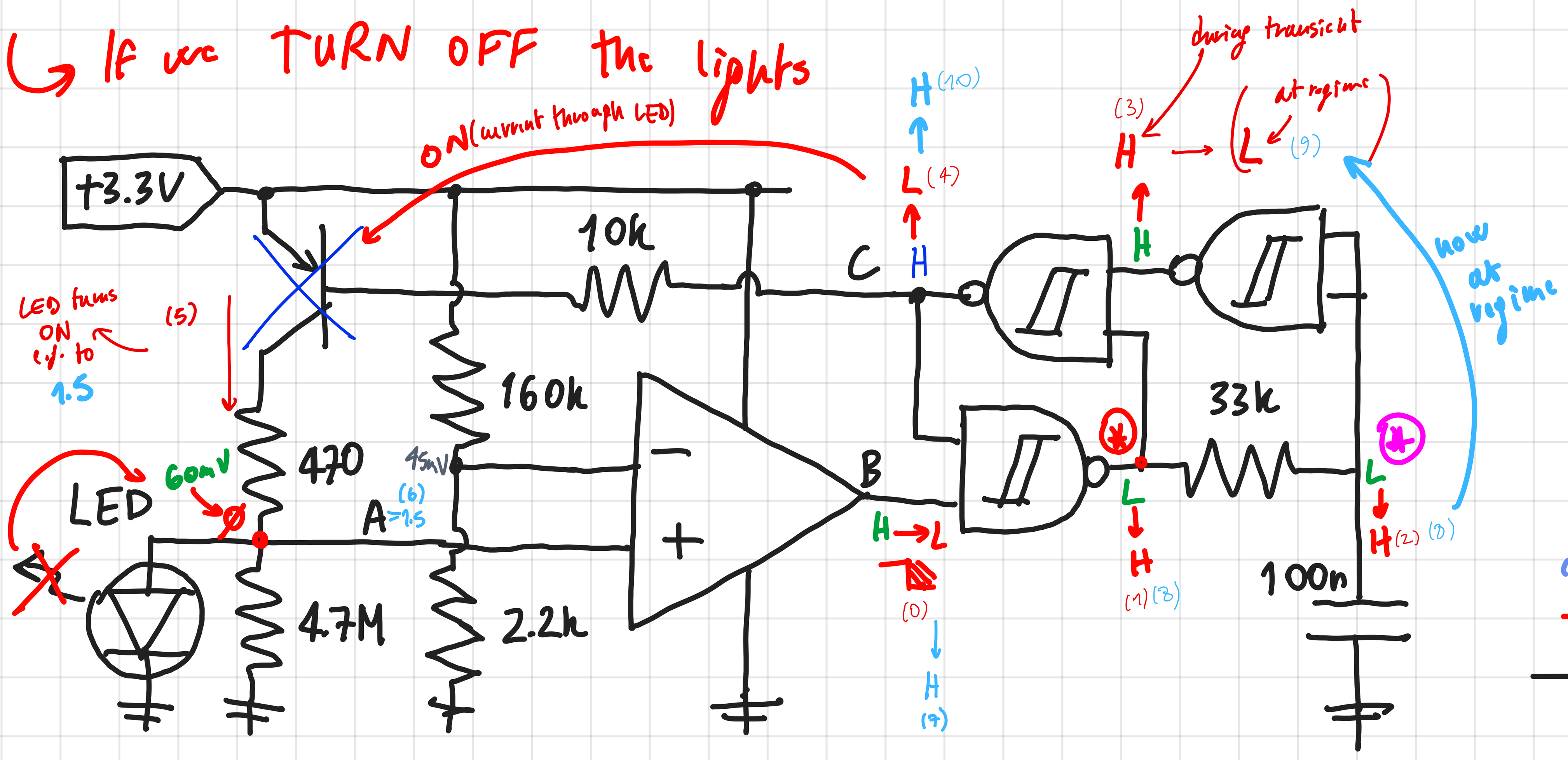
(Remember = Shmitt trigger) NAND gate

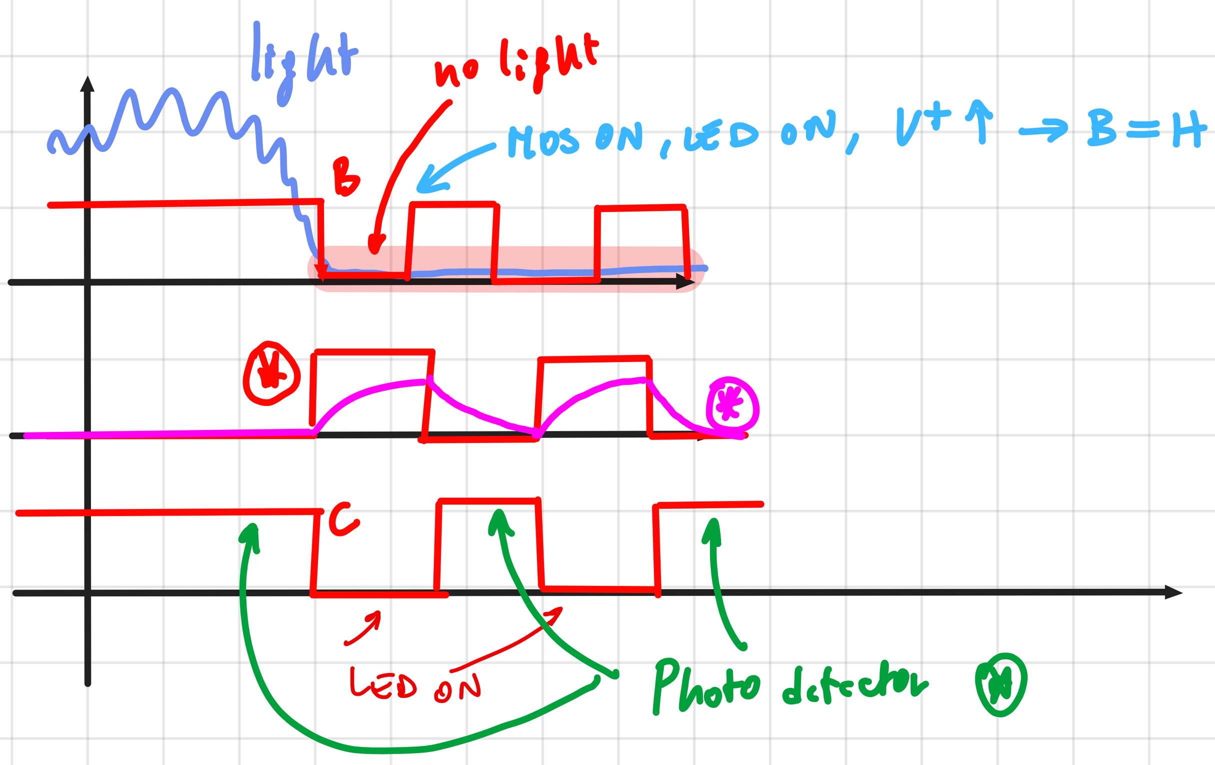


↳ A shmitt trigger is needed because we have an analog voltage in order to be uncertain (due to noise on signal) when commuting we should use Shmitt trigger digital gates

b)

↳ If we TURN OFF the lights





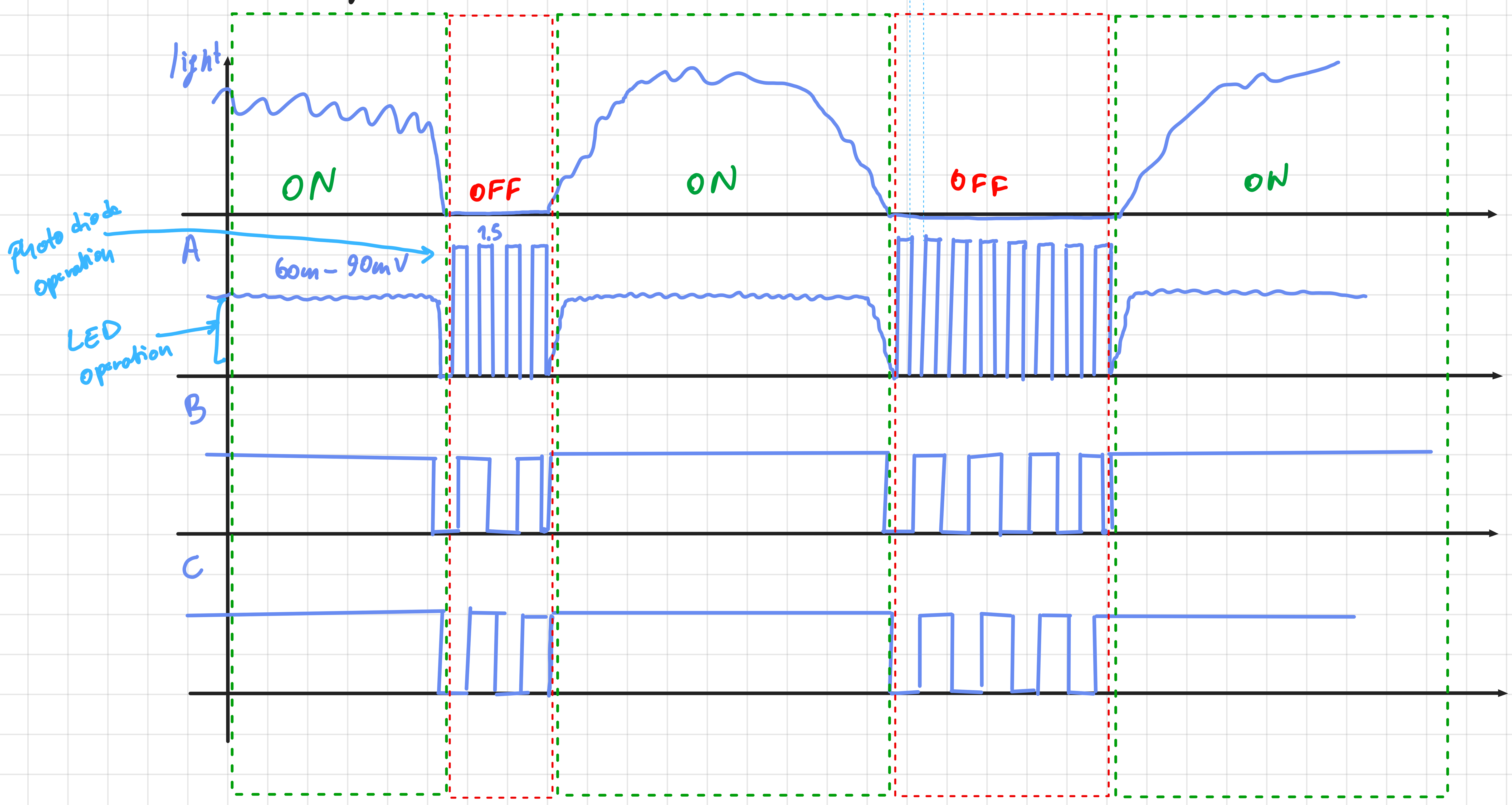
↳ then if there's the light off again the circuit continues to commute

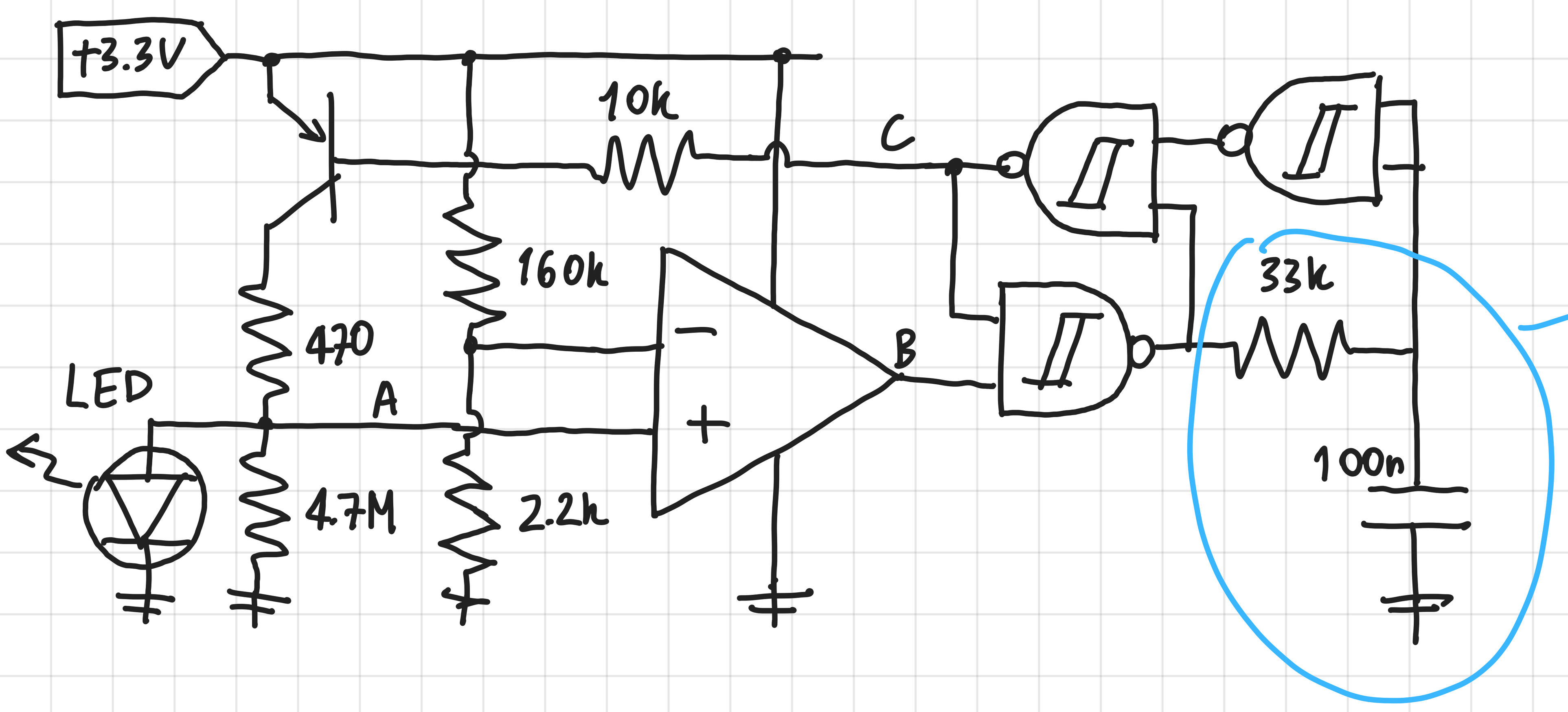
- If there's always light → C ≡ H (because B ≡ H)
- if there's no light → C ≢ L for B ≡ L (LED on)

$\tau \longrightarrow T = 2\tau \longrightarrow T = 6.6\,ms$

$f_{osc} = \frac{1}{T} = 151\,Hz$

↳ So summarizing:

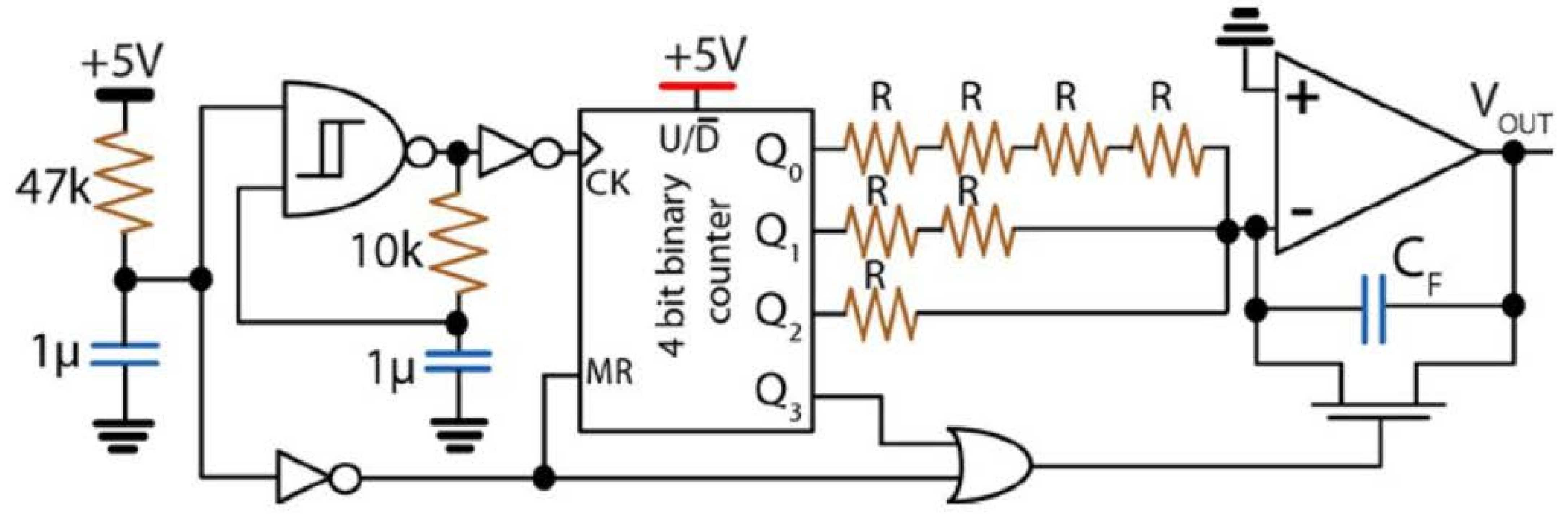




$\tau = 33k \cdot 100n = 3.3\,ms$

(Es 11 on slide ES16)

9

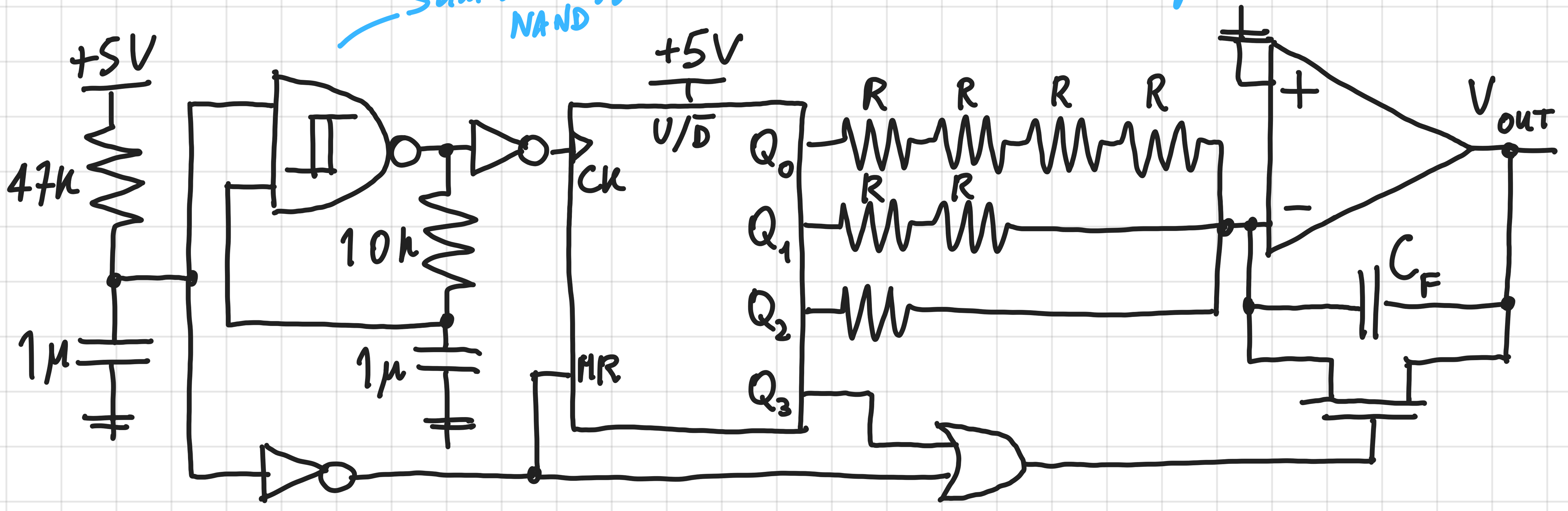


R=100kΩ, C_F=10μF. The digital counter provides +5V high levels and Q_0 is the least significant bit.

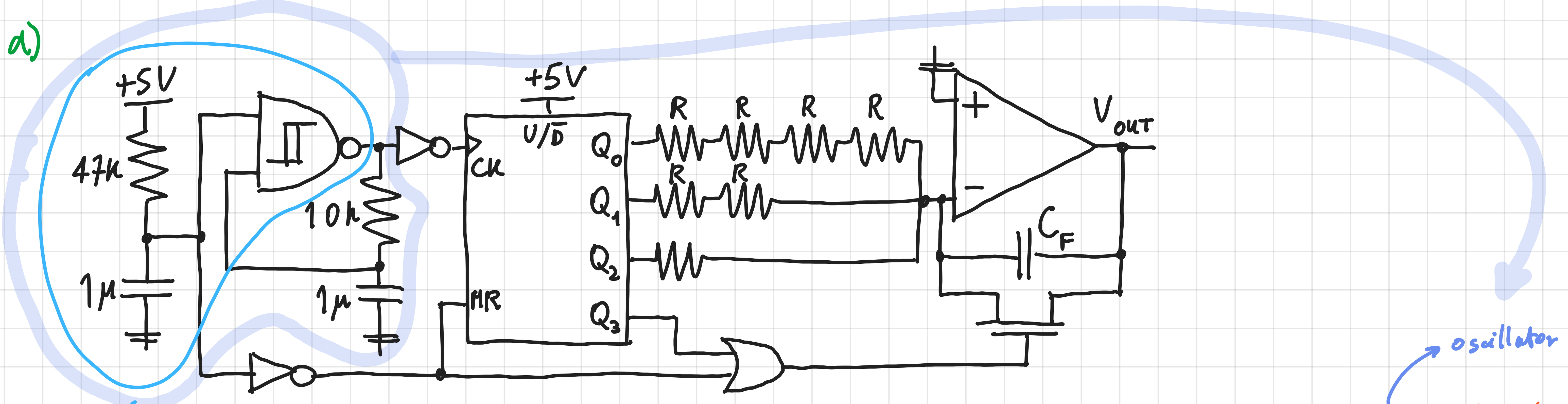
a) Plot the V_{OUT} quoted waveform during the first 3 clock periods (10ms period).

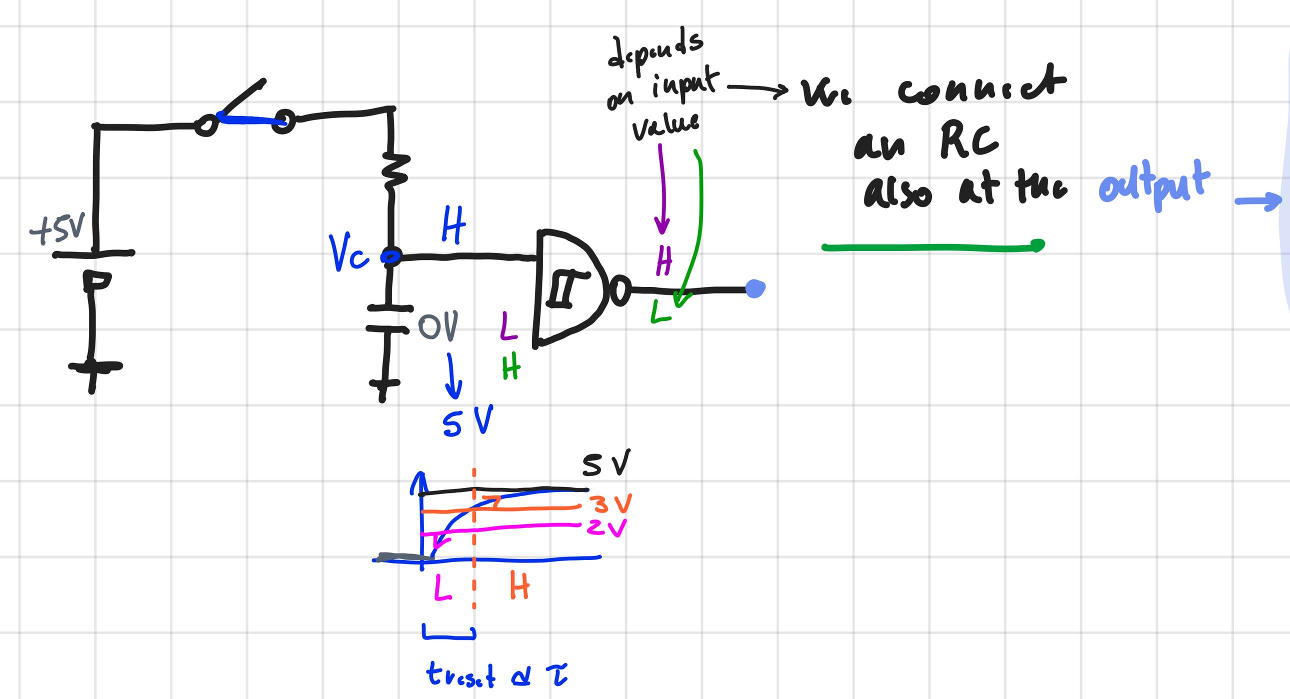
b) Plot CK and V_{OUT} waveforms during the first 200ms.

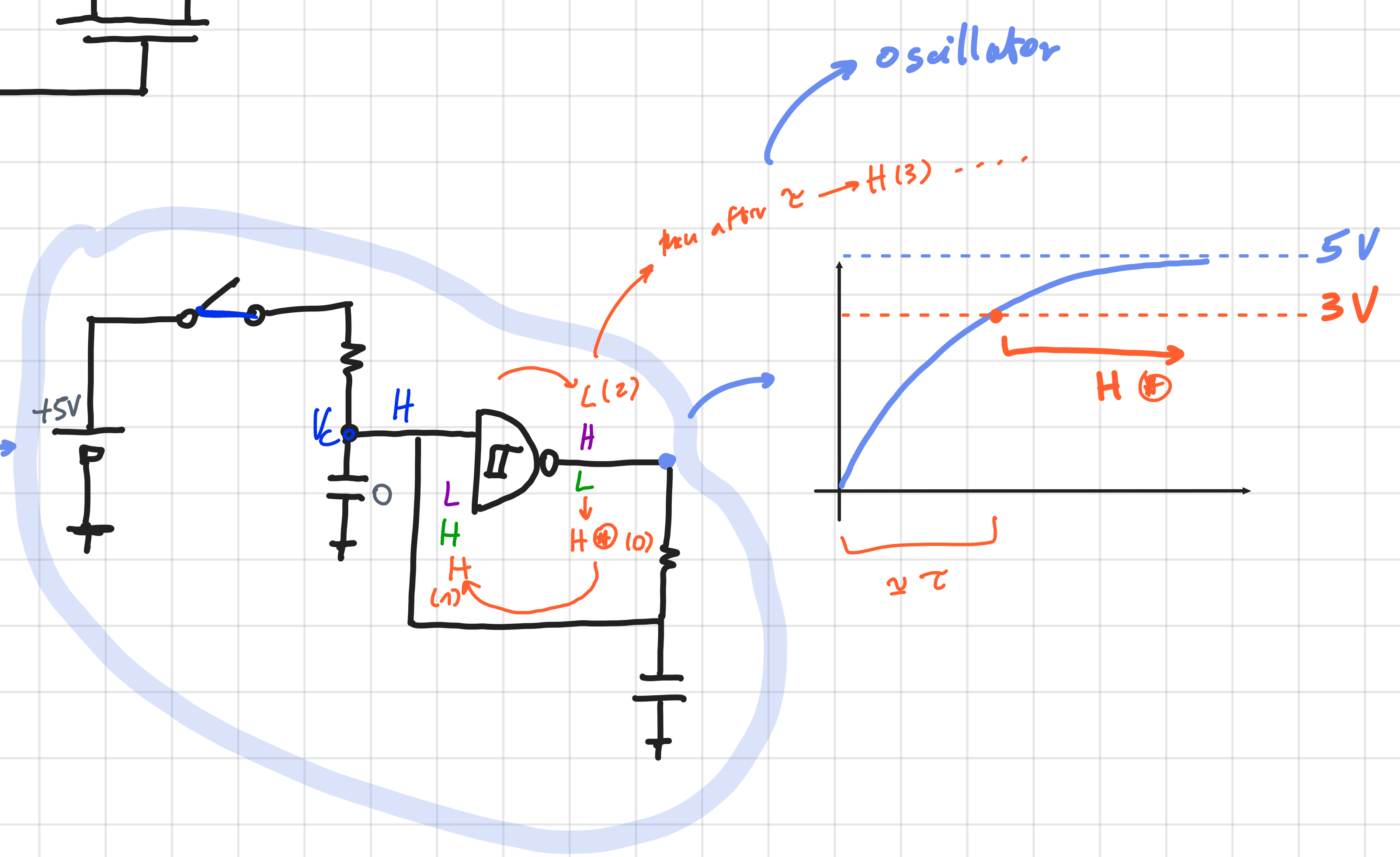
Schmitt trigger NAND ('cause we have an analog signal that drives it)



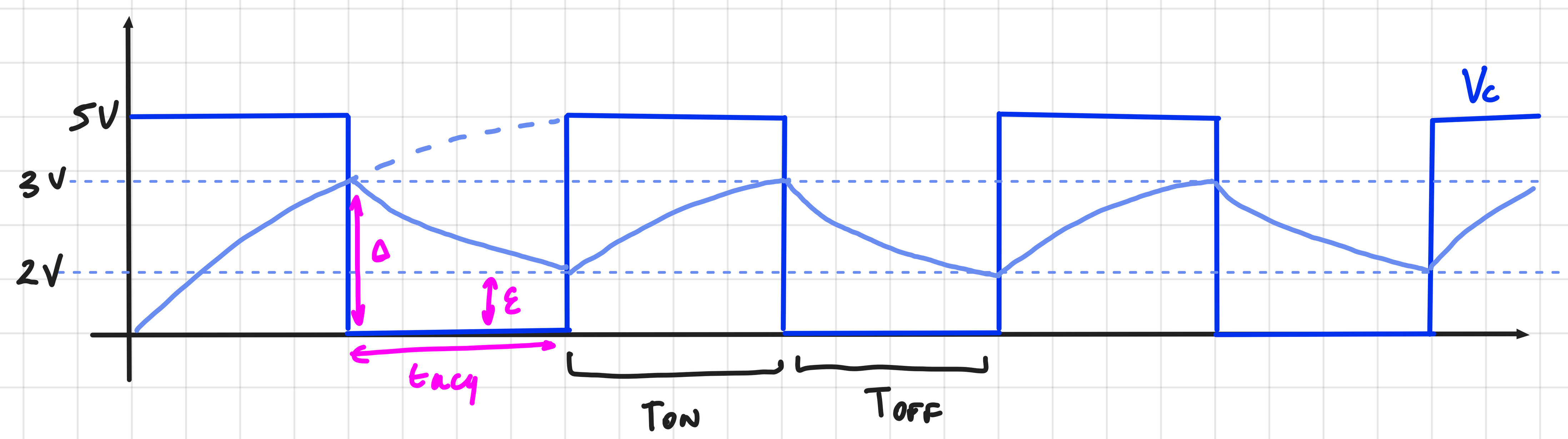
a)







So for the oscillator:

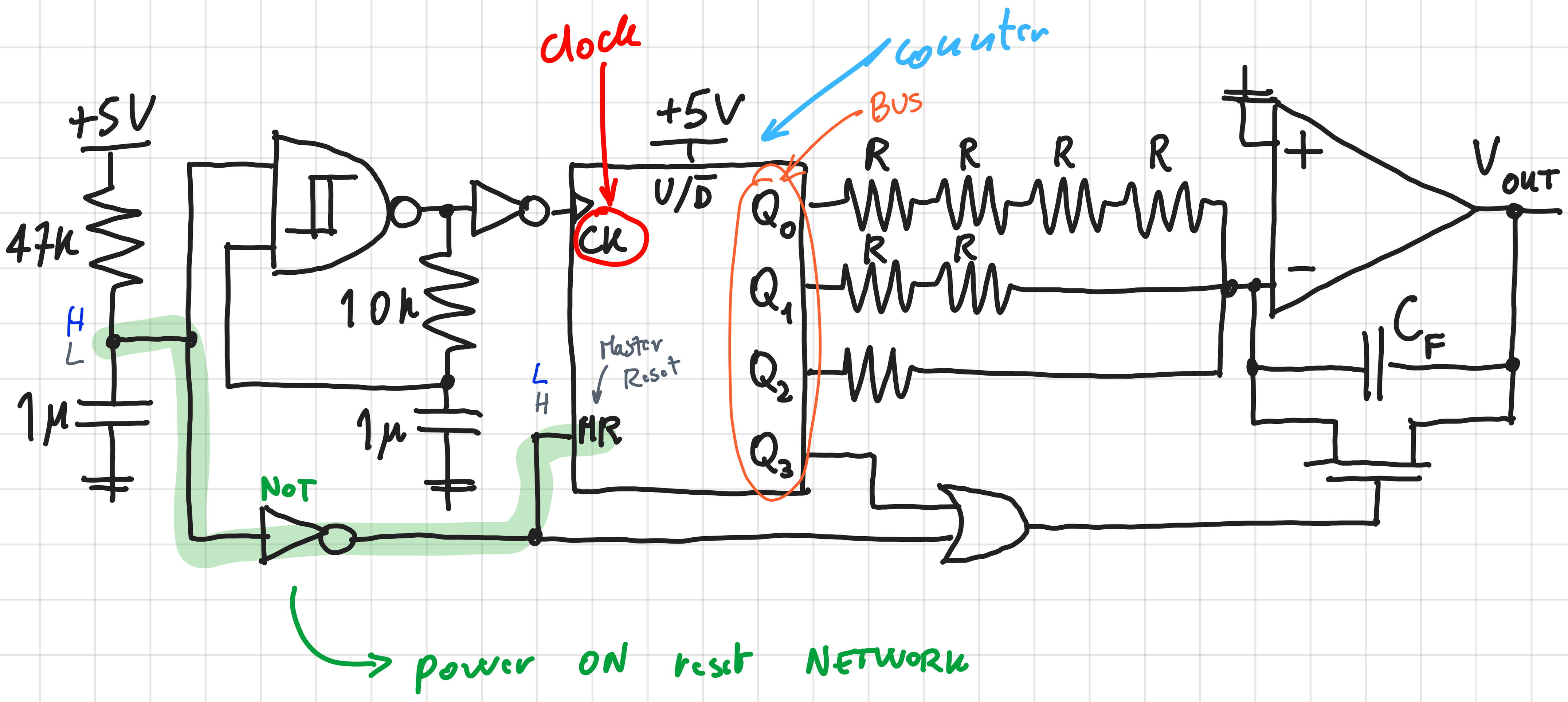


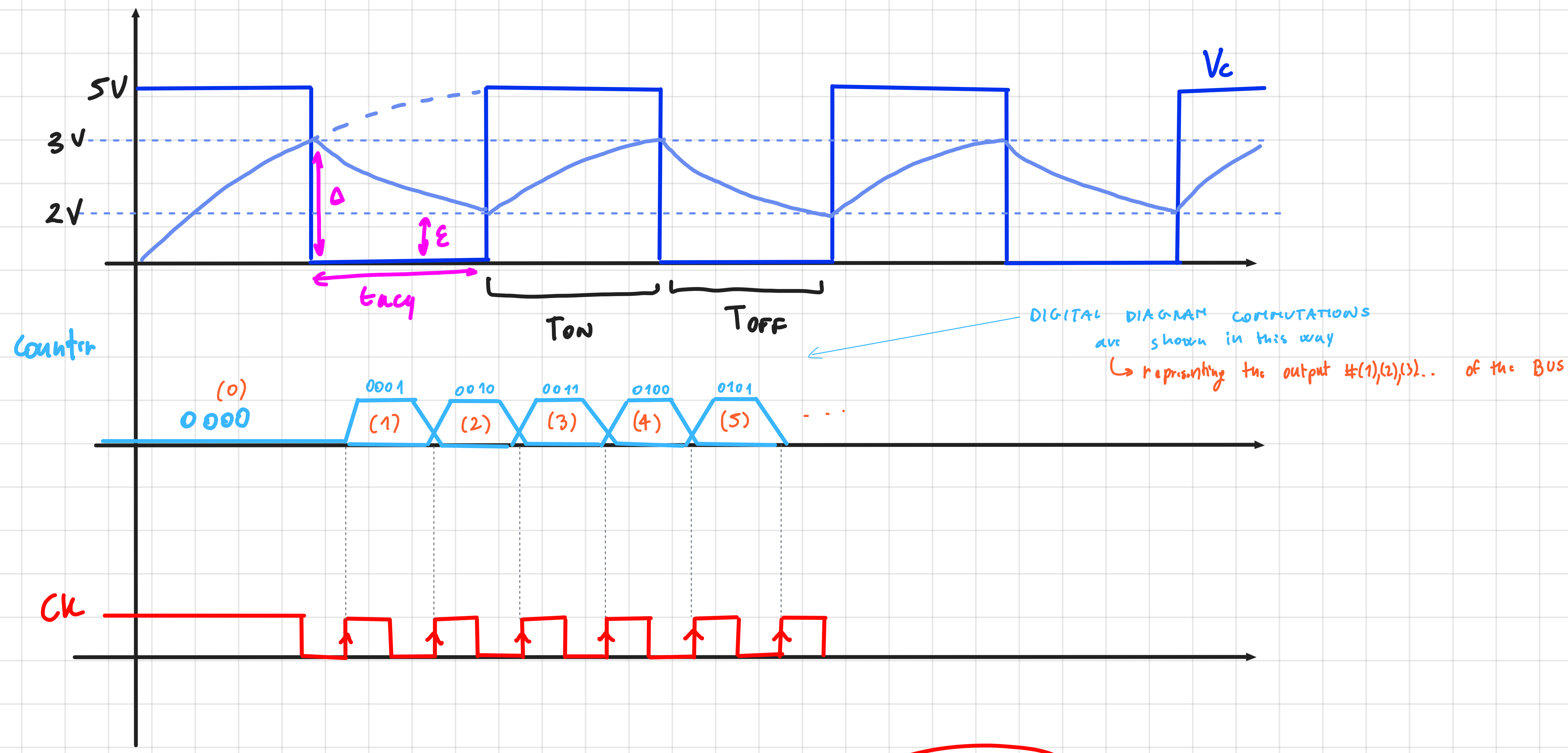
Δ = 3V

ε = 2V $\quad \longrightarrow T_{OFF} = t_{eq} = \tau \ln \frac{\Delta}{\varepsilon} = \tau \ln 1.5 = \ln \cdot 40\% \cong T_{ON}$

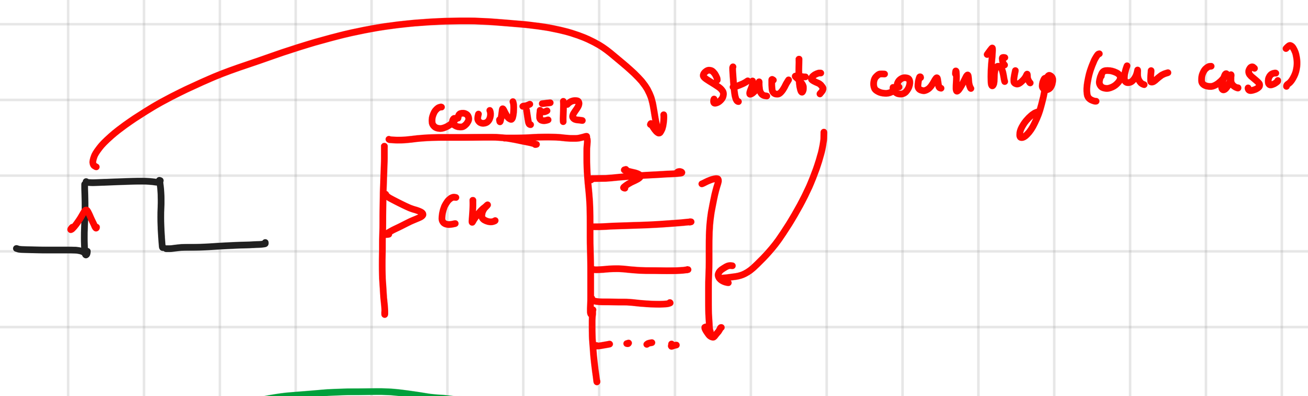
$\hookrightarrow T = T_{ON} + T_{OFF} = 2 \cdot 40\% \cdot \tau \cong \tau \longrightarrow$ for $\tau = 10ms \longrightarrow f_{OSC} = \frac{1}{T} \cong 100Hz$

↳ Now consider

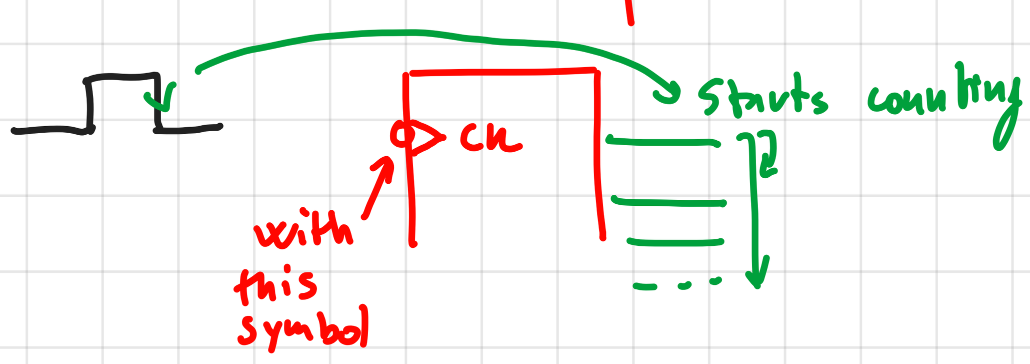




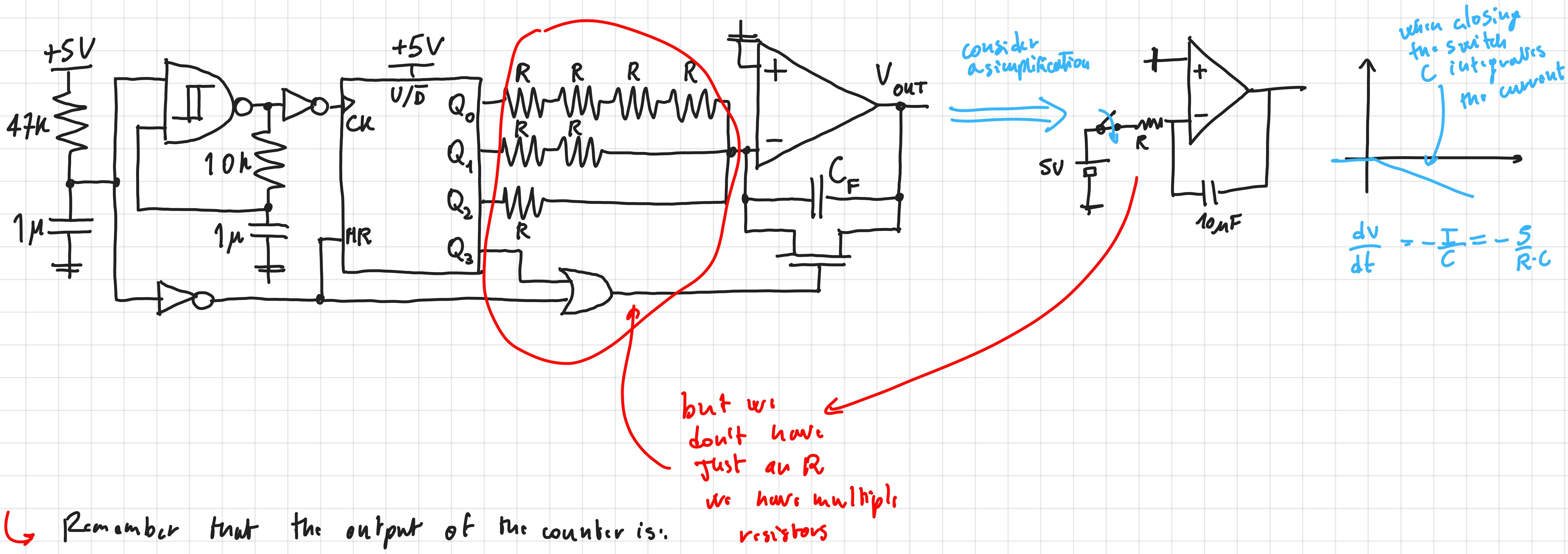
Note: • Rising edge transition of the ck



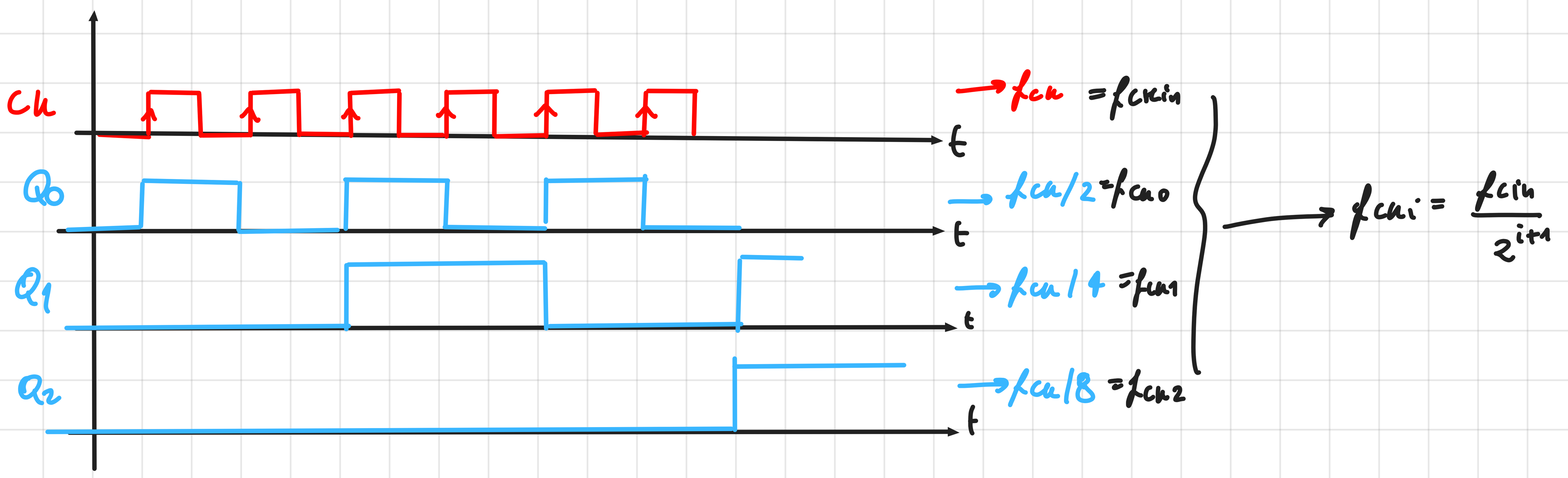
• Falling edge transition of the ck



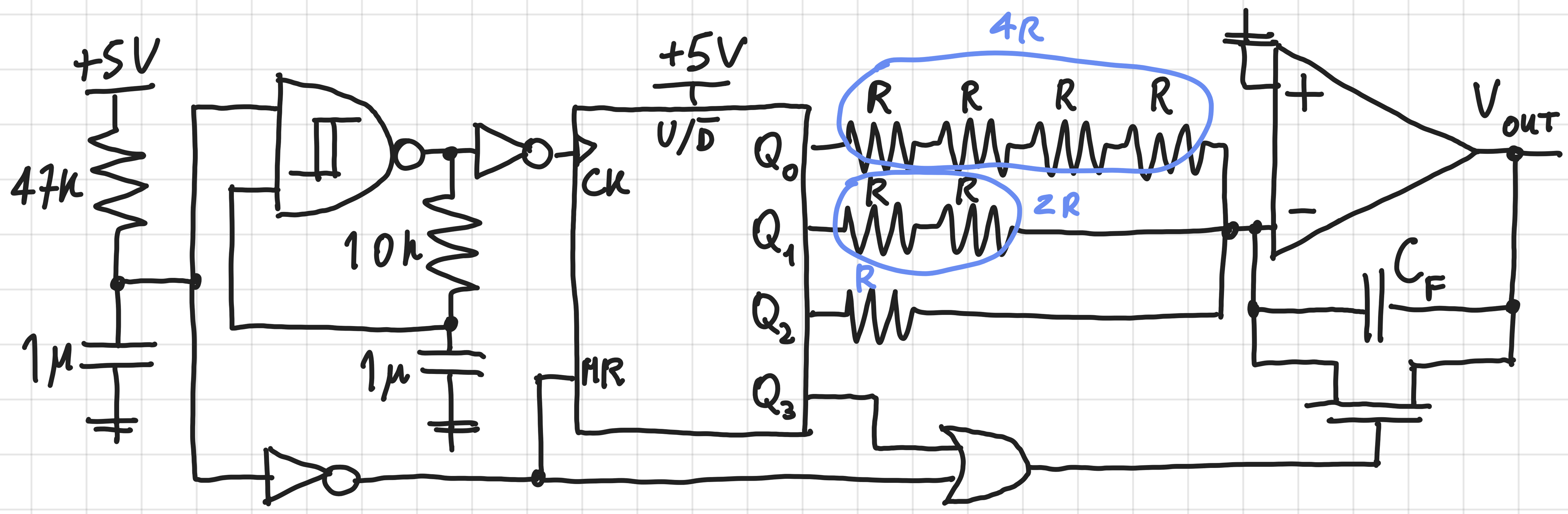
↳ If we keep analyzing the circuit:



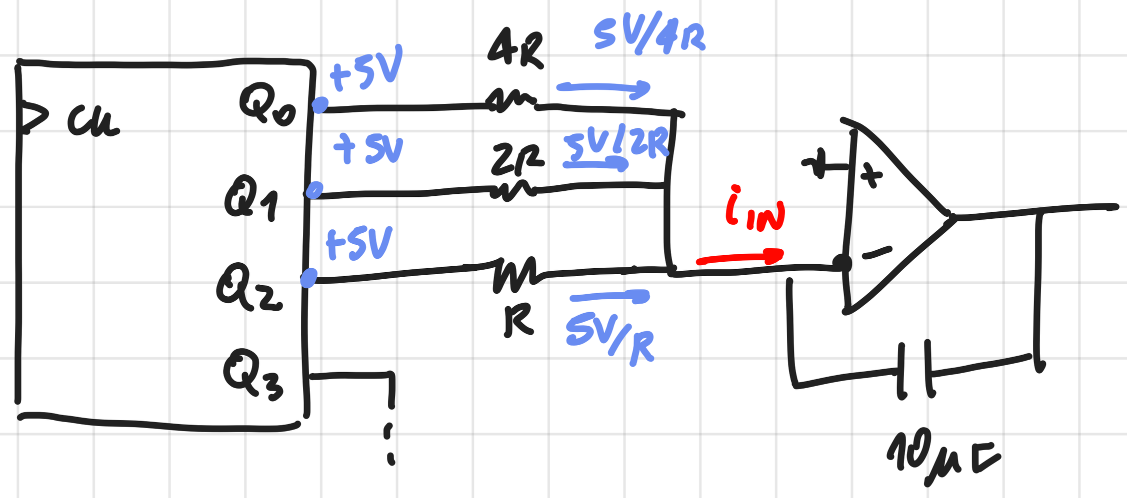
↳ Remember that the output of the counter is:



↳ So in the circuit, each Q_i contributes with Rs in a different way:



↳ So



→ So generically:

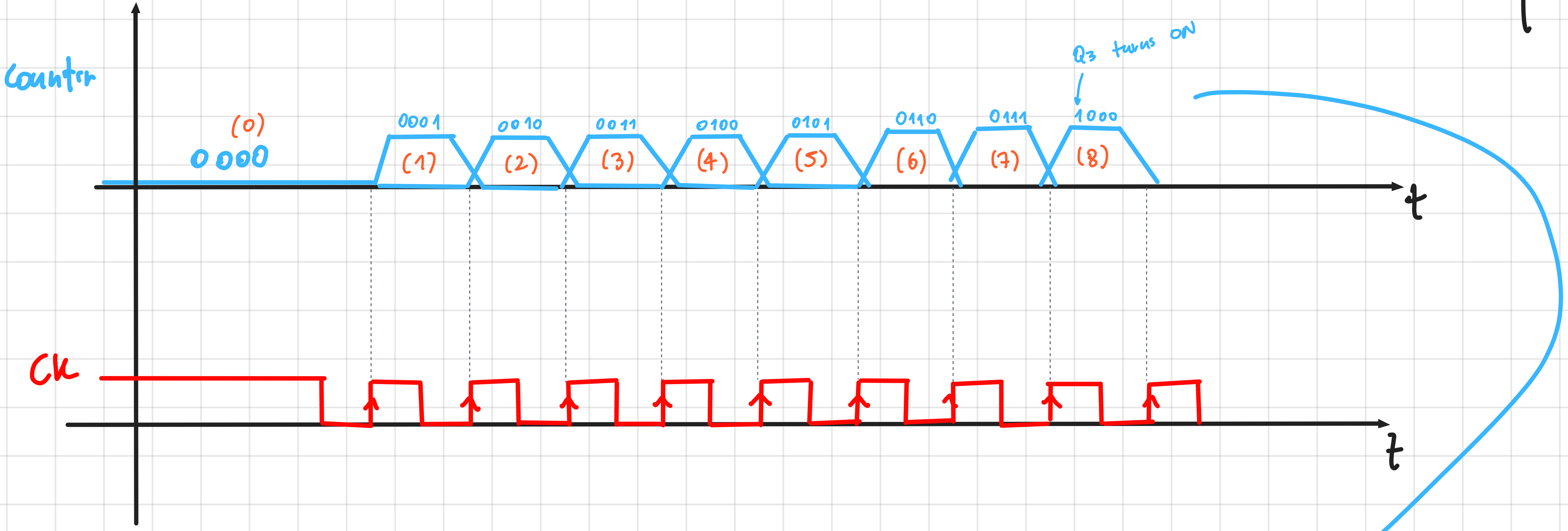
$$i_{IN} = Q_0 \cdot \frac{5}{4R} + Q_1 \cdot \frac{5}{2R} + Q_2 \frac{5}{R} = \frac{5}{R}\left[\frac{Q_0}{4} + \frac{Q_1}{2} + \frac{Q_2}{1}\right]$$

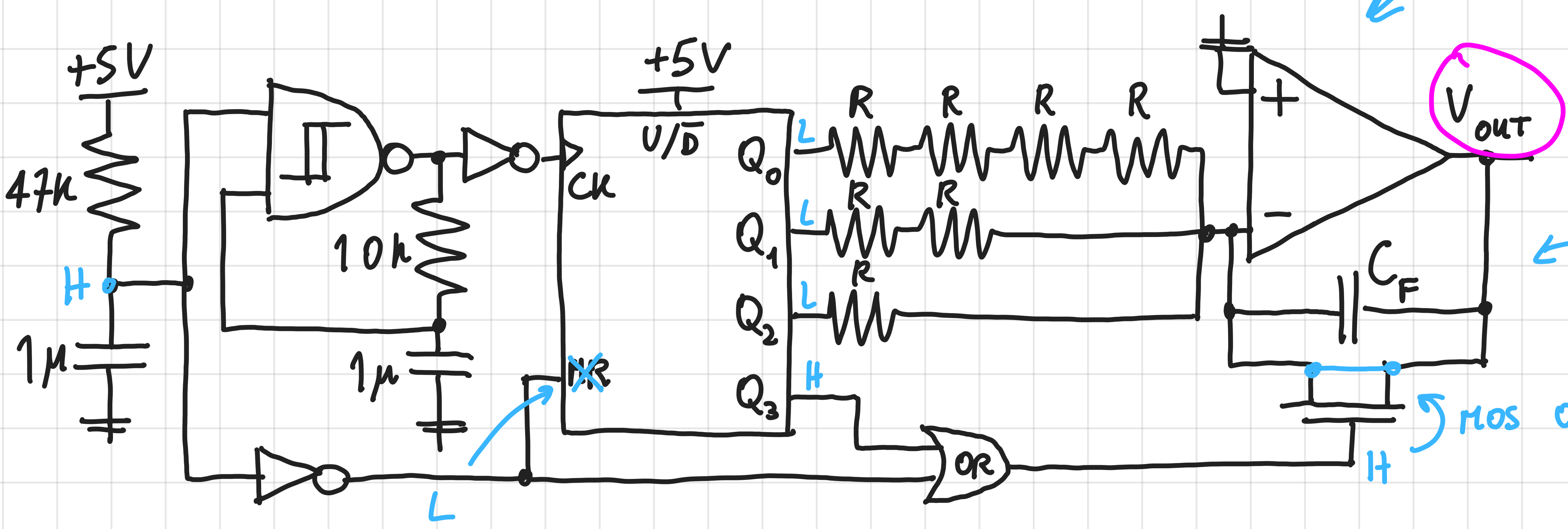
$$= \frac{5}{R} \cdot D_{out}$$

digital output of the counter

↳ So when the output (BUS) increments the current increments:

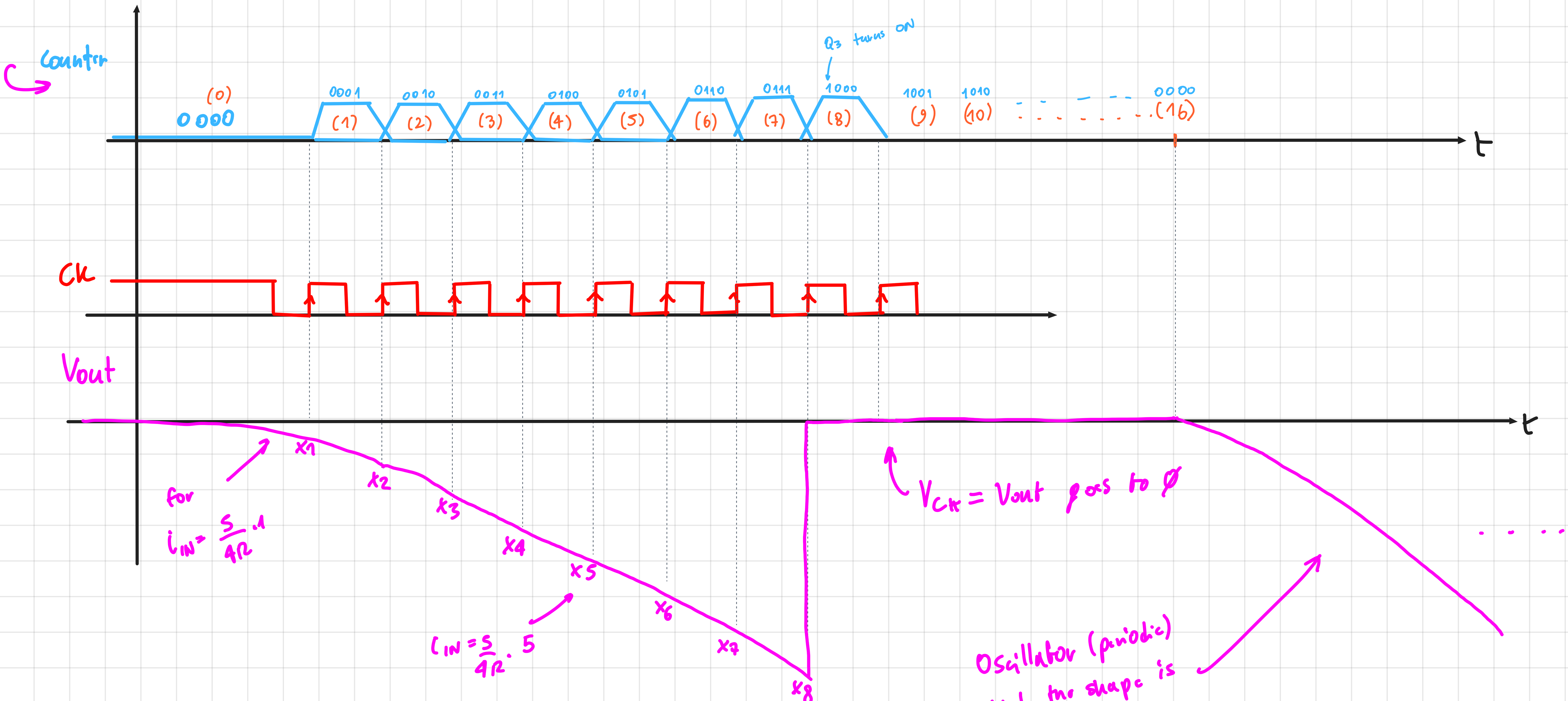
(Number format ex.
0 1 0 1
Q_3 Q_2 Q_1 Q_0)





the capacitor is quickly discharged to Ø

MOS ON → close switch



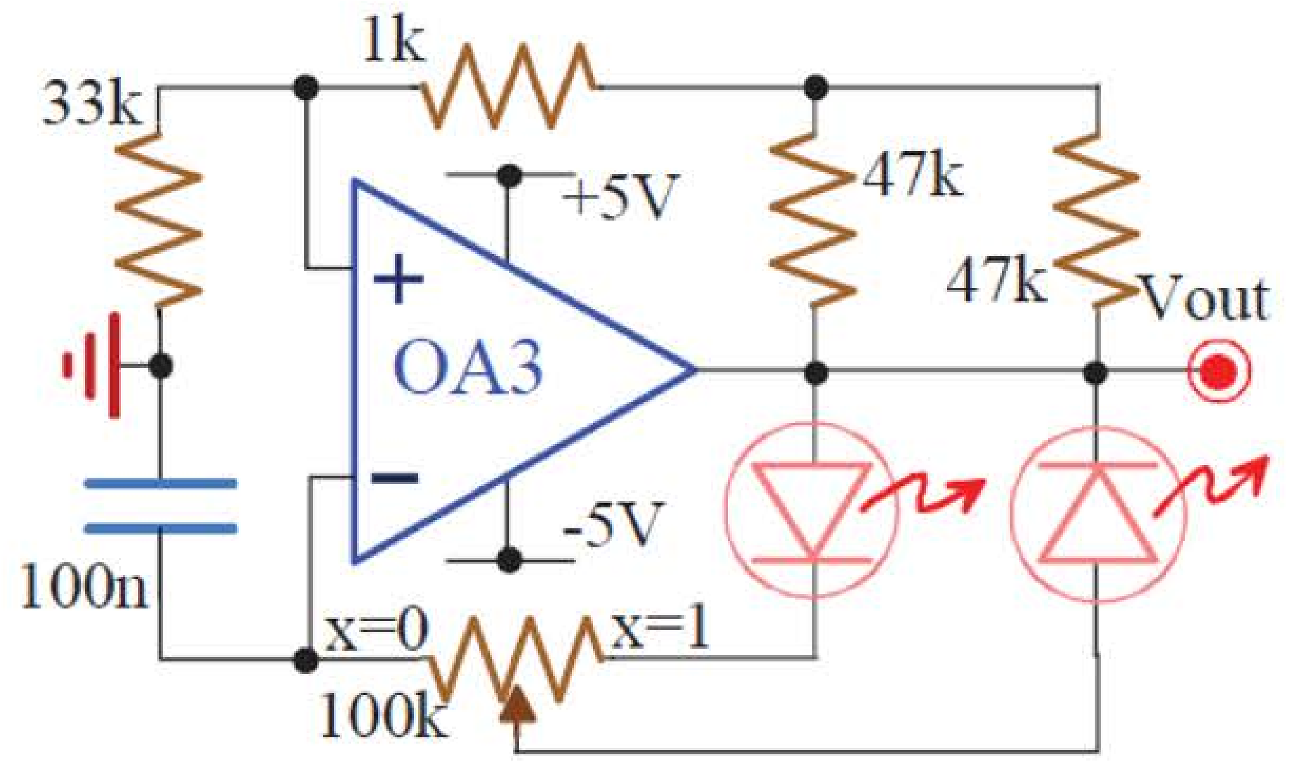
for $i_{IN} = \frac{5}{4R} \cdot 1$

$i_{IN} = \frac{5}{4R} \cdot 5$

$V_{CF} = V_{out}$ goes to Ø

Oscillator (periodic) and the shape is this kinda of paraboloid

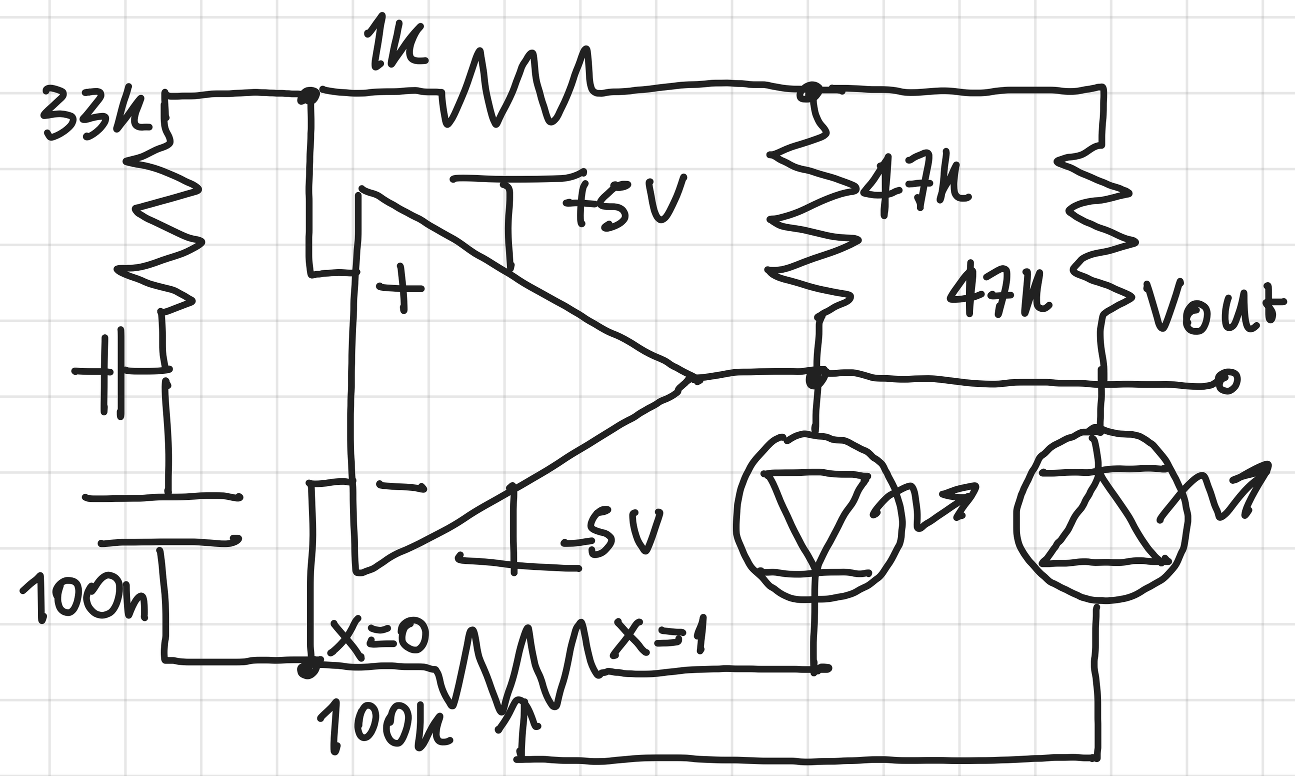
10 (Ex 13 – ES1'6)



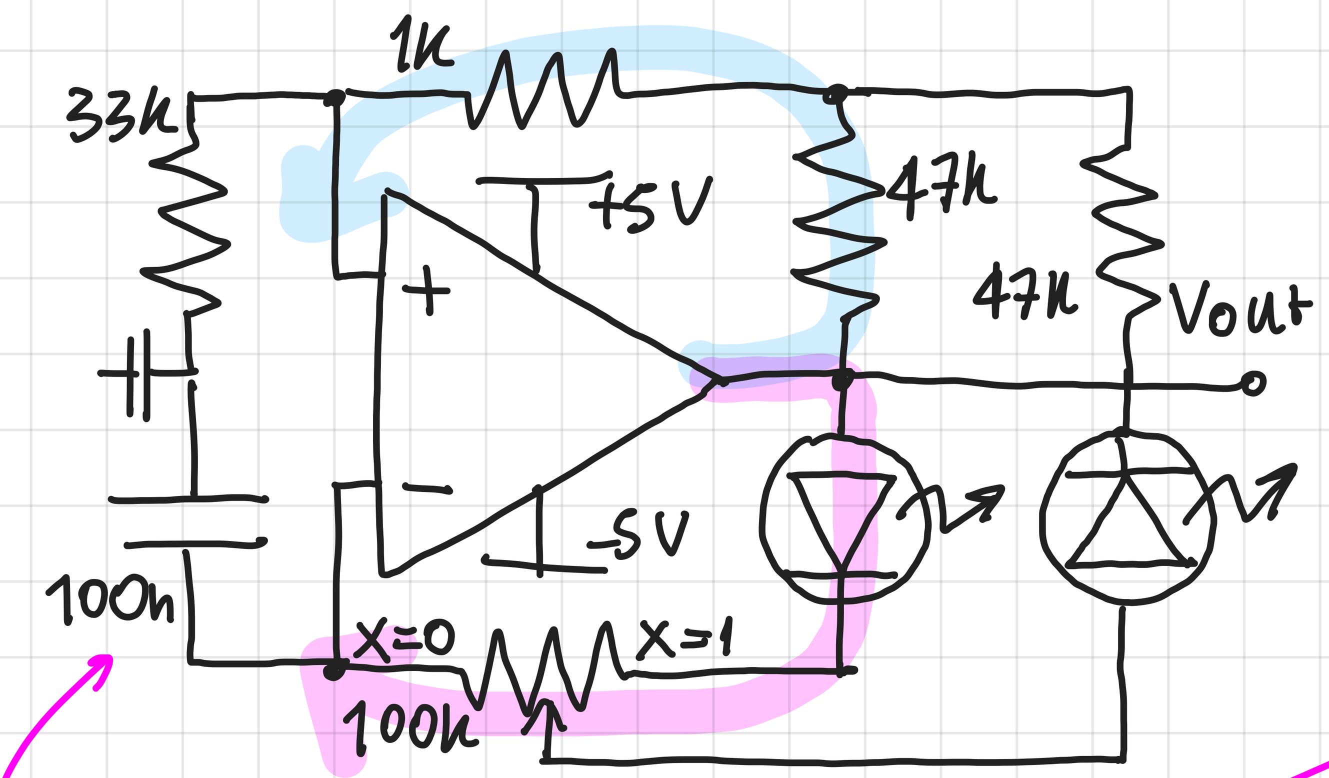
Employ 1.5V forward bias LEDs and a rail-to-rail OpAmp.

a) Study circuit operation when the pot is turned to 100% and draw the quoted output waveform.

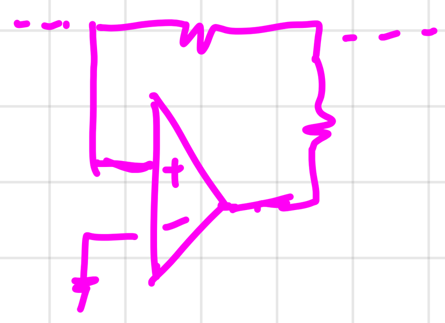
b) Compute the analytical dependence of the output main parameters on x pot position.



a) We see two possible feedback path ⟶ positive / negative feedback ⟶ which is going to prevail?



Just pos. feedback ⟶ Shmitt trigger



transient

↳ the ⊖ input slowly go up to the feedback value

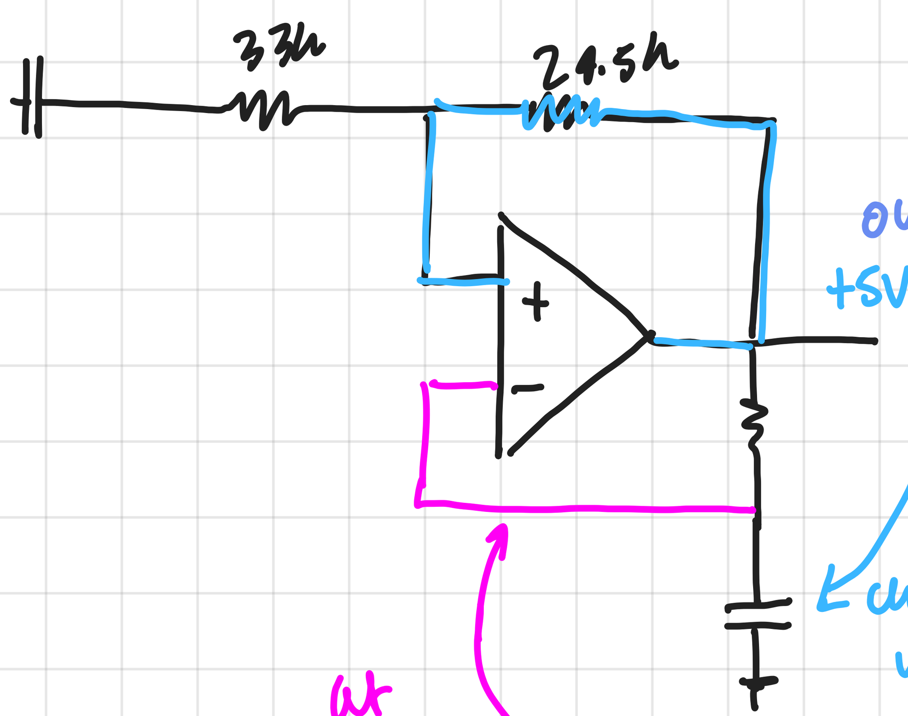
at the fast transient (at the beginning)

at regime ⟶ the negative feedback is stronger

transient ⟶ pos. feedback

regime ⟶ neg. feedback

↳ So analyzing the stage:



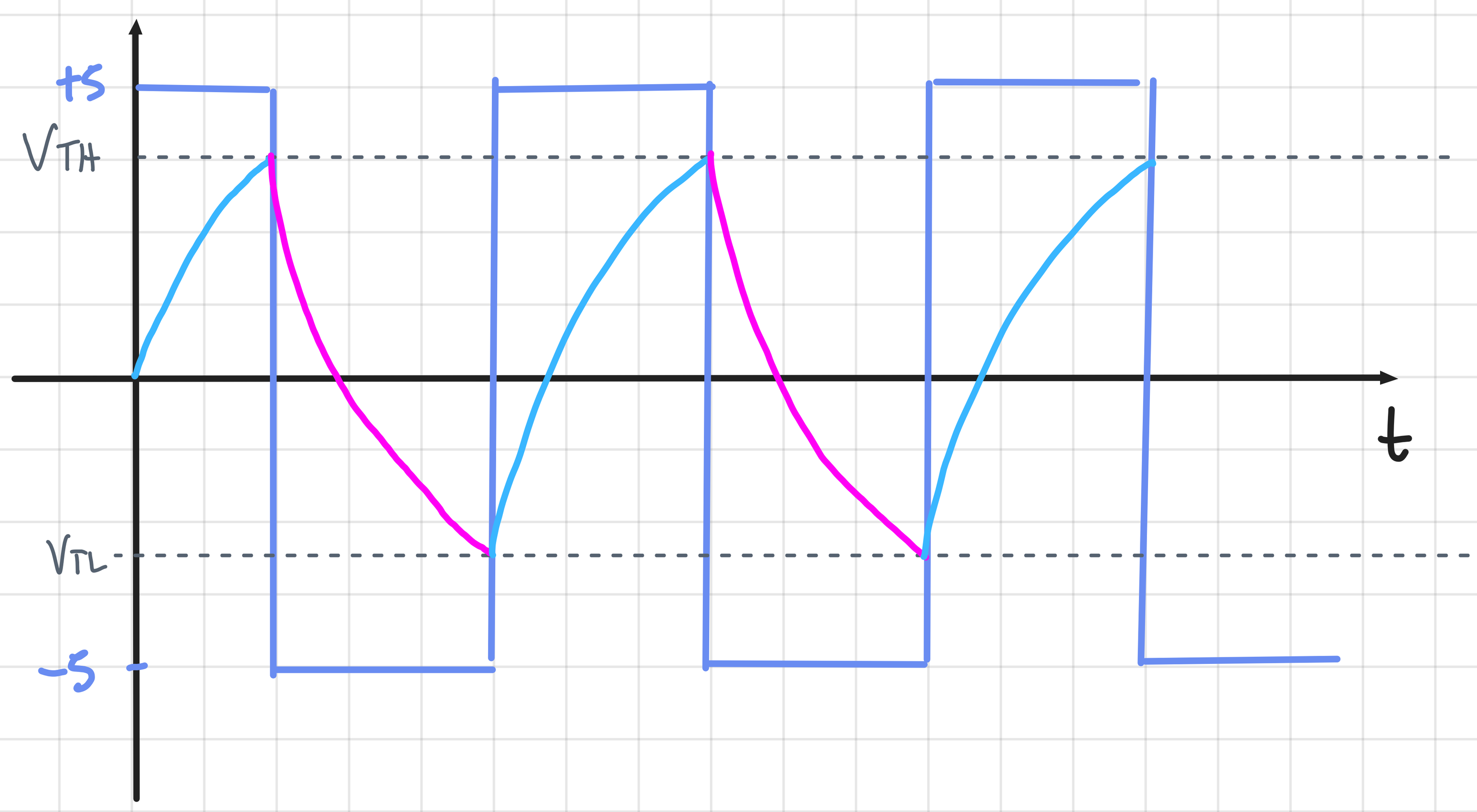
⟶ oscillator circuit

output +5V / -5V

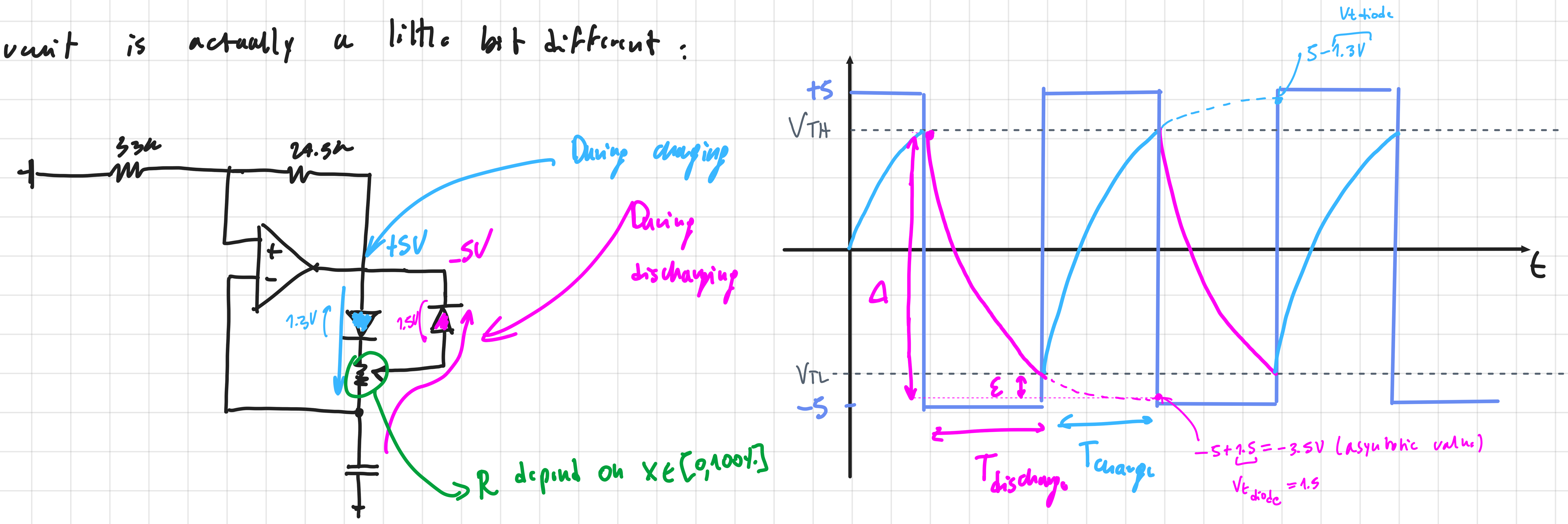
discharges and so on

charges up C

at regime neg. feedback



↳ our circuit is actually a little bit different :



Thresholds : $\bullet\ V_{TH/L} = \pm 5V \cdot \frac{33k}{33k+24.5k} = \pm 2.9\,V$

symmetric

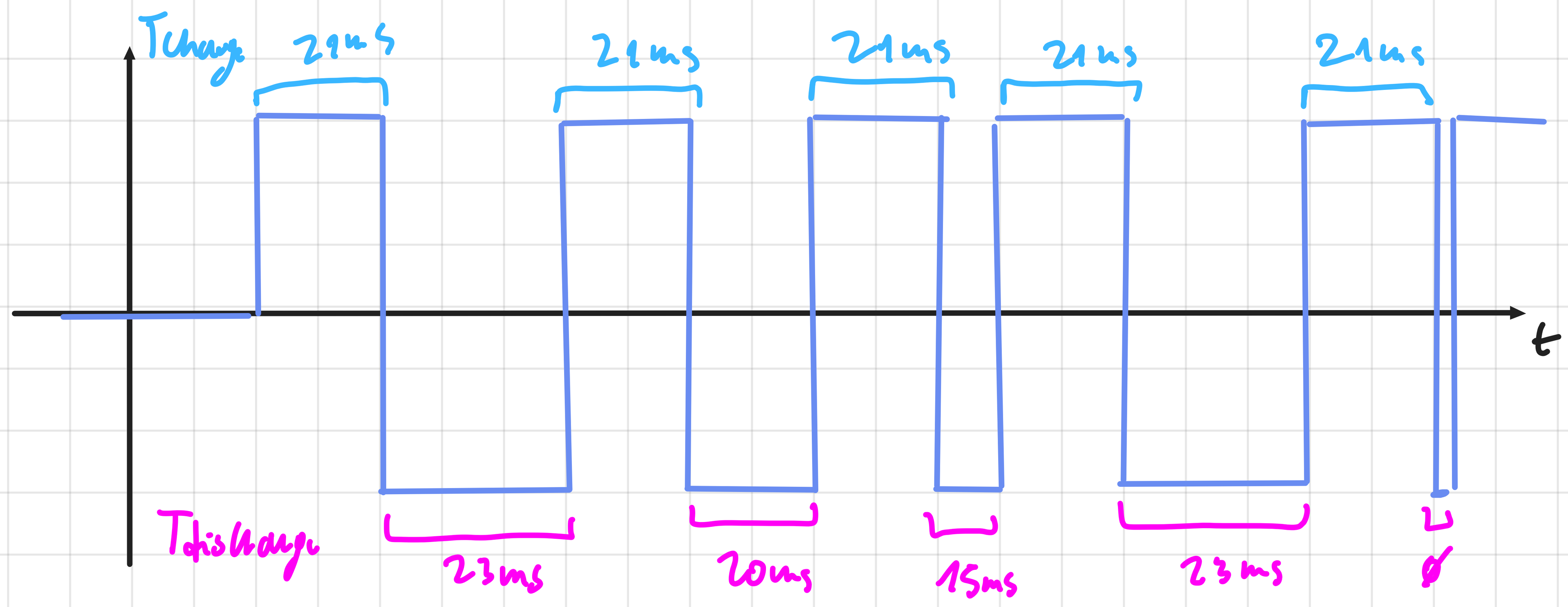
↳ $\Delta = 2.9+3.5$, $\varepsilon = -2.9+3.5$ $\rightarrow T_{discharge} = \tau \ln\frac{\Delta}{\varepsilon} = RC \ln\frac{\Delta}{\varepsilon} = 100k \cdot X \cdot 100n \ln\frac{2.9+3.5}{-2.9+3.5} = 10ms \cdot X \cdot 2.3 = X \cdot 23\,ms$

discharge duration is variable on X

↳ $T_{charge} = 100k \cdot 100n \ln\frac{5-1.3+2.9}{5-1.3-2.9} = 10ms \cdot 2.1 = 21ms$ → const duration

DIODE BLUE sees all R

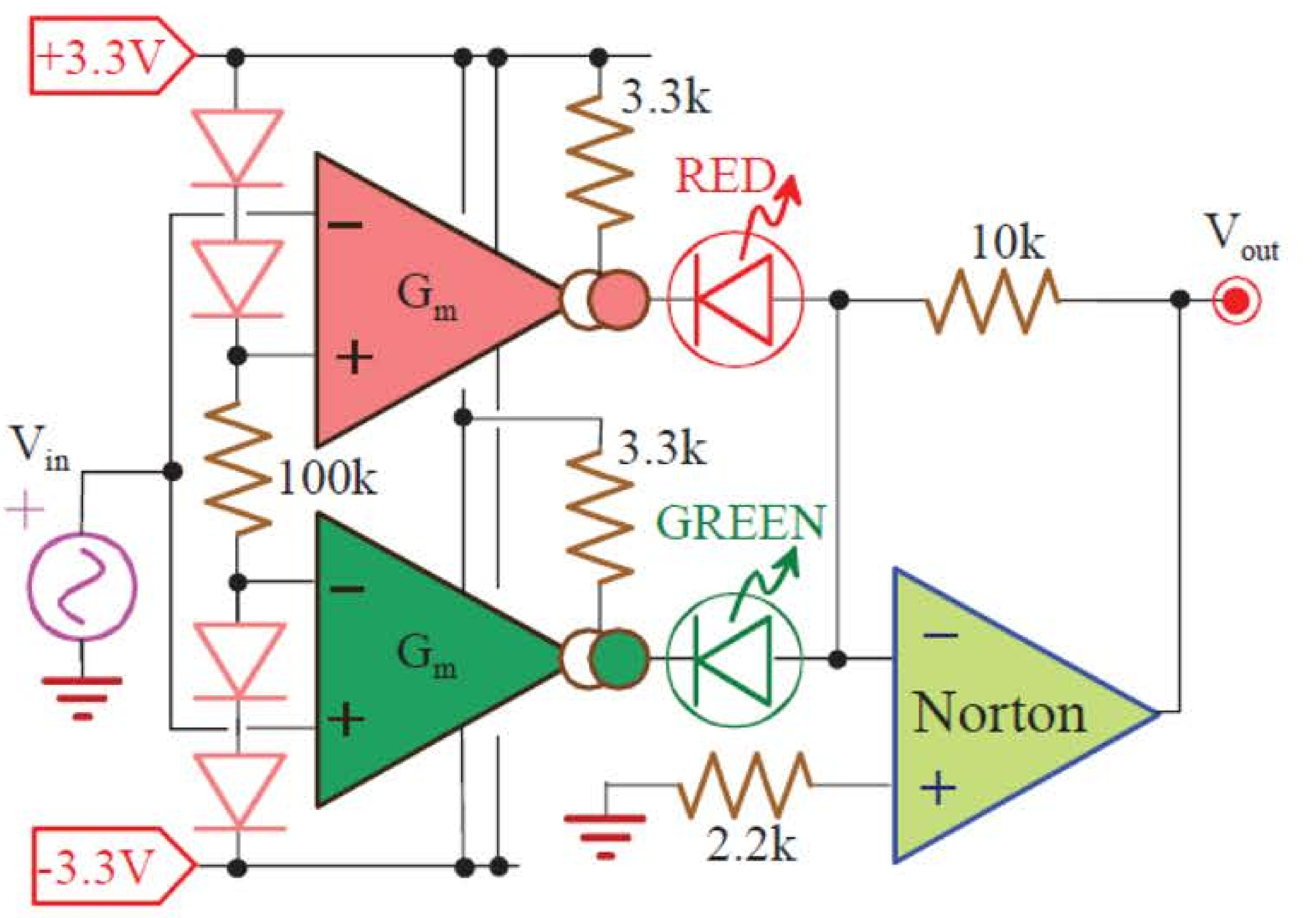
↳ So in the end we have an oscillator :



→ Variable period

↳ $\begin{cases} f_{max} = \frac{1}{21ms+\emptyset} = 48Hz \\ f_{min} = \frac{1}{21ms+23ms} = 23Hz \end{cases}$

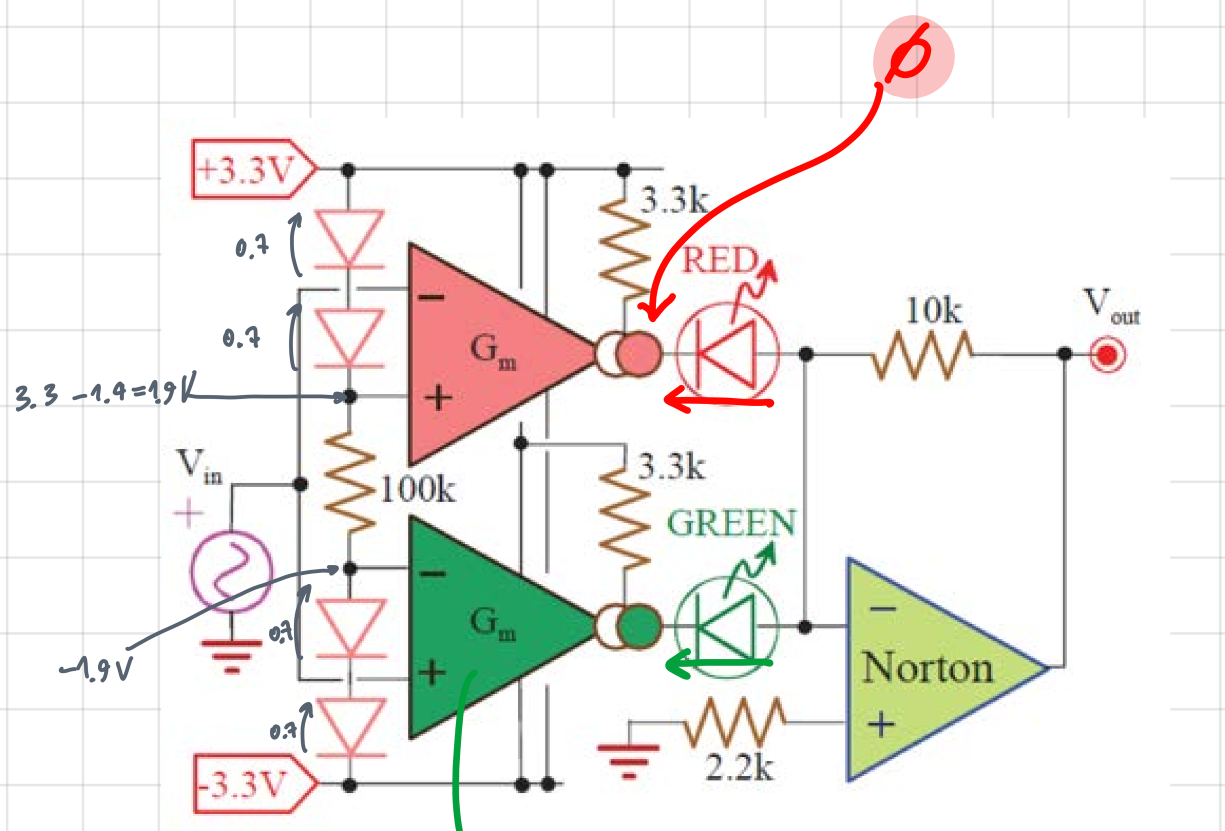
11 (Ex. 15 ES16)



OTAs with control pin at 0V. Diodes with on-voltage of about 0.7V and LEDs with on-voltage of about 1.8V. Norton amplifier with A_i=10.

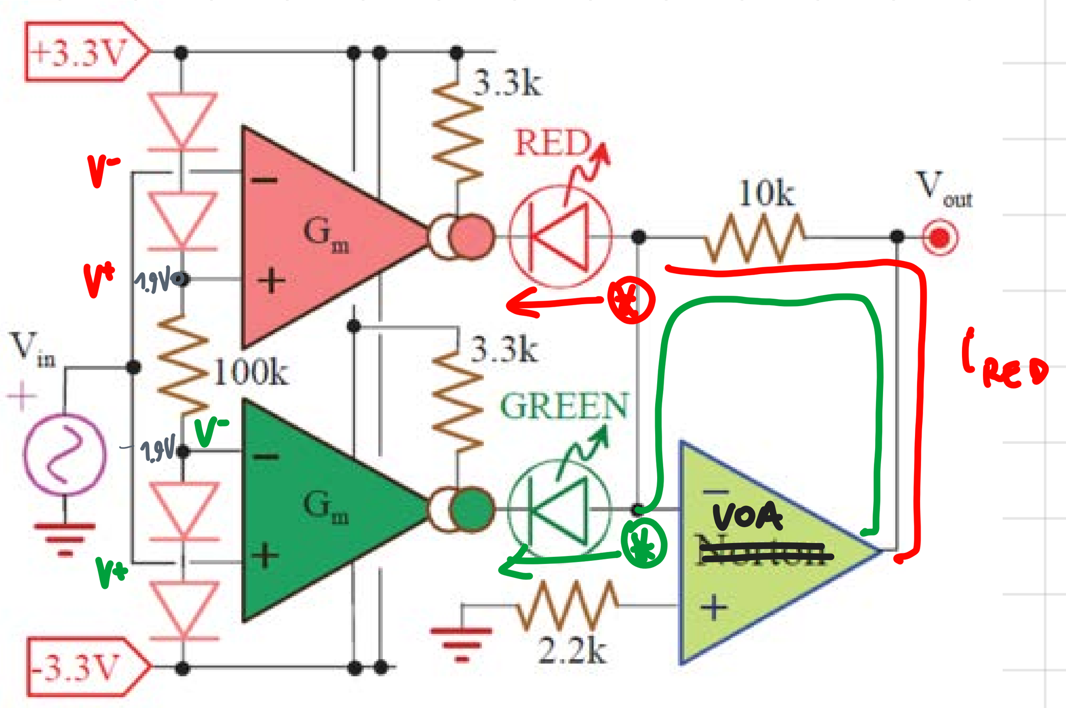
a) Draw the light intensity of both LEDs vs. the V_{in} input voltage across the -3V ÷ +3V range.

b) Compute the V_{out} output voltage vs. V_{in}.



$$G_m = \frac{I_{control}}{V_{th}} = \frac{I_{control}}{25\,mV} = \frac{\frac{3.3V - \emptyset}{3.3k}}{25\,mV} = 40\,\frac{mA}{V}$$

↳ Now start by considering instead of Norton a VOA



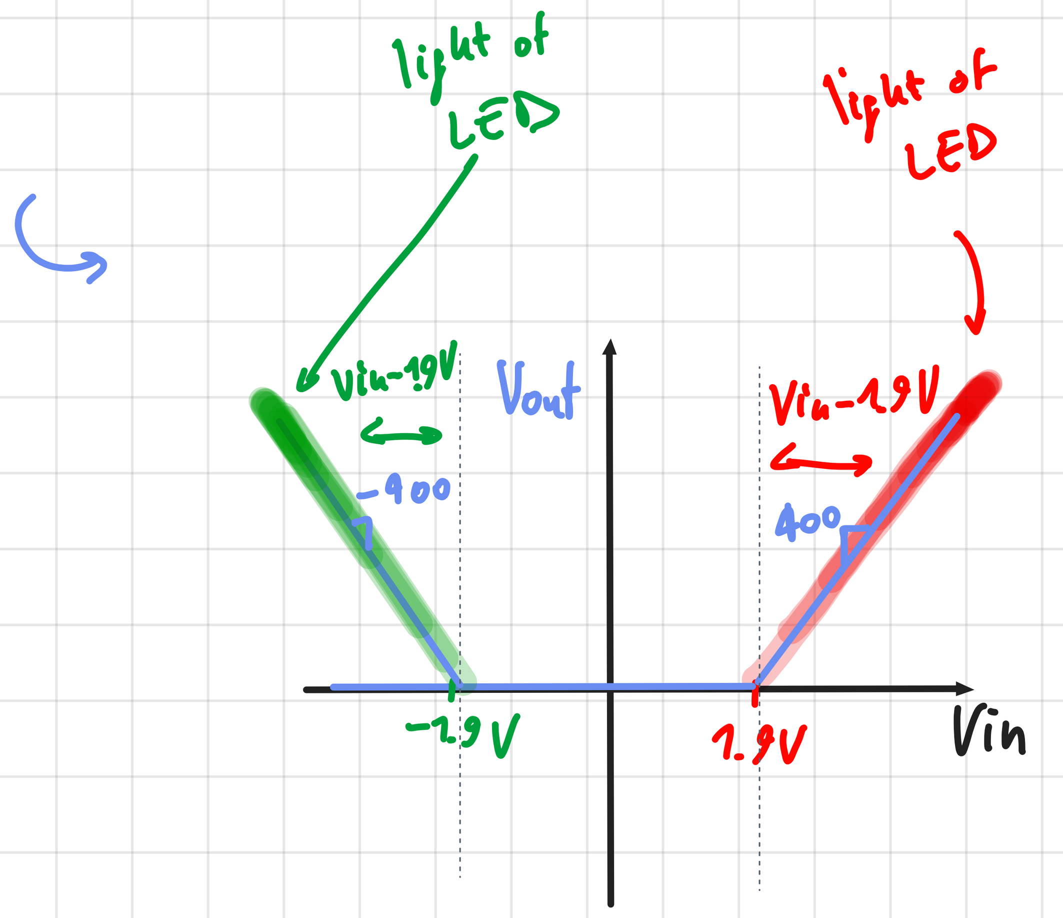
- If $\underset{V_{in}}{V^-} > \underset{1.9V}{V^+}$ → we have a current on RED LED

↳ $V_{out} = \overbrace{(V_{in} - 1.9V) \cdot 40\,\frac{mA}{V}}^{i_{RED}} \cdot \underbrace{10k\Omega}_{}$; $400\,\frac{V}{V}$

- If $V_{in} < 1.9V$ → $i_{RED} = 0$

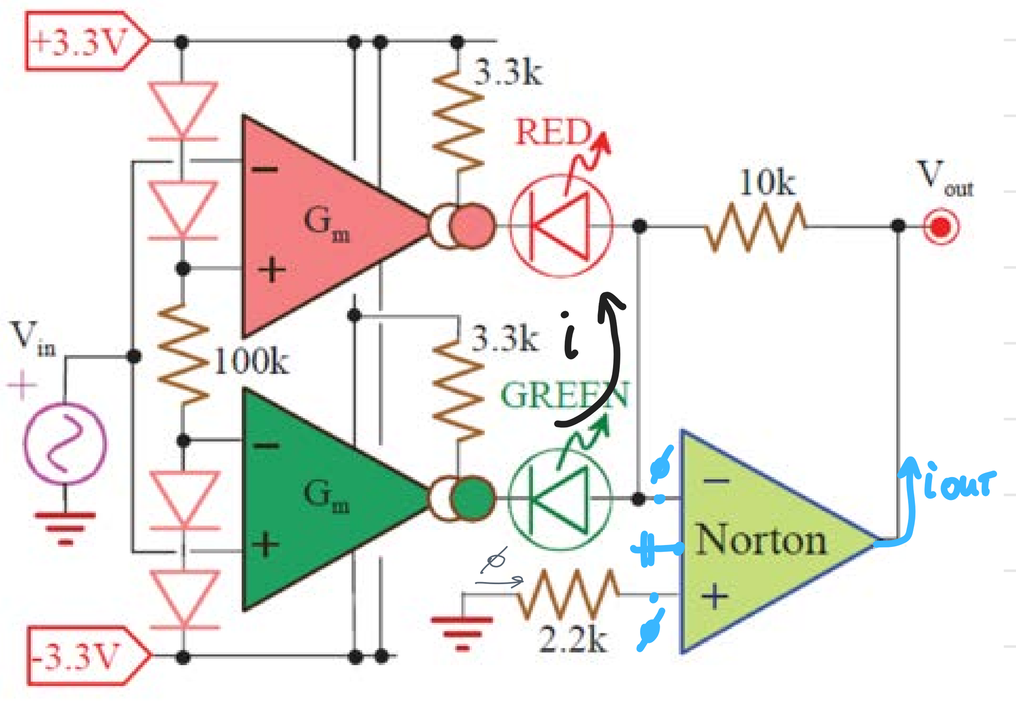
- If $\underset{-1.9V}{V^-} > \underset{V_{in}}{V^+}$ → we have a current on GREEN LED

↳ $V_{out} = -|V_{in} - 1.9V| \cdot 40\,\frac{mA}{V} \cdot 10k\Omega = \underbrace{-(V_{in} - 1.9V)}_{>0} \cdot 400$



So the characteristic is very similar to this

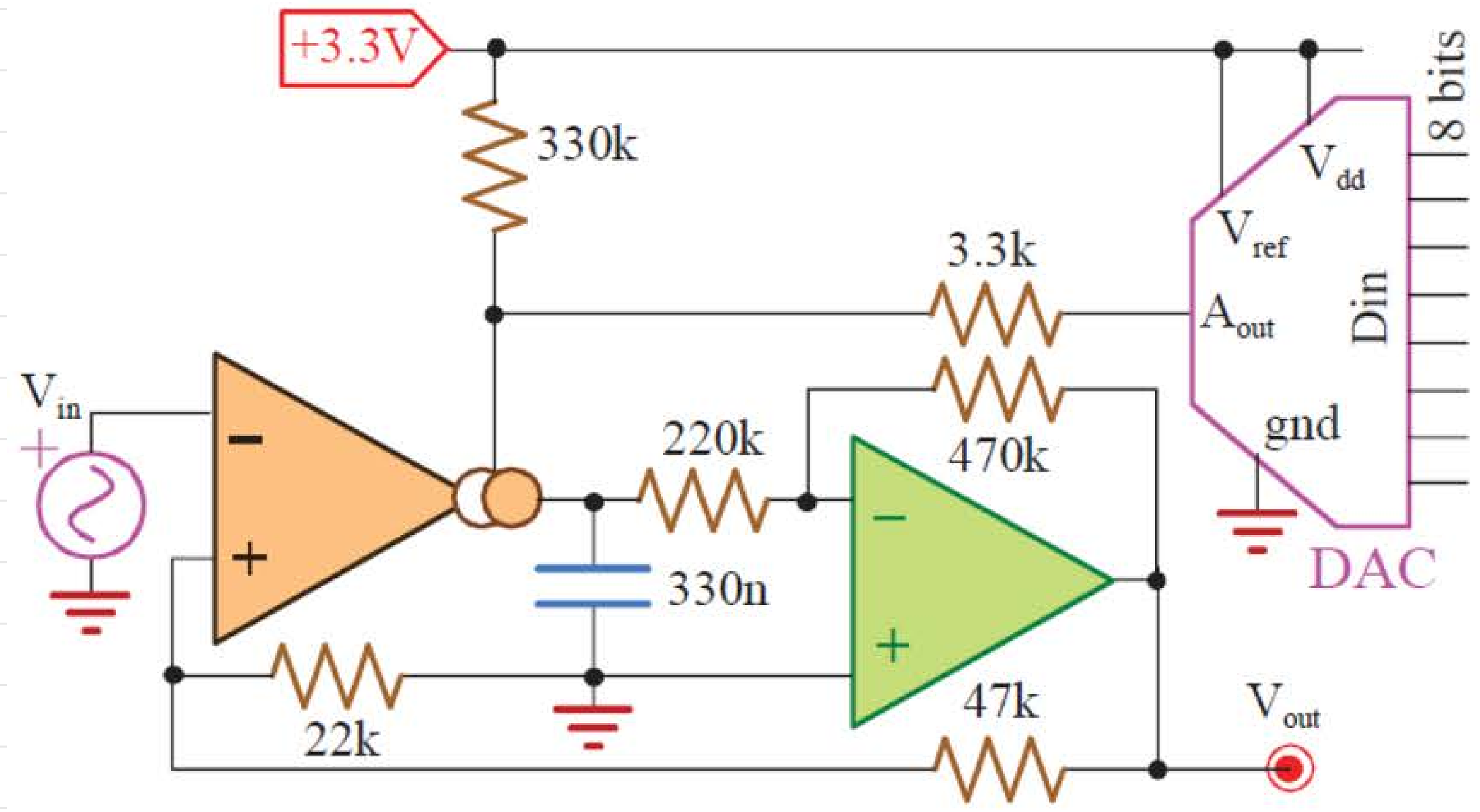
→ Now consider that we actually had a Norton (Current Mode OpAmp) and not a VOA



→ Norton: $i_{OUT} = A_i(i^+ - i^-) = A_i(\emptyset - i_{out} + i)$

↳ $i_{out} = \frac{A_i}{1+A_i}\, i_{RED} = \frac{10}{11}\, i_{RED}$ $\qquad V_{out} = i_{OUT} \cdot 10k$

(12) (Ex16-ES16)

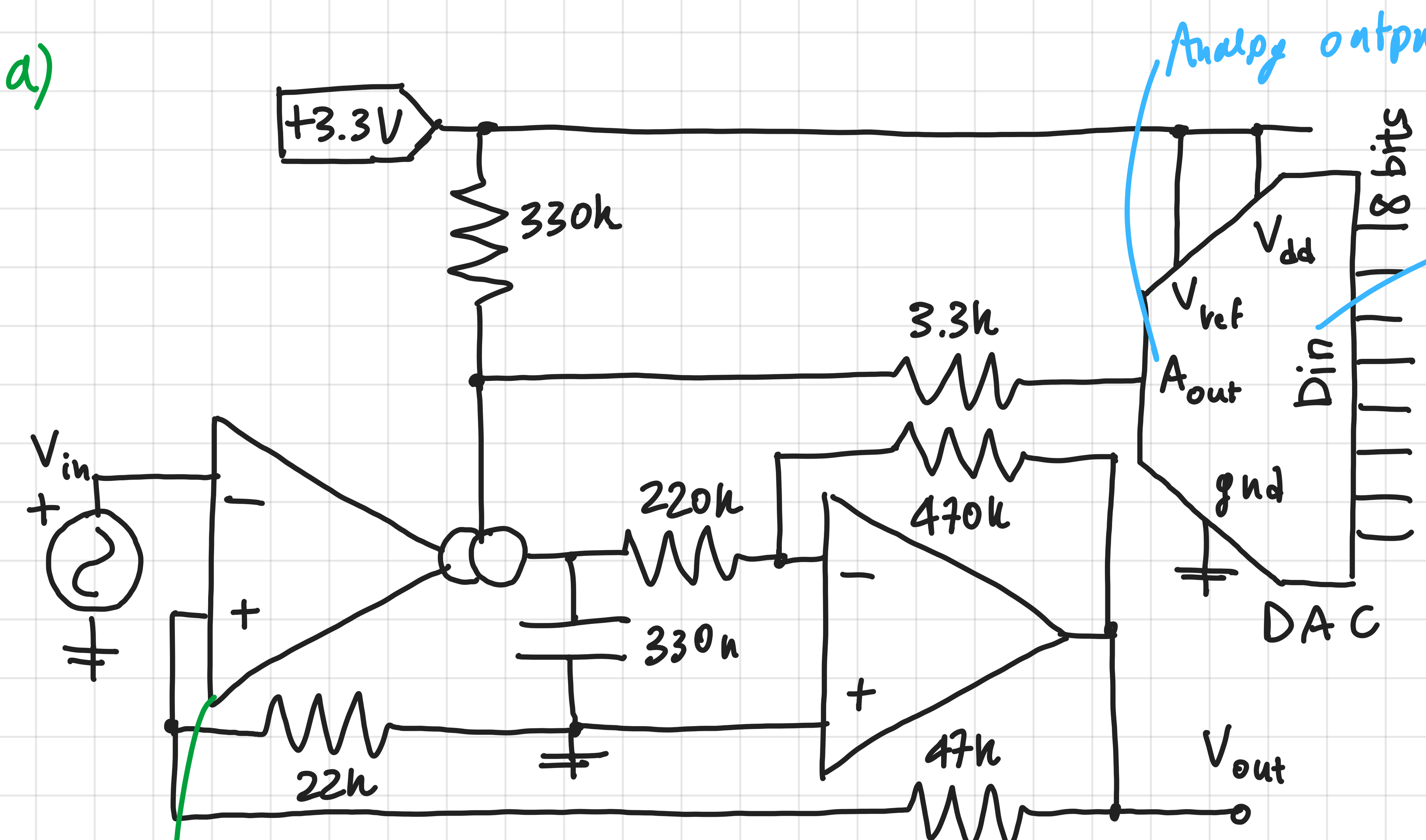


OTA with control pin at 0V and ±5V power supply.

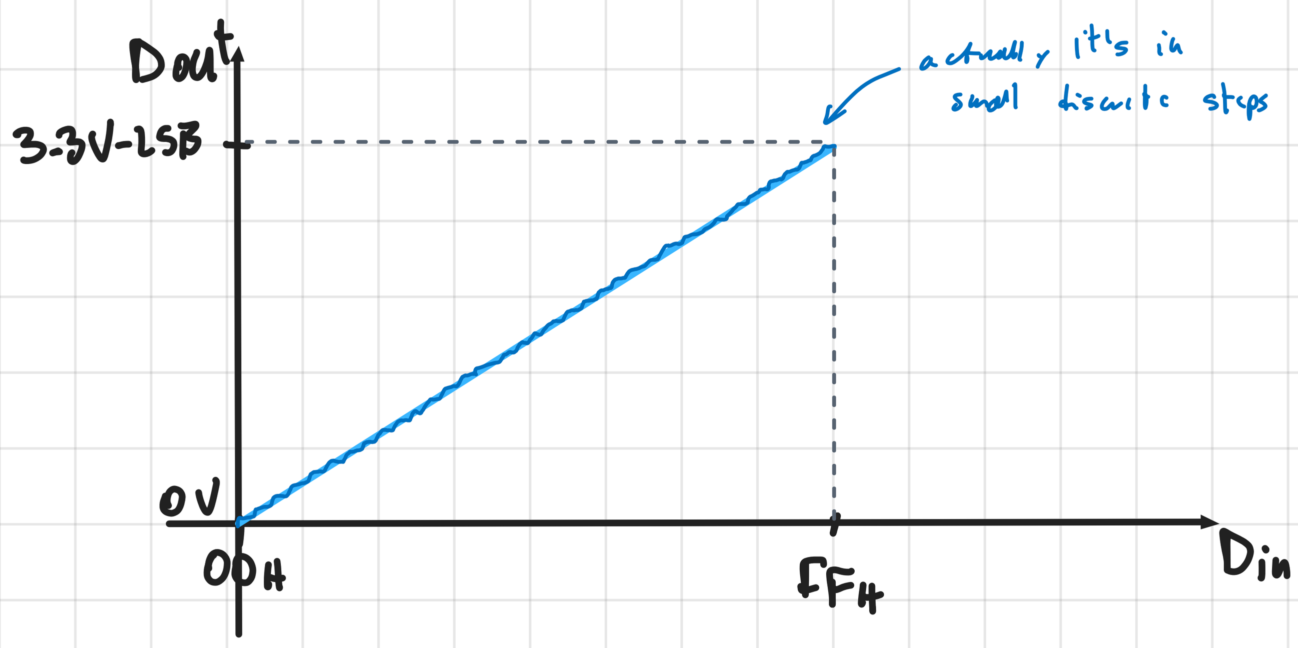
a) Compute the OTA's transconductance as a function of D_{in}.

b) Compute the real $v_{out}(f)/v_{in}(f)$ gain, bandwidth, and stability vs. the input digital code D_{in}.

a)



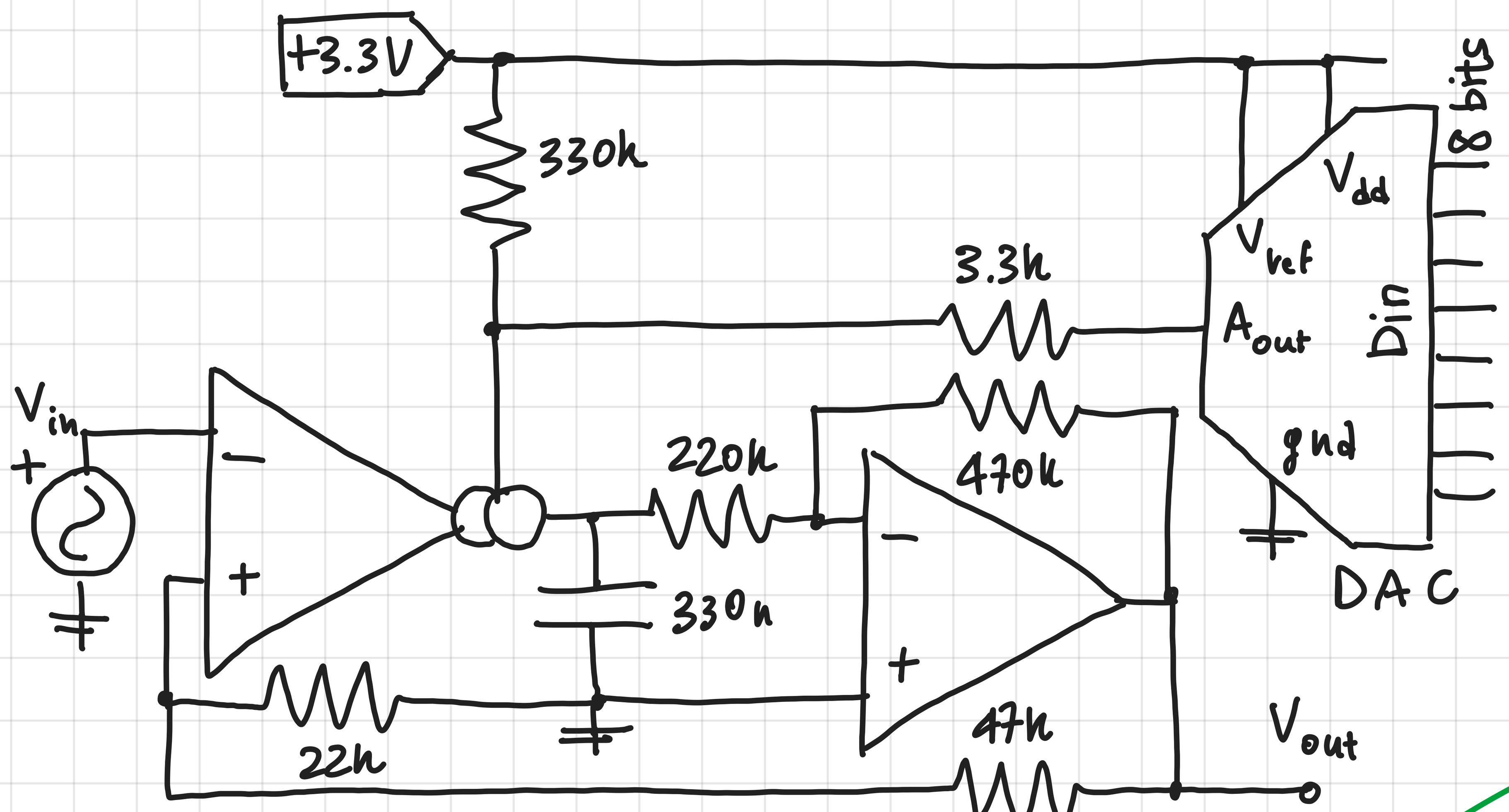
digital input → $A_{out} = V_{ref} \cdot \frac{D_{in}}{2^8} = \frac{3.3V}{256} \cdot D_{in} = 12.9mV \cdot D_{in}$



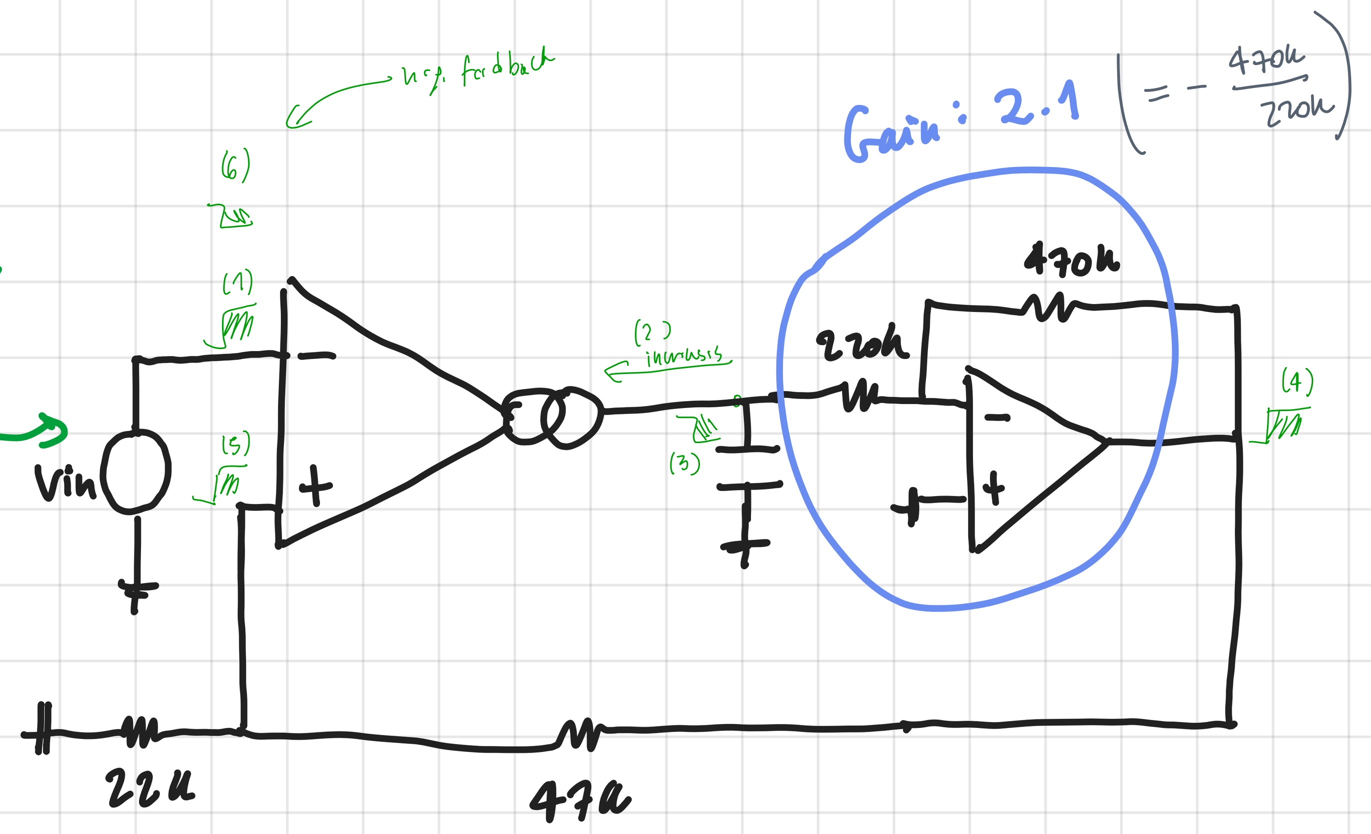
$LSB = \frac{3.3V}{2^8} = 12.9\,mV$

$$G_m = \frac{I_{control}}{25mV} = \frac{\frac{3.3V}{330k} + \frac{A_{out}}{3.3k}}{25mV} = 0.4\frac{mA}{V} + 156\frac{\mu A}{V} \cdot D_{in} = \begin{cases} G_{m_{min}} = 0.4\frac{mA}{V} & \text{for } D_{in} = 00_H \\ G_{m_{max}} = 40\frac{mA}{V} & \text{for } D_{in} = FF_H \end{cases}$$

b) ↳ Let's study the circuit:



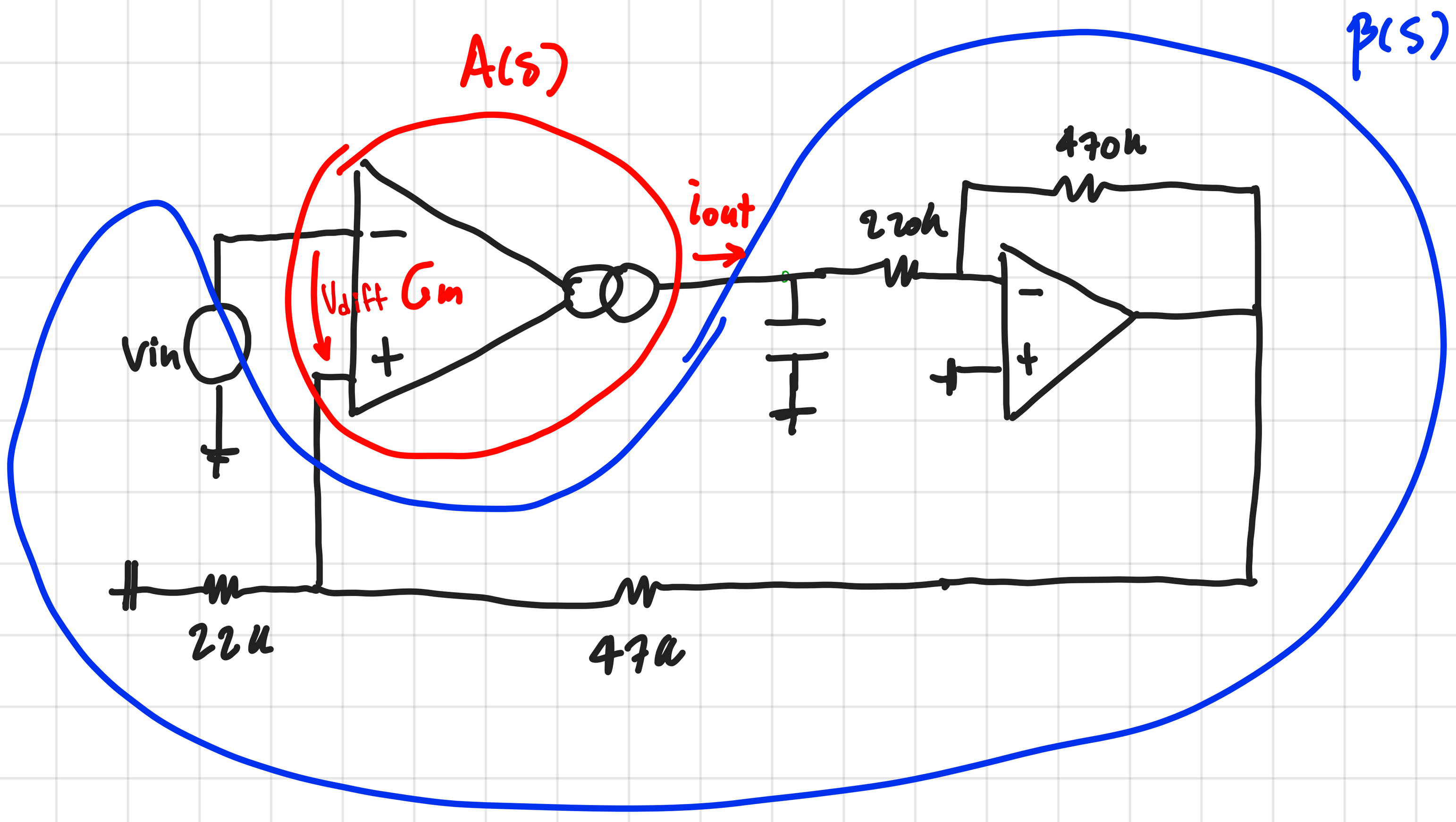
Let's simplify it



→ Ideal Gain

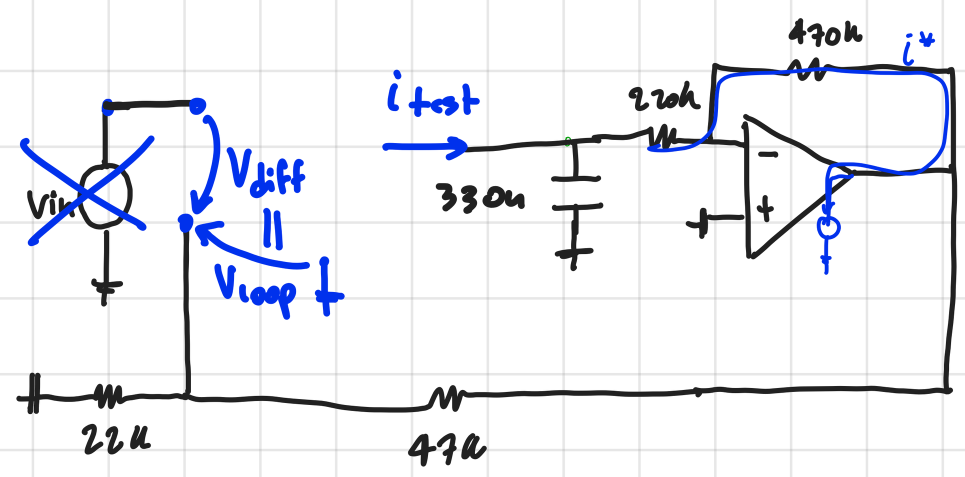
$$V_{out} = V_{in}\underbrace{\left(1 + \frac{47k}{22k}\right)}_{3.1}$$

Let's study the stability:



→ A(s) : $A(s) = G_m = \frac{i_{out}}{V_{diff}}$ $\left[\frac{A}{V}\right]$

→ β(s) : $\frac{V_{diff}}{i_{out}} = \frac{V_{loop}}{i_{test}} =$ $\beta(0) = \frac{470k \cdot 22k}{22k + 47k} = 149.900 \left[\frac{V}{A}\right]$; $\beta(\infty) = \varnothing$

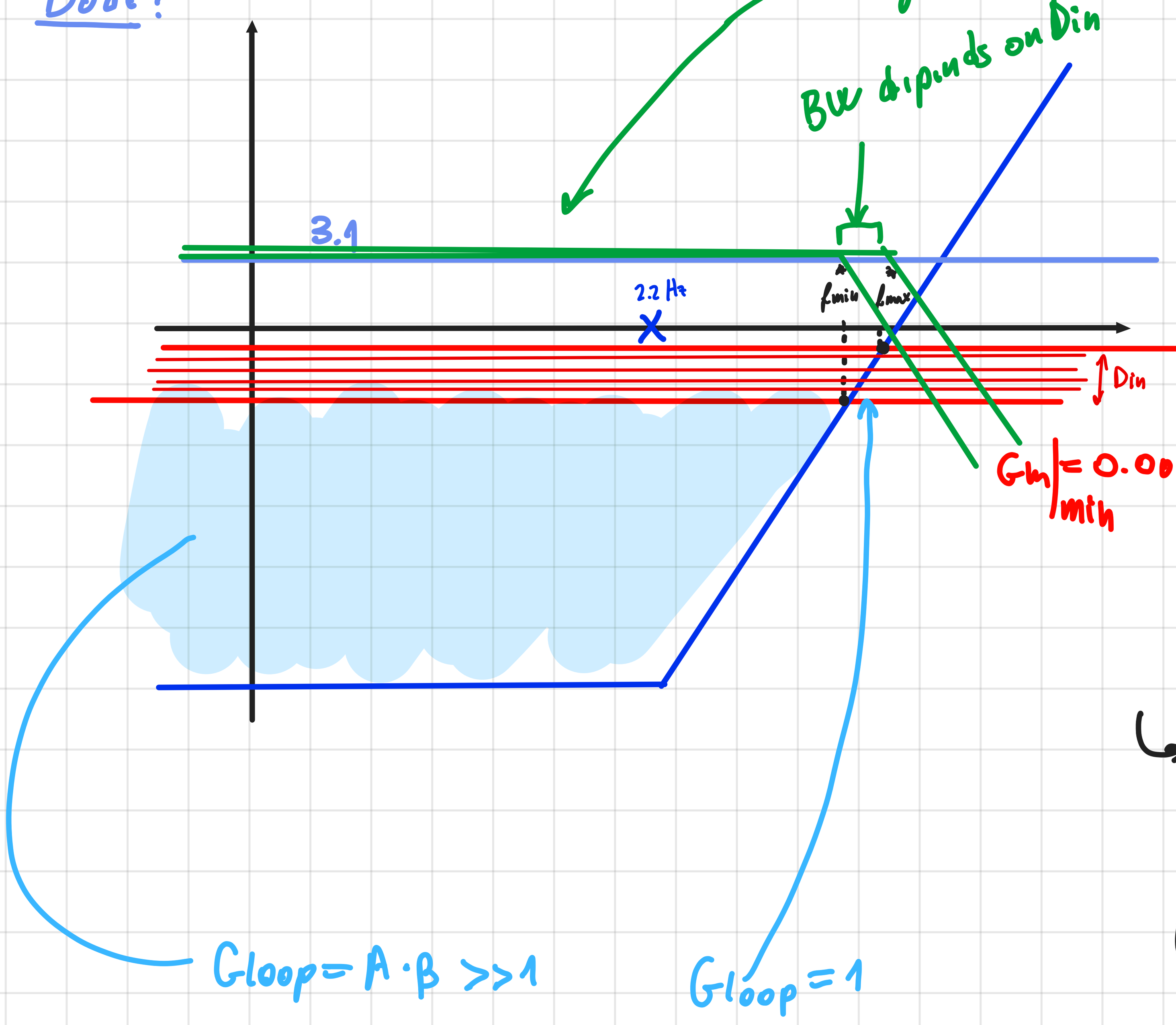


@DC $i^* = i_{test}$

@HF $i^* = 0$

→ pole: $f_{pβ} = \frac{1}{2\pi\, 220k\, 330n} = 2.2Hz$

Bode:



$$\frac{1}{\beta}(s) = \begin{cases} \frac{1}{\beta}(0) = 6.7 \cdot 10^{-6} \\ \frac{1}{\beta}(\infty) = \infty \end{cases}$$

A(s)

Ideal Gain (3.1)

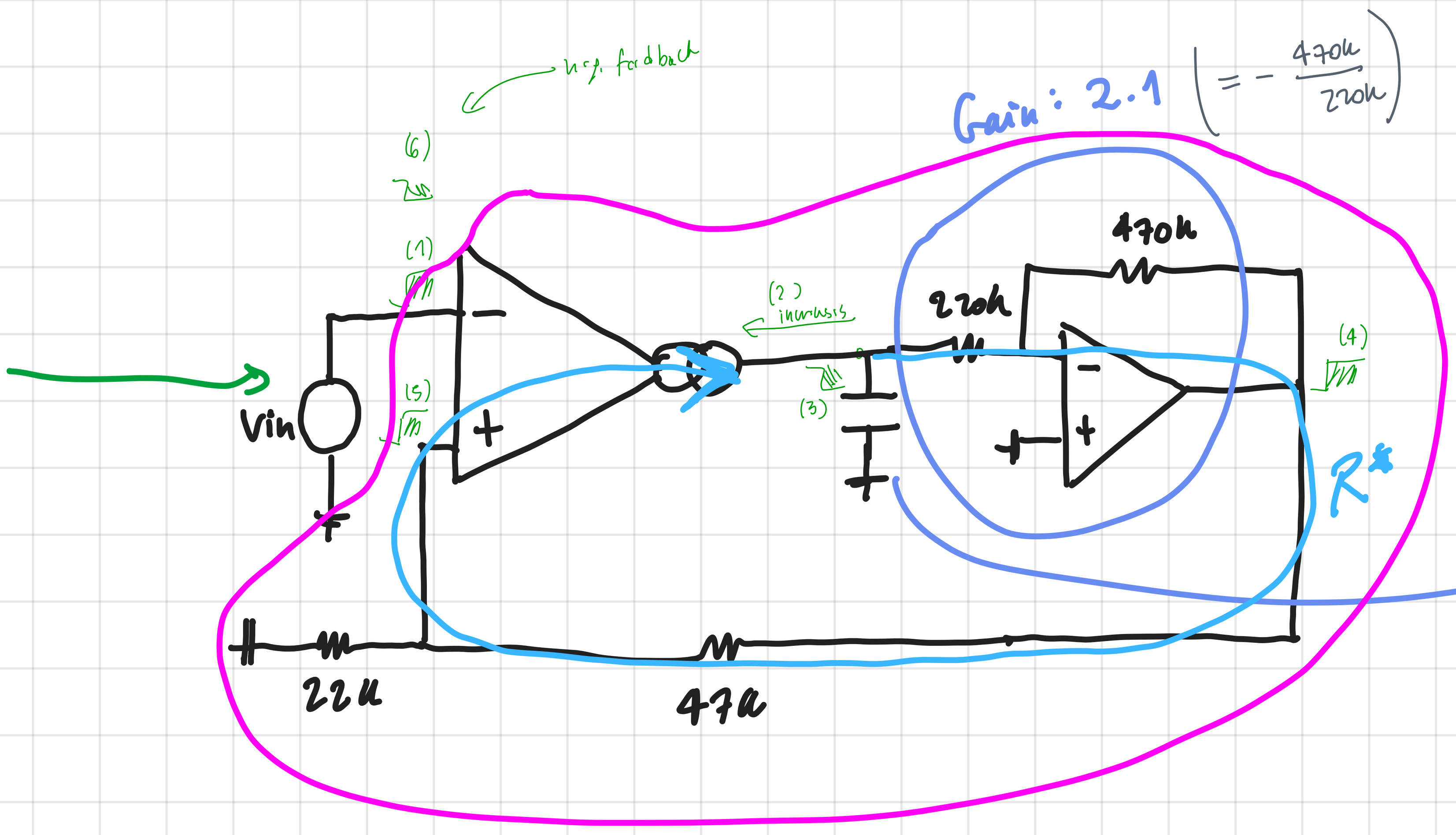
$G_m|_{max} = 0.04 = 40\ \frac{mA}{V}$

$G_m|_{min} = 0.0004 < 0.4\ \frac{mA}{V}$

$$\begin{cases} \text{min BW}: f^*_{min} = 2.2\,Hz \cdot \frac{0.4m}{6.7 \cdot 10^{-6}} = 131\ Hz \\ \text{max BW}: f^*_{max} = 2.2\,Hz \cdot \frac{40m}{6.7 \cdot 10^{-6}} = 13\ kHz \end{cases}$$

It's better to this approx to a const. ideal gain

Note: Actually for the ideal gain there was a closed loop pole:



So it depends on Gloop

Pole: $f_p = \frac{1}{2\pi C \cdot R^*} = \frac{(1+G_{loop})}{2\pi \cdot C \cdot 220k}$

$R^* = \frac{(220k)}{(1+G_{loop})}$

must take into account the feedback

12/12/2022

EX08 _ EXAMS

1 09/02/2006 _ EX2

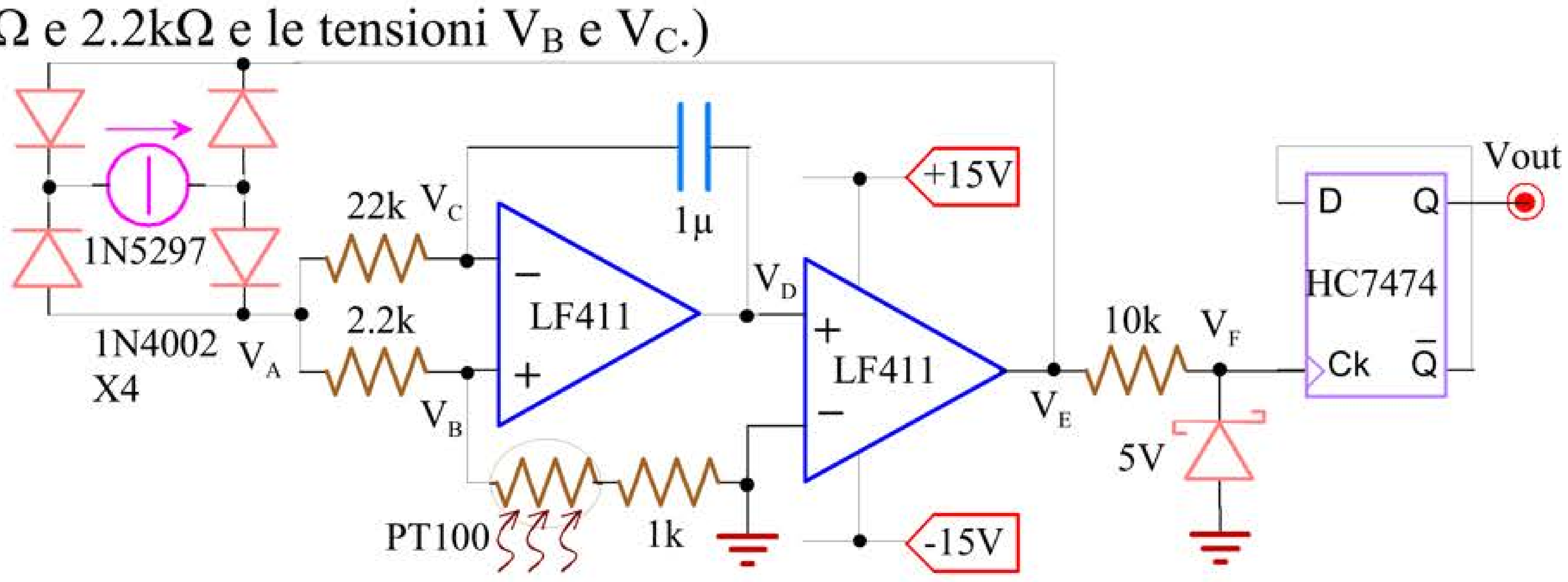
Es. 2

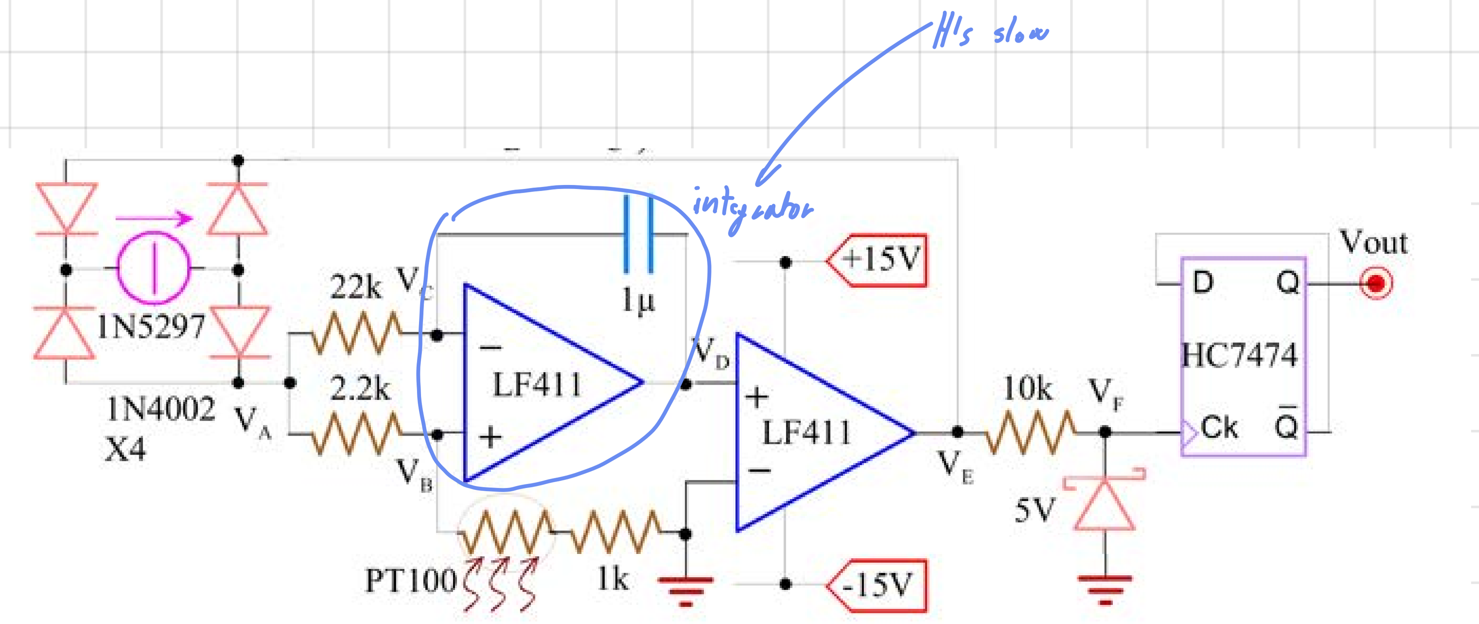
Il 1N5297 è un generatore di corrente integrato che genera 1mA. Il sensore termico è una PT100 che vale 100Ω a 0°C e varia di circa 0.4Ω/°C. Studiare il funzionamento del circuito a 0°C.

a) Spiegare il funzionamento del circuito. (Si suggerisce di partire dall'istante in cui V_E=+15V, per poi ricavare le correnti nelle resistenze da 22kΩ e 2.2kΩ e le tensioni V_B e V_C.)

b) Disegnare le forme d'onda quotate delle tensioni ai nodi e ricavare la frequenza di commutazione di V_{out}.

c) Dire come si modificano le forme d'onda al variare della temperatura misurata dalla PT100.

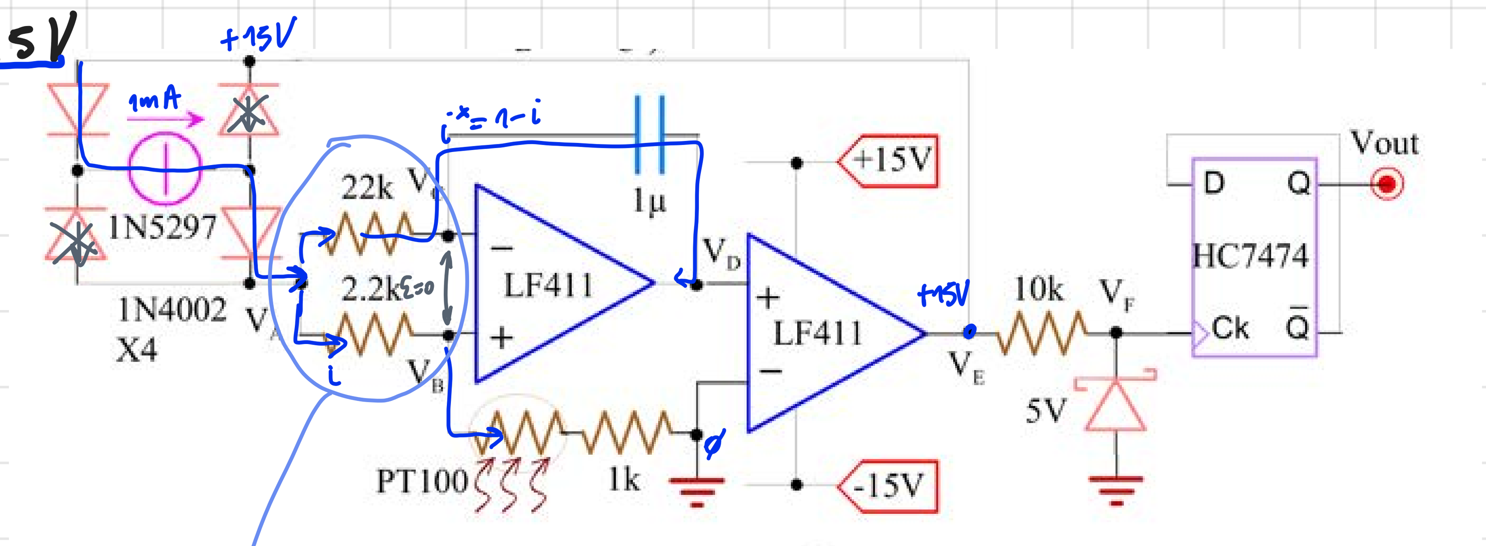


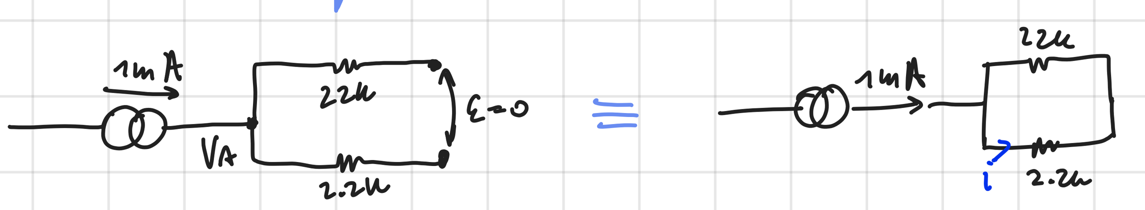


↳ From simple circuit analysis we're not sure about the working principle of the circuit

↳ start by considering the second OpAmp as comparator ⟶ So the output is ±15V

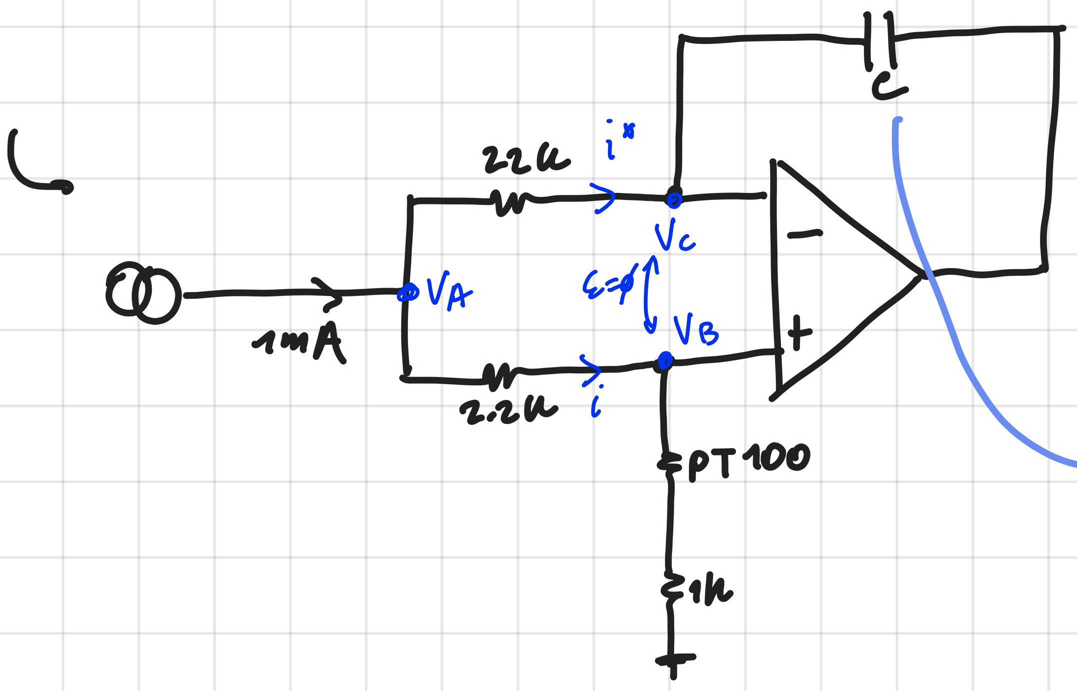
• $V_E = +15V$





$\longrightarrow \quad i = 1mA \cdot \frac{22k}{2.2k + 22k} = 0.91\,mA$

$i^* = 1mA - i = 0.09\,mA$

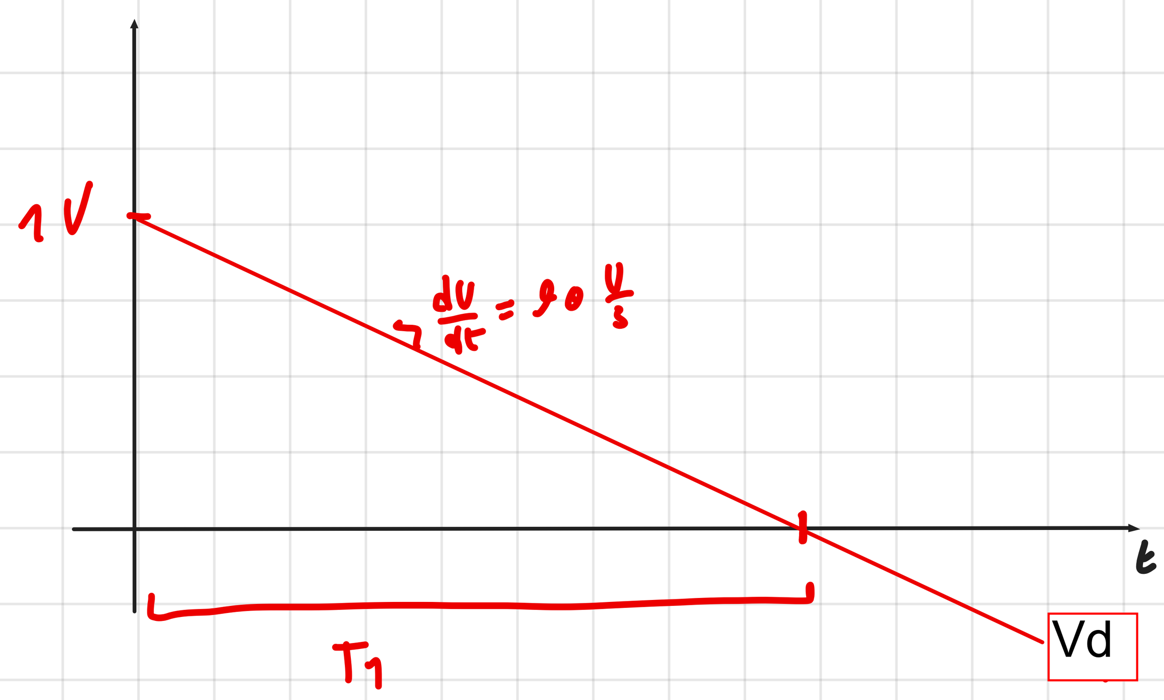


$\longrightarrow \quad V_A = i\,(2.2k + 1k + R_{PT100}) = 0.91mA \cdot 3.2k + 0.91mA\,(100 + 0.4 \cdot T) = 3V + 0.364\frac{mV}{°C} \cdot T$ temperature

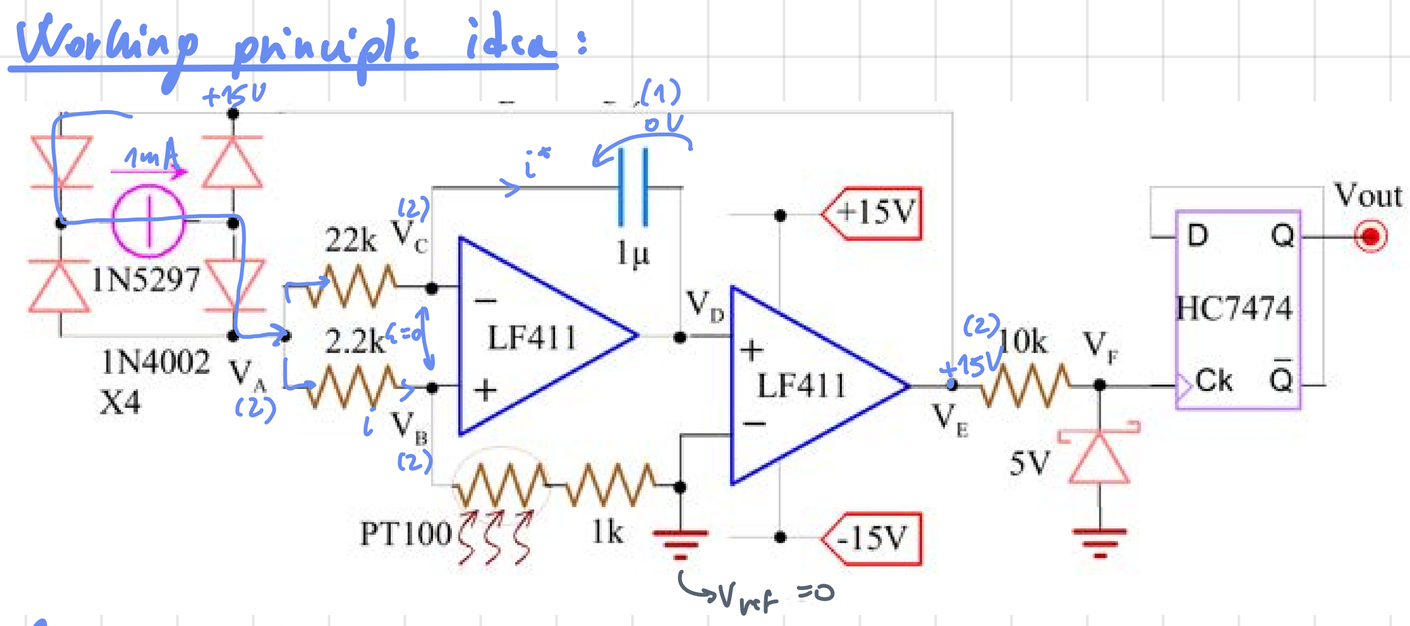
$\longrightarrow \quad V_B = V_C = i\,(R_{PT100} + 1k) = 0.91mA \cdot 1.1k + 0.364mV \cdot T = 1V + 0.364\frac{mV}{°C} \cdot T$

$\frac{dV_c}{dt} = \frac{i^*}{C} = \frac{0.09\,mA}{1\,\mu F} = 90\,\frac{V}{s}$

↳ Working principle idea :



$T_1 = \frac{1V}{\frac{dV}{dt}} = \frac{1V}{90\frac{V}{s}} = 11.1\,ms$

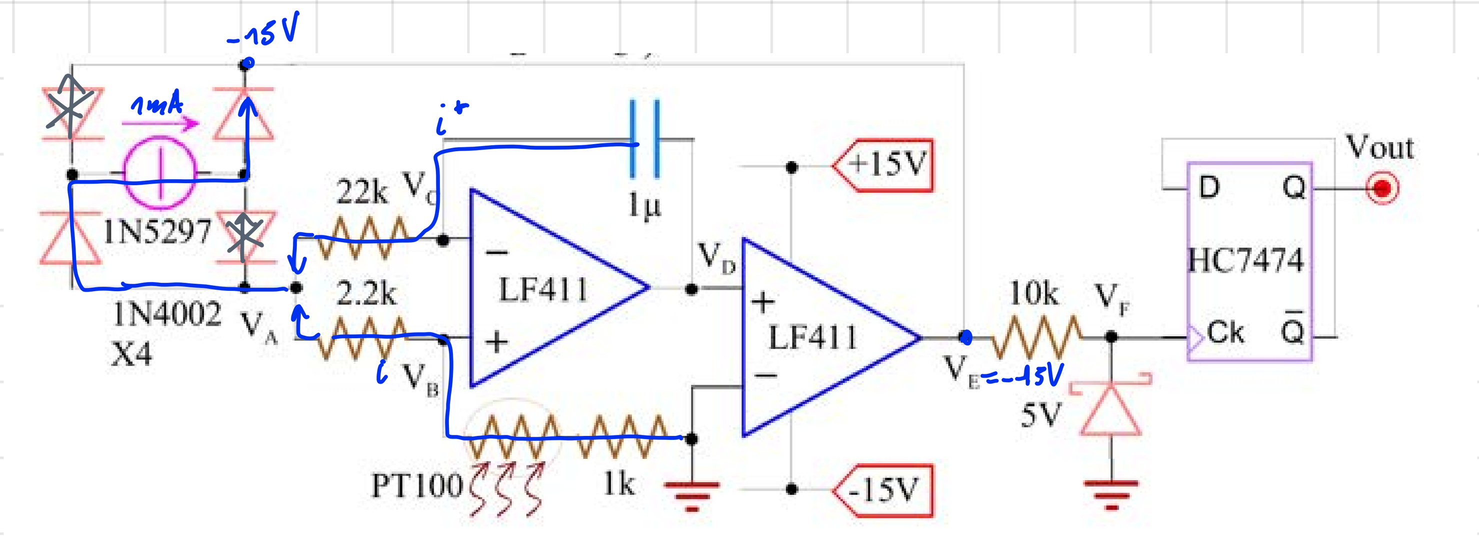


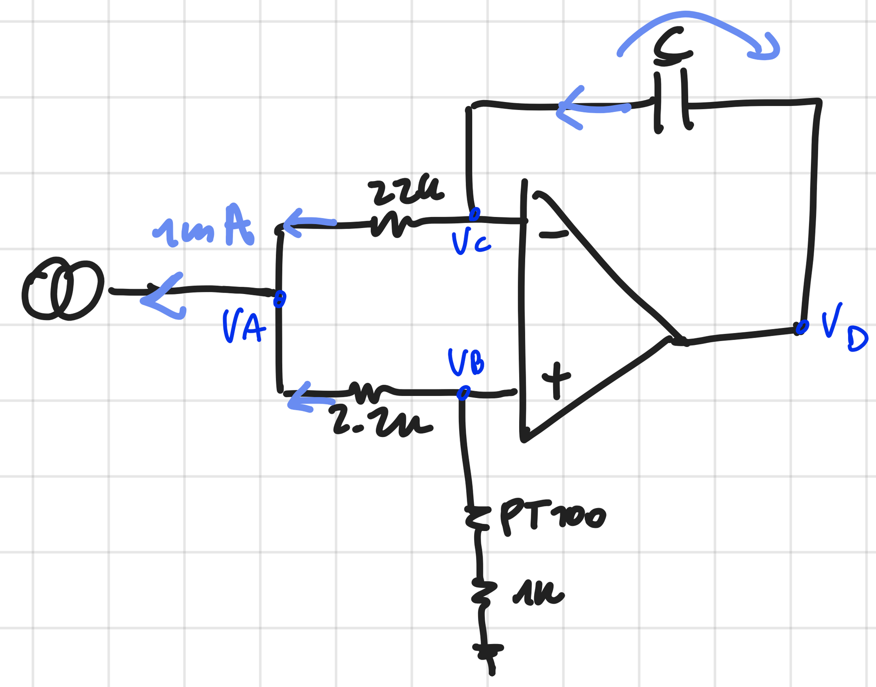
1. Start with discharged C , $V_E = +15V$

2. Compute V_A, V_B, V_C (done before)

3. $V_D = V_C = V_B$ ⟶ when $V_D < 0$ (after T_1) comparator output $V_E \longrightarrow -15V$
(when C charges up) V_{ref}

• $V_E = -15V$

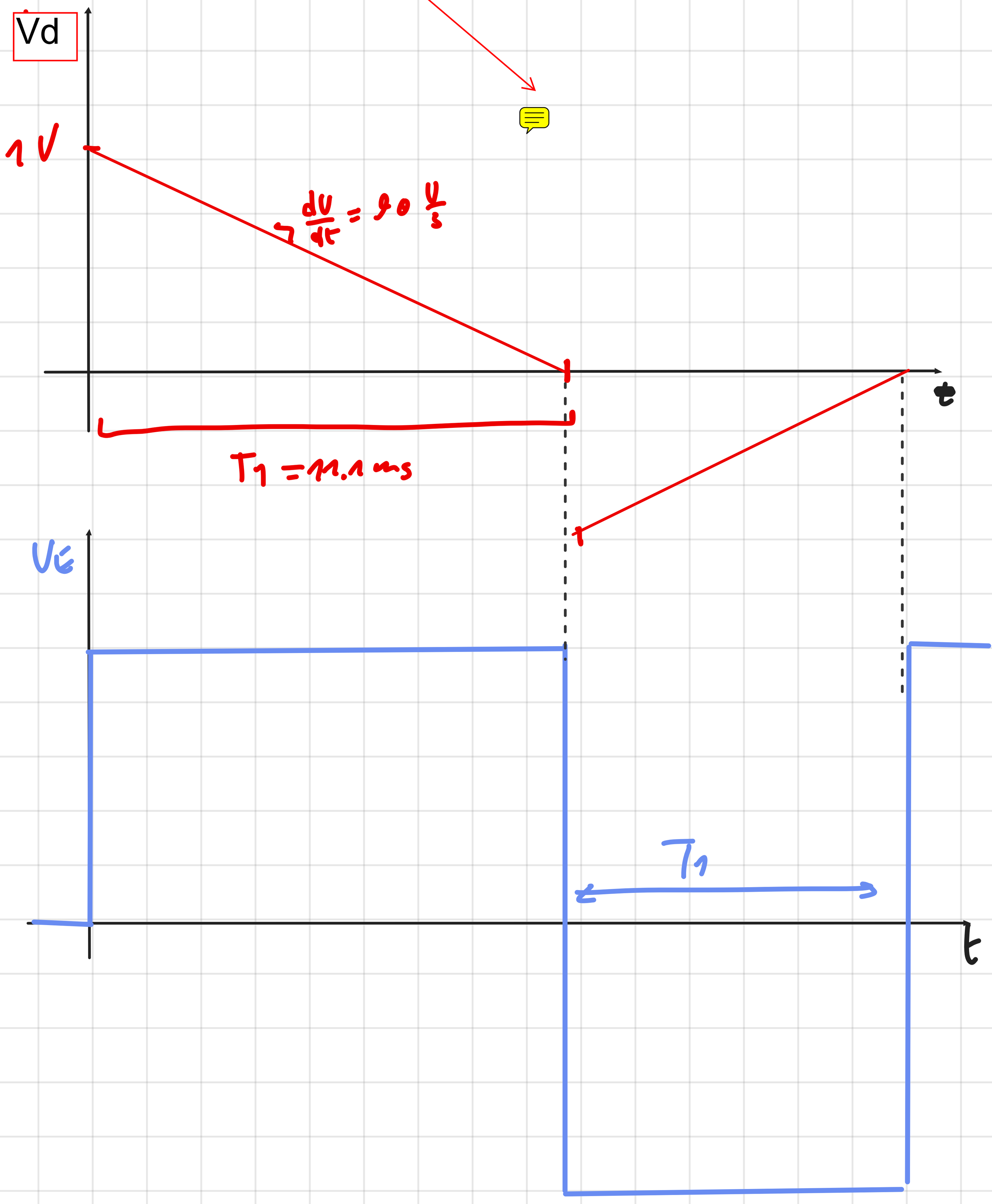




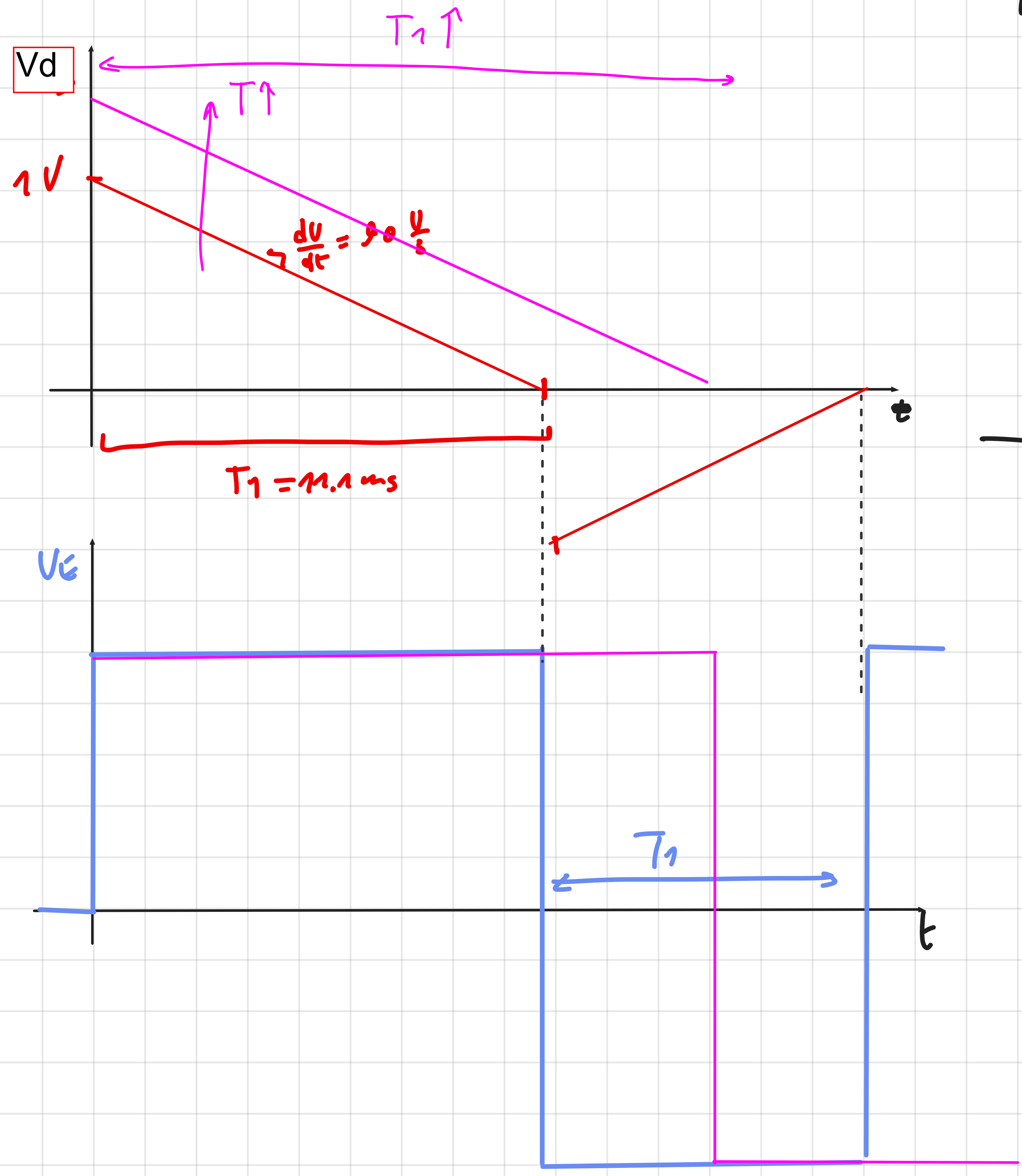
Applying the same considerations:

- $V_A = -3V - 0.364 \frac{mV}{°C} T$
- $V_B = V_C = -1V - 0.364 \frac{mV}{°C} T$

the comparator will charge up in the opposite direction



Note: V_B depends on T if $T\uparrow$ $|V_B|\uparrow \rightarrow T_1\uparrow \rightarrow f\downarrow$

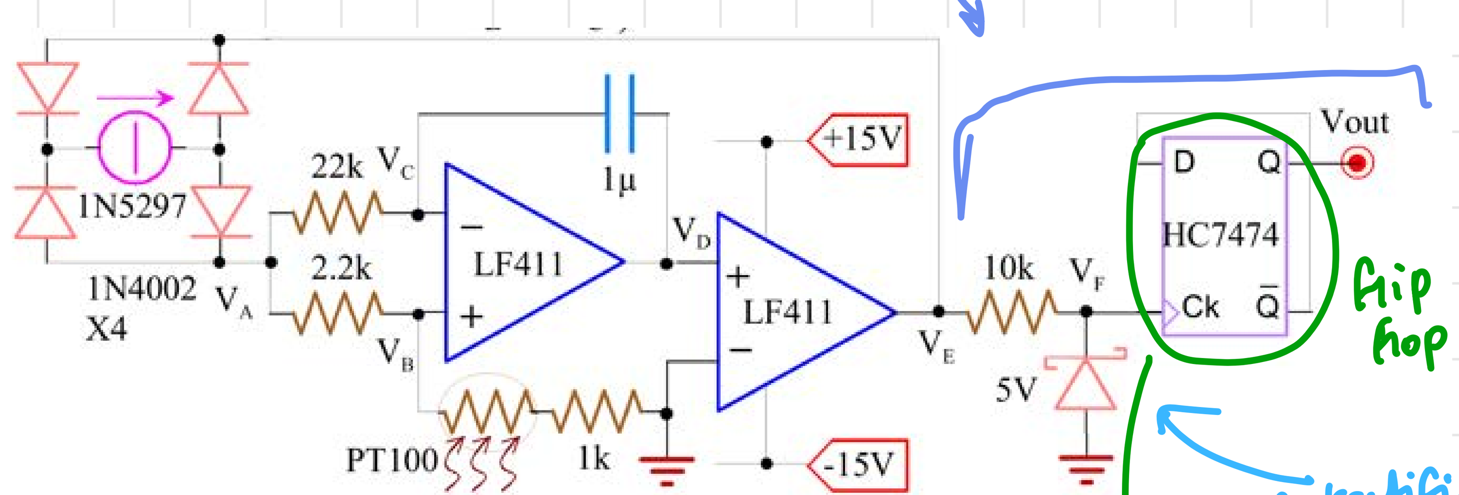


$$\rightarrow f_{osc}(0°C) = \frac{1}{2 \cdot 11.1ms} = 45 \text{ Hz}$$

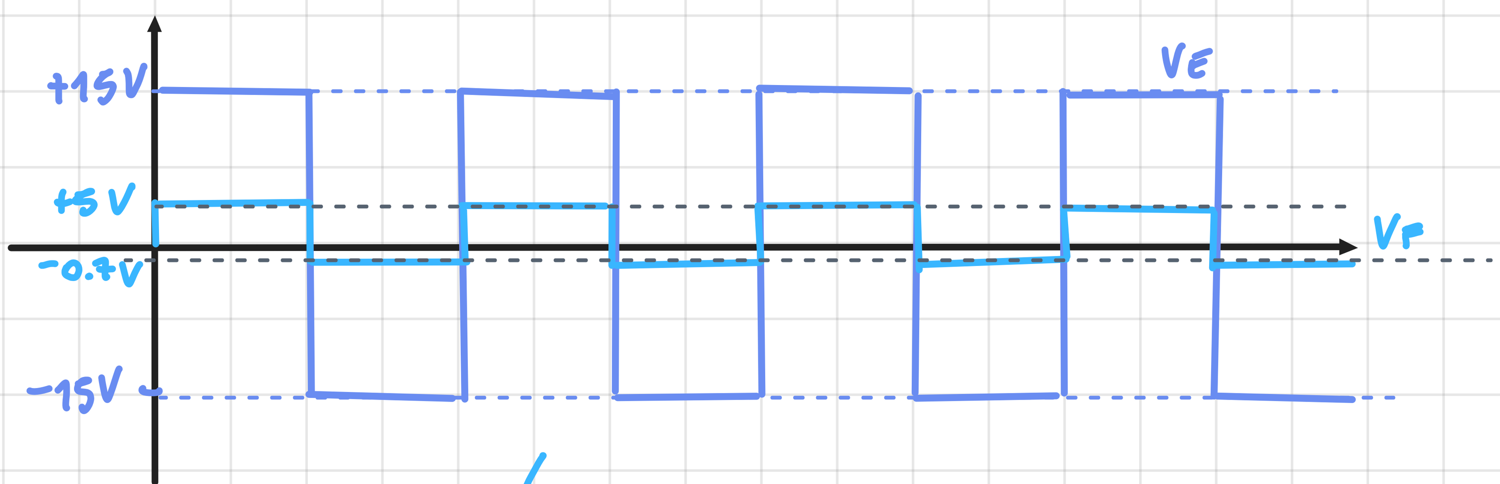
$$f_{osc}(T) = \frac{1}{2 \cdot \frac{1V + 0.364 \frac{mV}{°C} T}{90 \frac{V}{s}}} = \frac{45 \frac{V}{s}}{1V + 0.364 mV \cdot T}$$

$$\hookrightarrow T_{osc}(T) = \frac{1V}{45 \frac{V}{s}} + \frac{0.364 mV}{45 \frac{V}{s}} \cdot T = 22.2 \text{ ms} + 8.1 \mu s \cdot T$$

↳ Then we consider the second part of the circuit



We have VE:

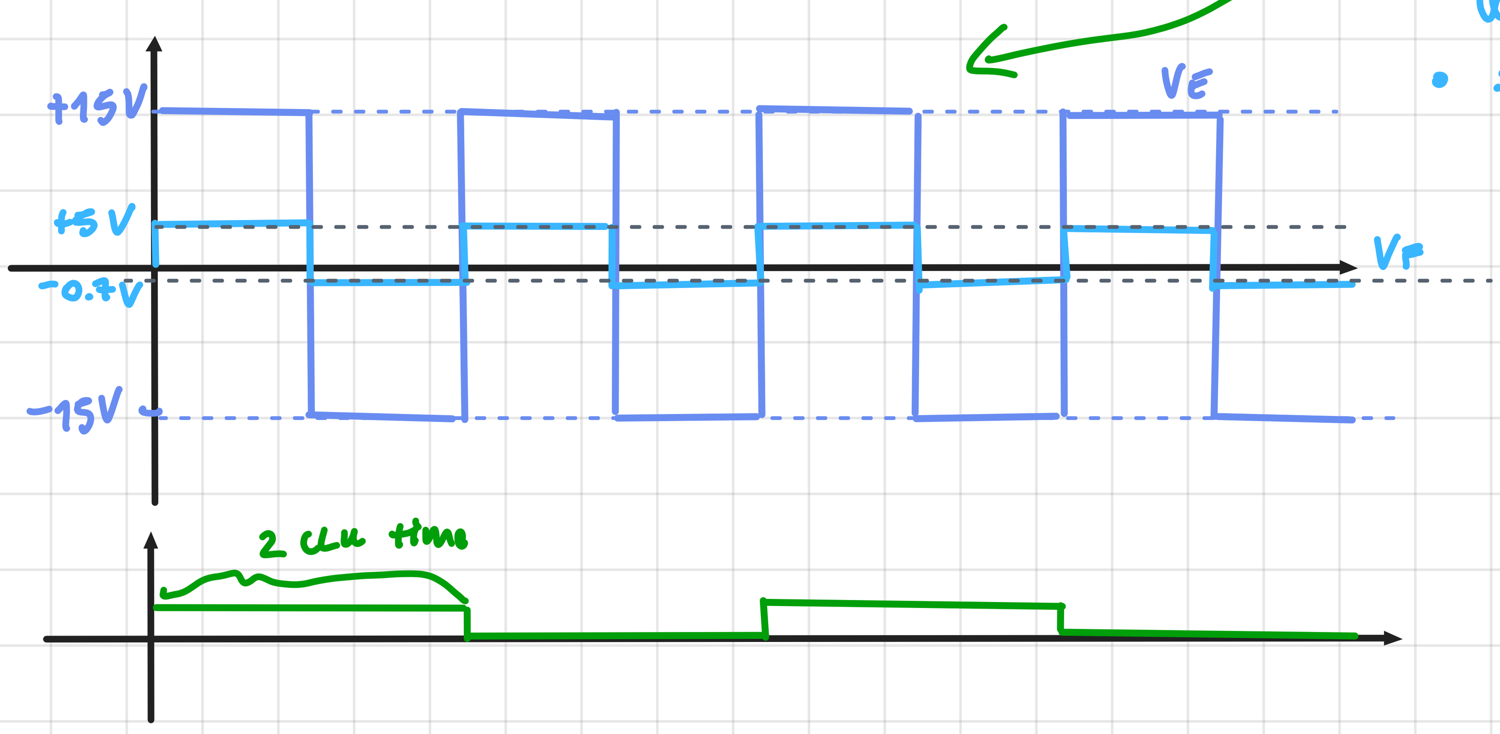


- rectifies it at 5V when VE>0
- zener-diode OFF ↳ -0.7V

almost a digital wave → [0,5V]

actually -0.7V

use it as CLK for the flip-flop



19/12/2022

EXO 9_EXAMS

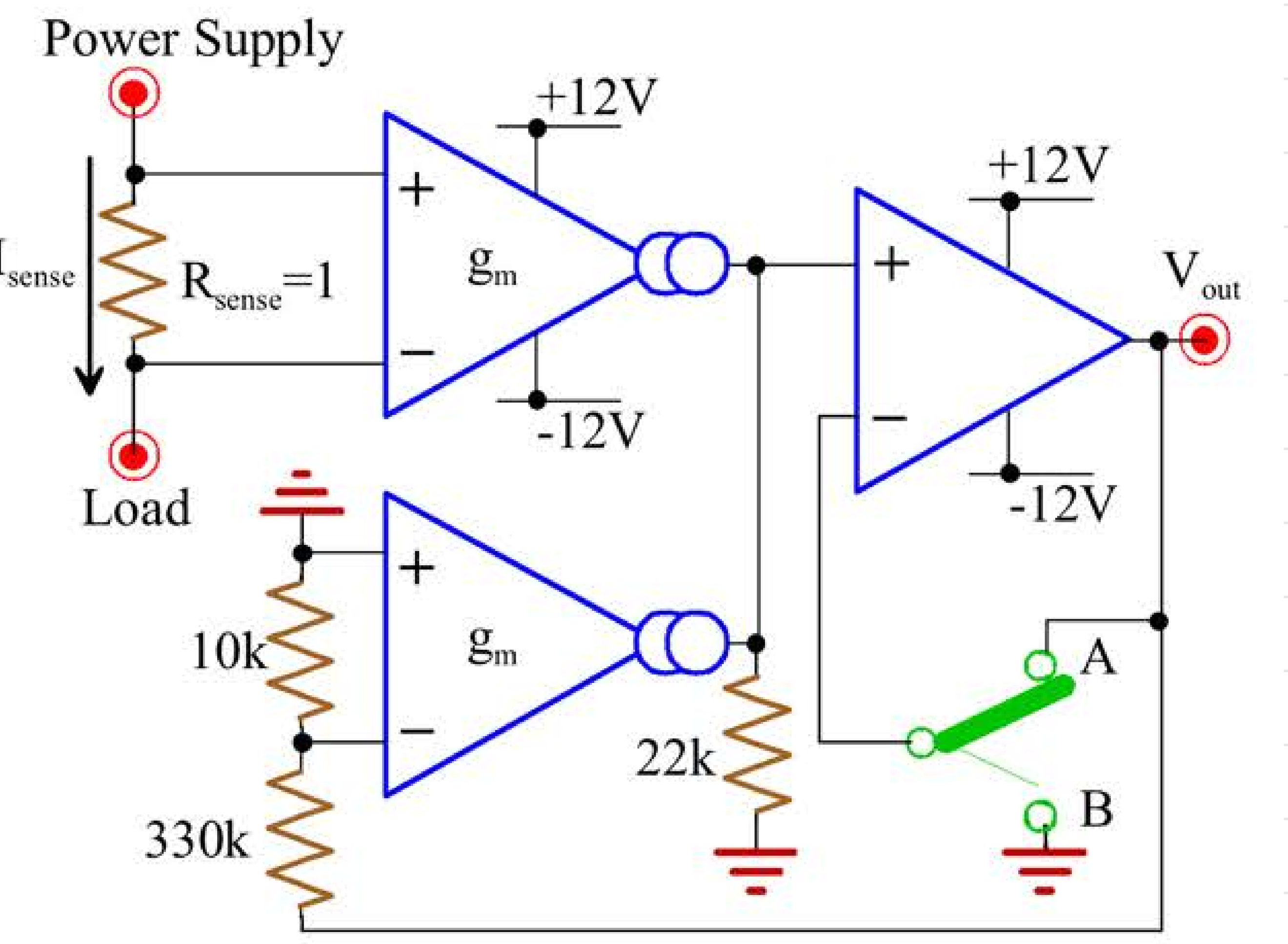
1 From 28/06/2007

Es. 1

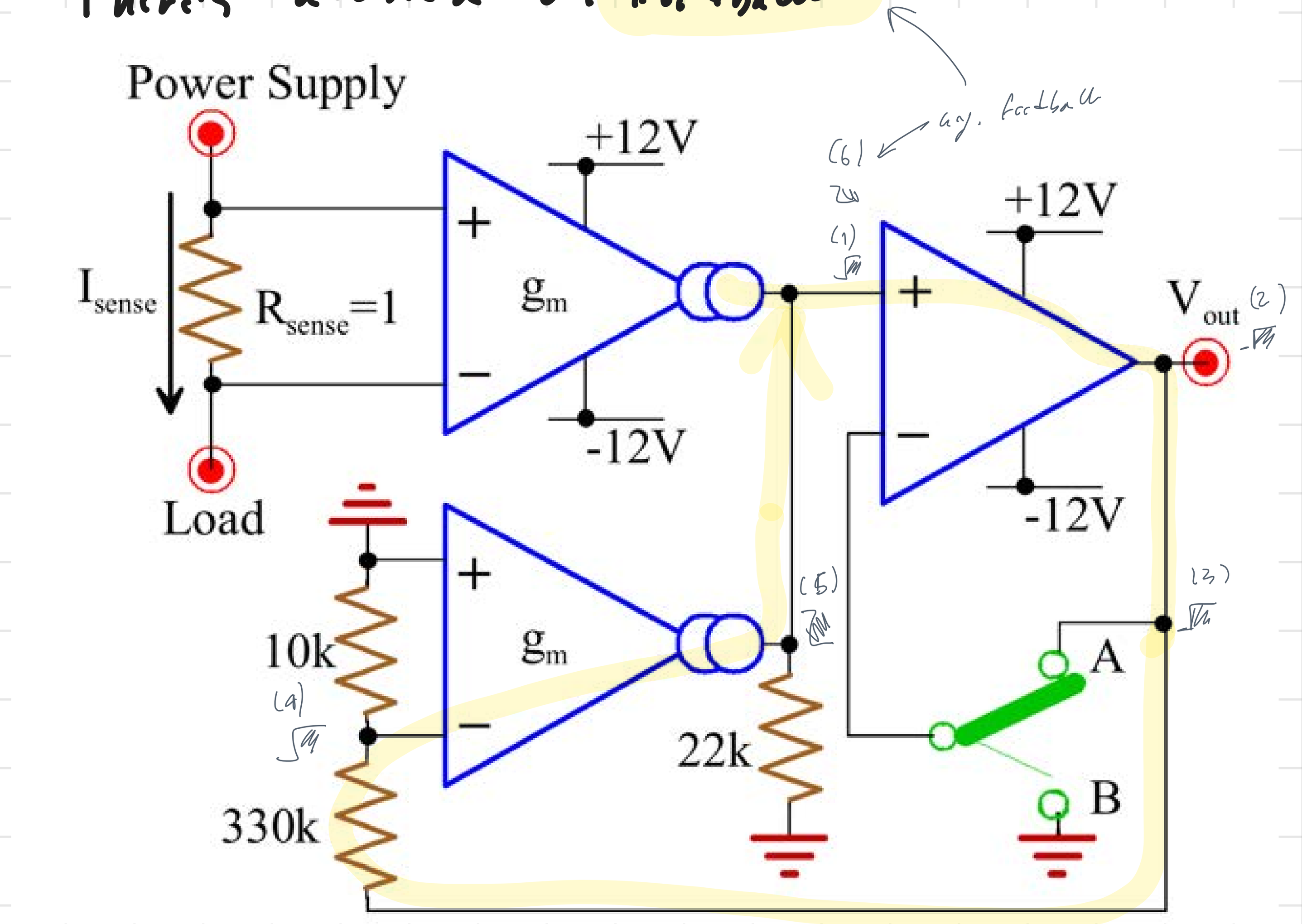
Il circuito impiega due OTA aventi transconduttanza g_m=1mA/V e monitora la corrente in una R_{sense}=1Ω.

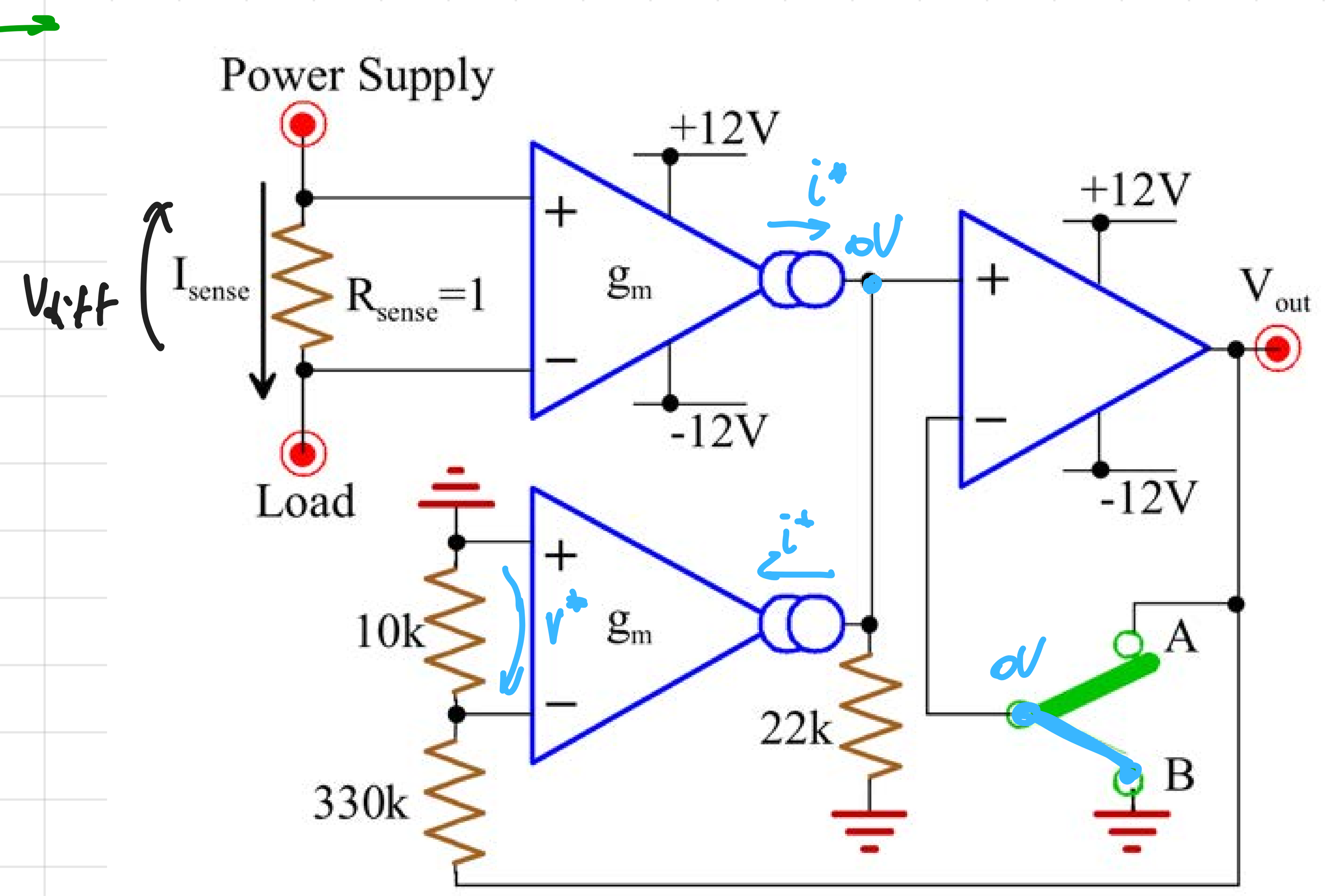
a) Quando l'interruttore è in posizione B, determinare la funzione del circuito ed il legame tra V_{out} e I_{sense}.

b) Quando l'interruttore è in A, dire **quantitativamente** cosa cambia rispetto al caso precedente.



There's a kinda of feedback





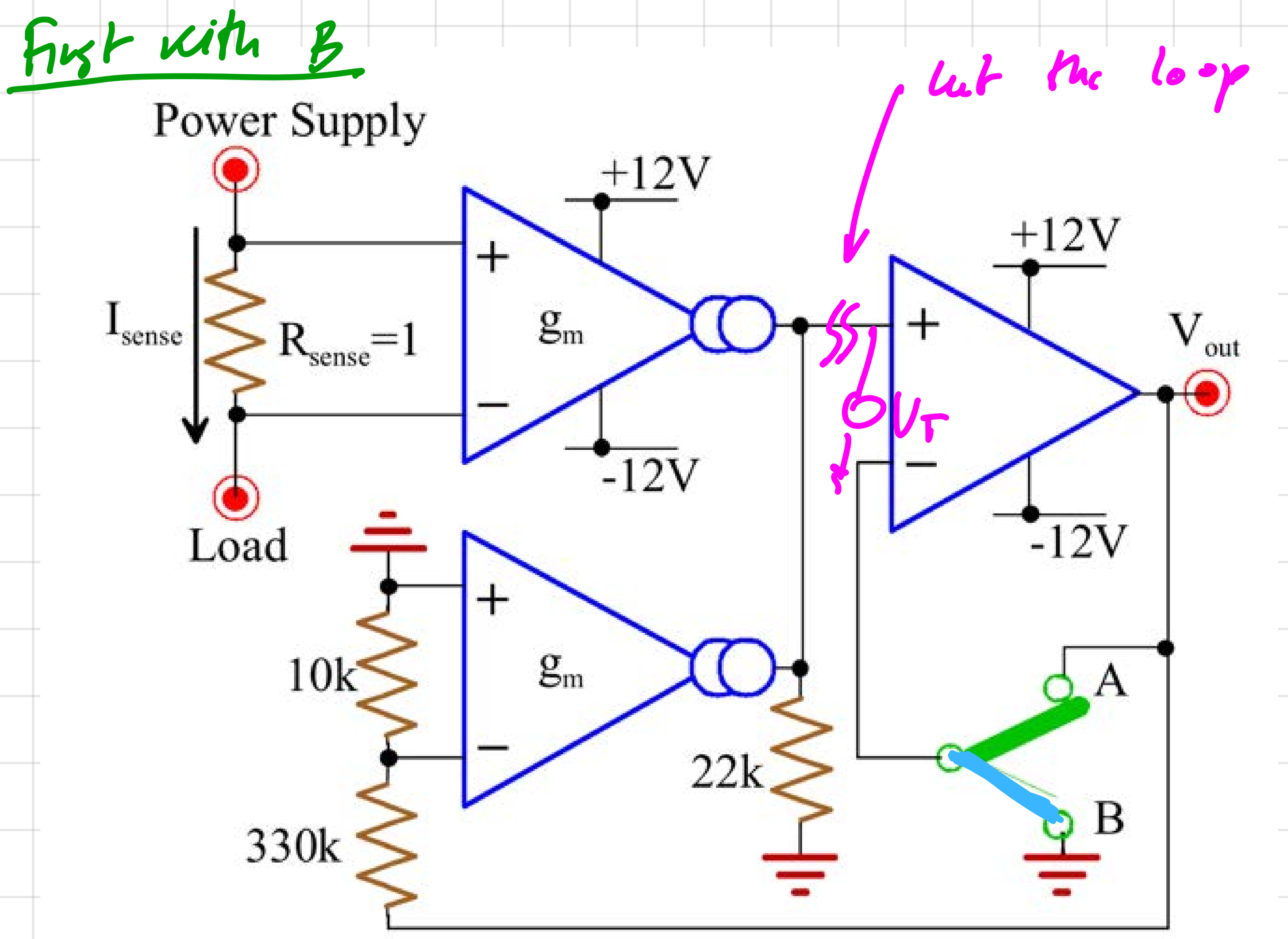
a)

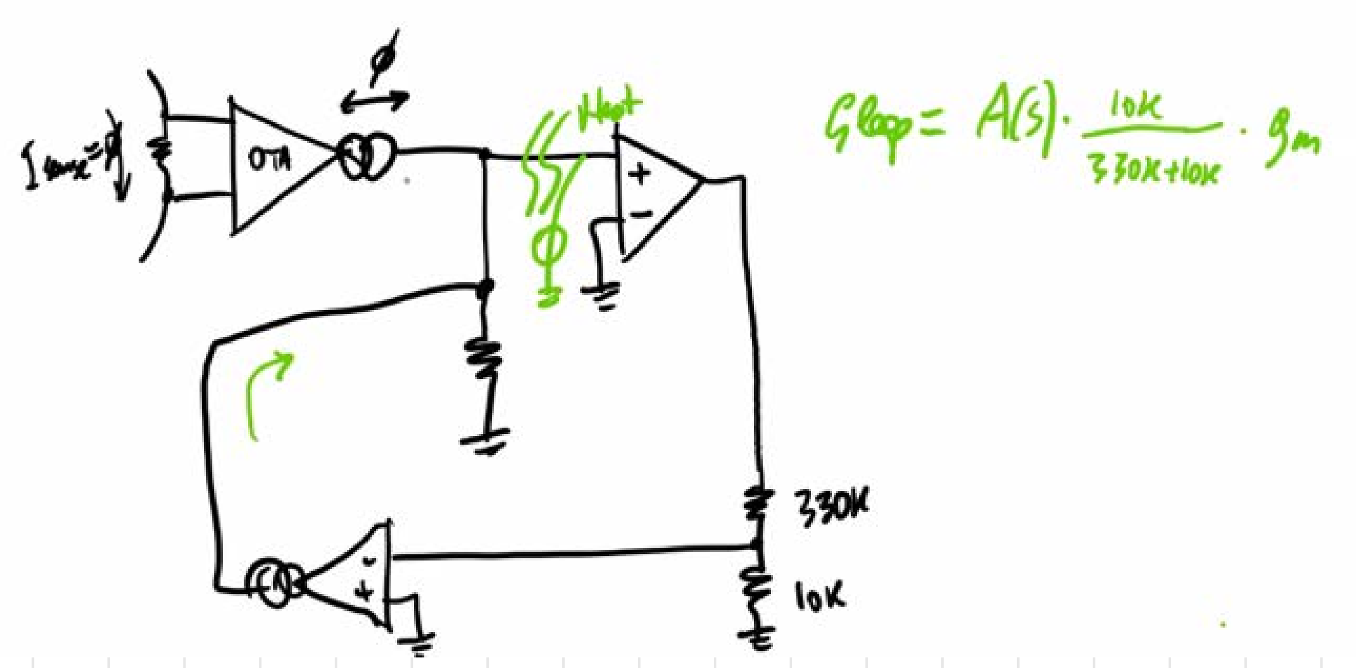
$$i^+ = V_{diff} \cdot g_m = I_{sense} \cdot R_{sense} \cdot g_m = I_{sense} \cdot 1 \cdot 1\,\frac{mA}{V}$$

$$i^* = V^+ \cdot g_m \longrightarrow V^+ = I_{sense} \cdot 1\,\Omega \longrightarrow V_{out} = \frac{V^+}{10k}\,(10k + 330k)$$

$$V_{out} = I_{sense} \cdot 1\,\Omega \left(1 + \frac{330k}{10k}\right) = I_{sense} \cdot 1\,\Omega \cdot 34$$

b) First with B



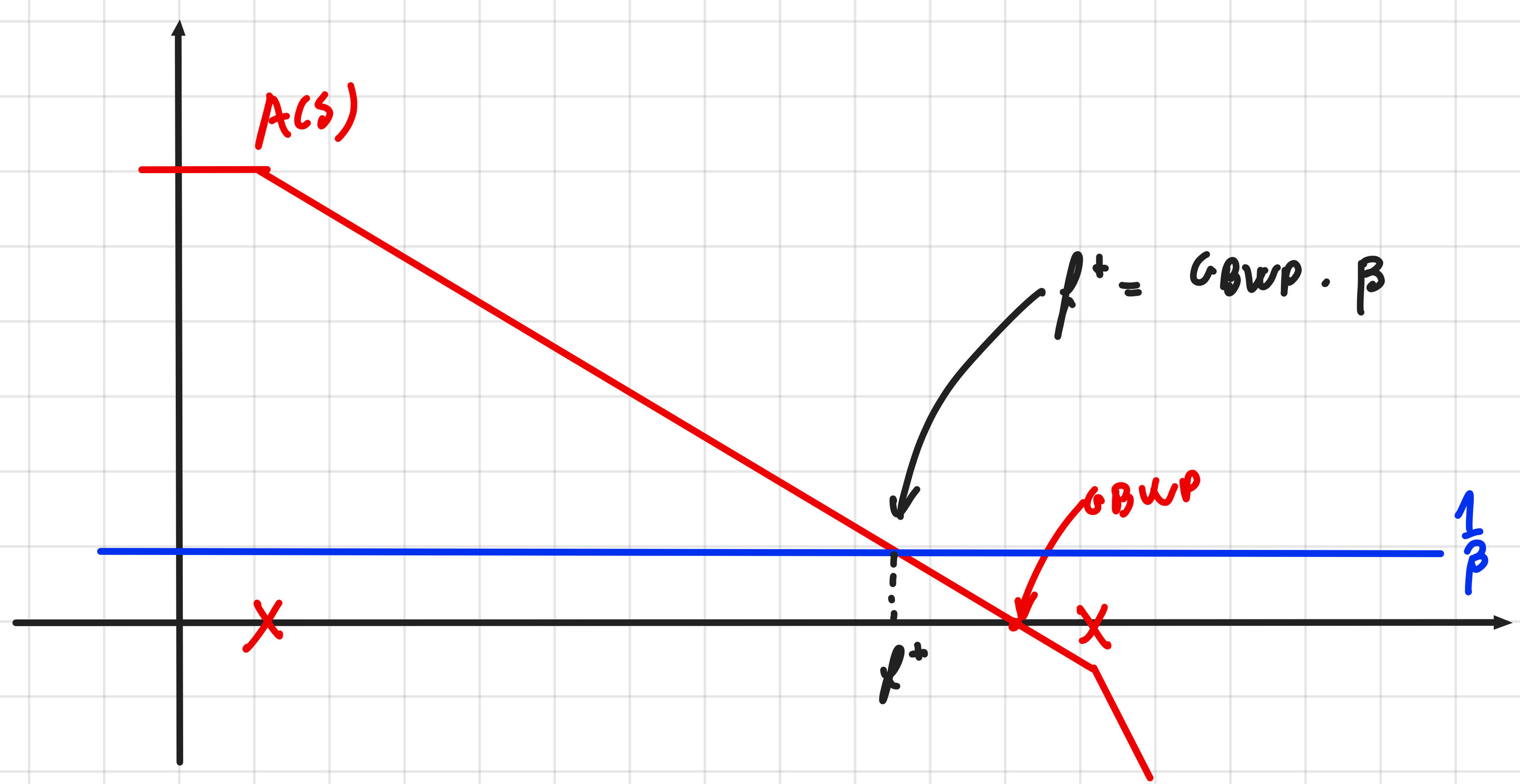


$$G_{loop} = A(s) \cdot \frac{10k}{330k+10k} \cdot g_m$$

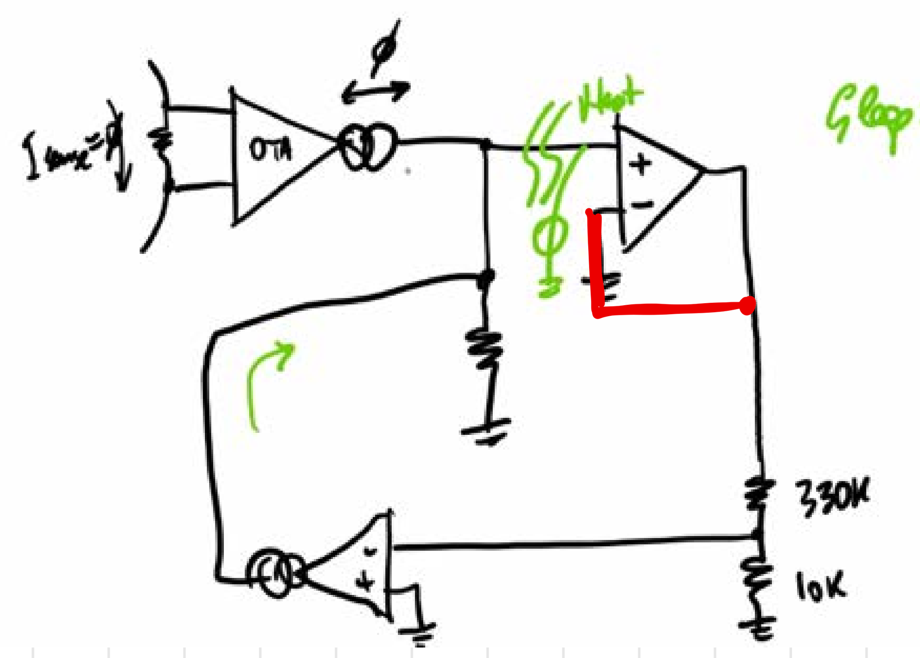
$$G_{loop} = A(s) \cdot \underbrace{\frac{10}{340} \cdot 22k \cdot 1\,\frac{mA}{V}}_{0.65 = \beta}$$

$$\beta \longrightarrow \frac{1}{\beta} = \frac{1}{0.65} = 1.5$$

Bode



- **Now consider A connected**



$\cancel{G_{loop} = A(s) \cdot \frac{10k}{330k + 10k} \cdot g_m}$

$$G_{loop} = 1 \cdot \frac{10k}{330k + 10k} \cdot g_m \cdot 22k = 0.65$$

$V_{out,id} = I_{sense} \cdot 34\,\Omega$

$$G_{real} = \frac{V_{out}}{I_{sense}}(F) = \frac{G_{ideal}}{1 - \frac{1}{G_{loop}}} = \frac{34\,\frac{V}{A}}{1 + \frac{1}{0.65}} = \frac{34\,\frac{V}{A}}{1 + 1.5} = 13.6\,\frac{V}{A}$$

Es. 3

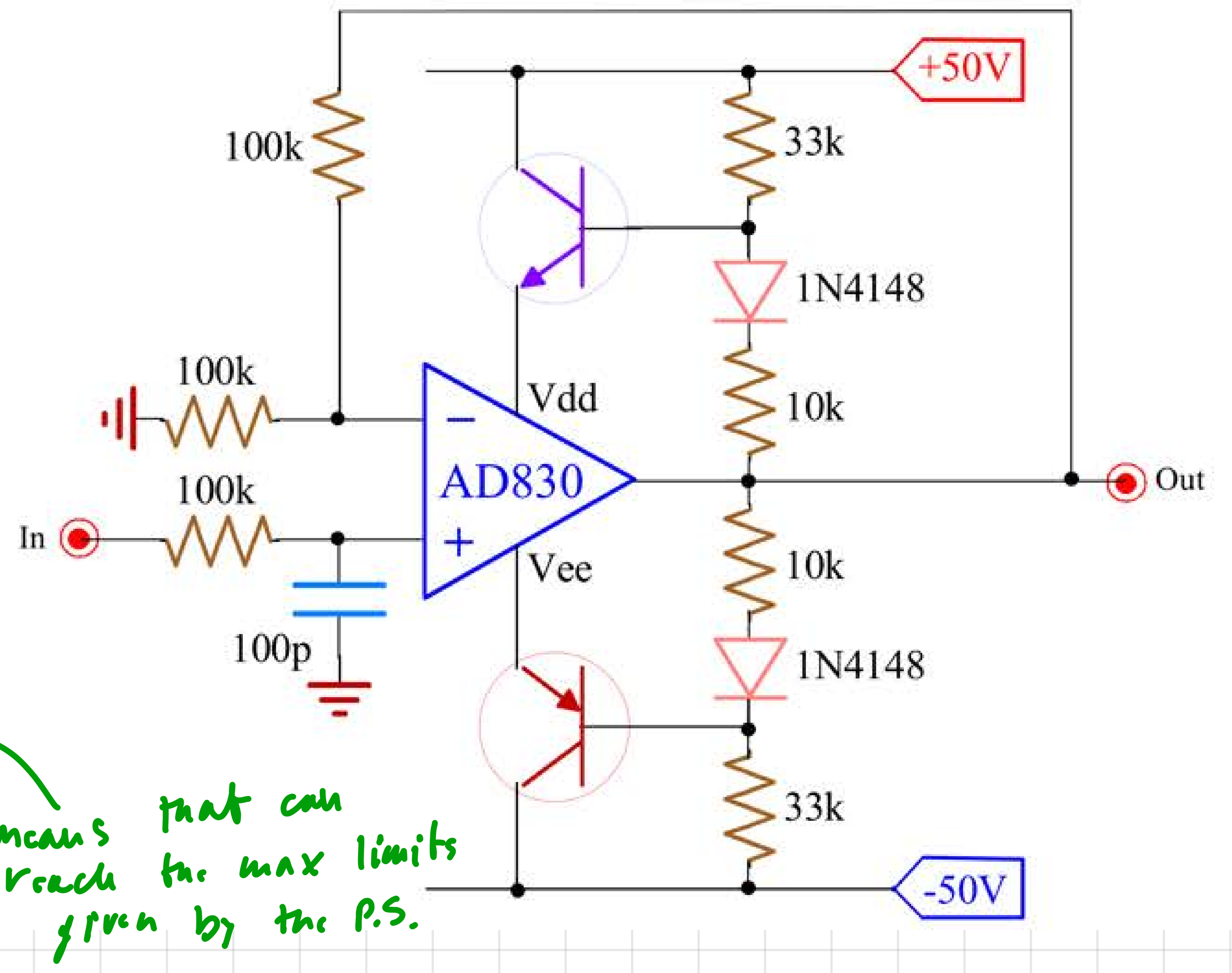
Usando un OpAmp con $V_{supply,max}=\pm 14V$, per potere erogare in uscita delle tensioni tra $\pm 50V$, ossia oltre i ***maximum absolute ratings***, si impiega il bootstrap.

a) Determinare la tensione di alimentazione $V_{dd}-V_{ee}$ dell'OpAmp e disegnare l'andamento di V_{out}, V_{dd} e V_{ee} quando $V_{in}=10V$ sinusoidali.

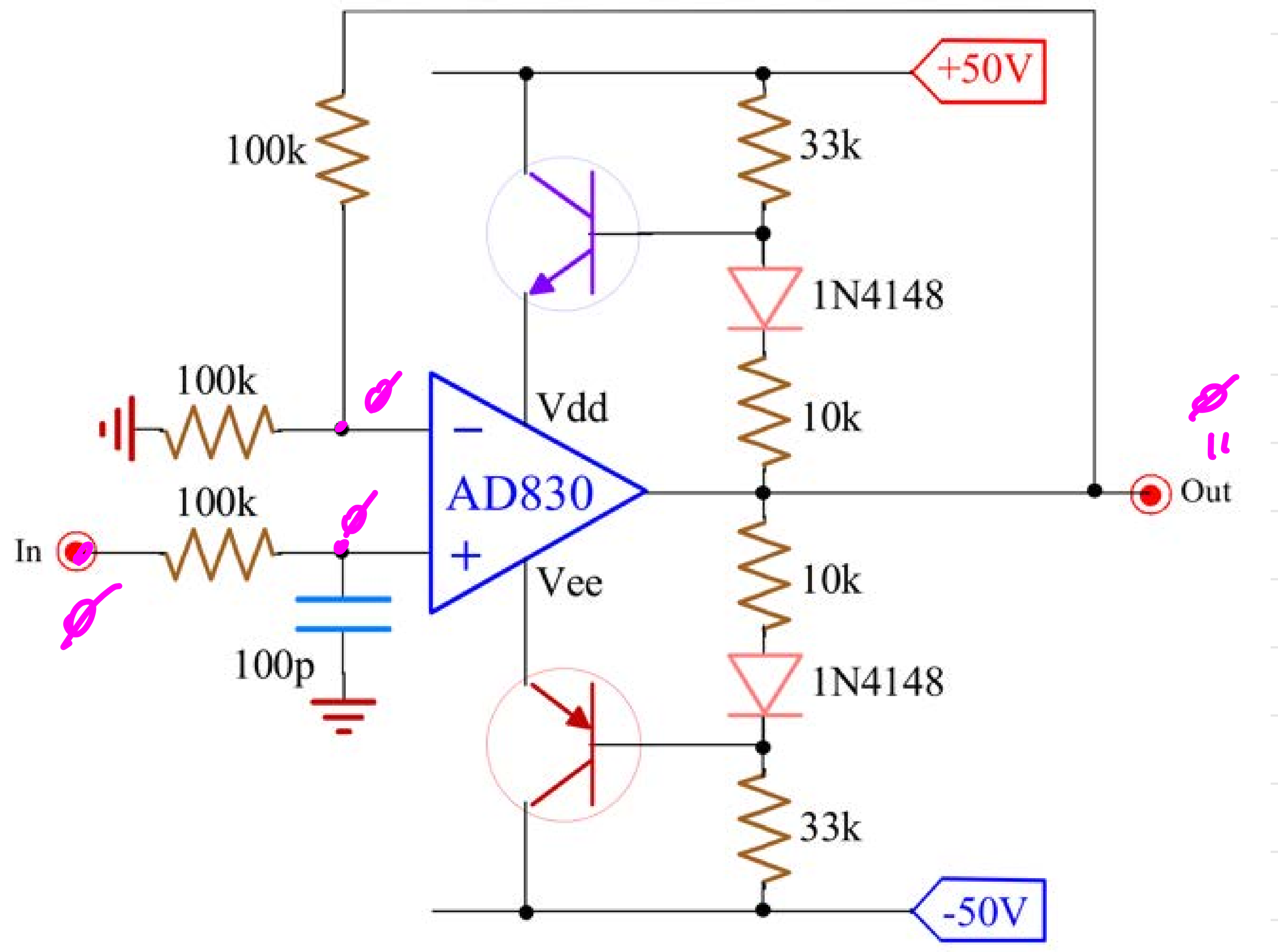
b) Determinare il massimo guadagno dello stadio, oltre il quale si eccede il common mode input voltage range dell'OpAmp, sapendo che è un *rail-to-rail* sia come *input common range* che come *output voltage swing*.

means that can reach the max limits given by the P.S.

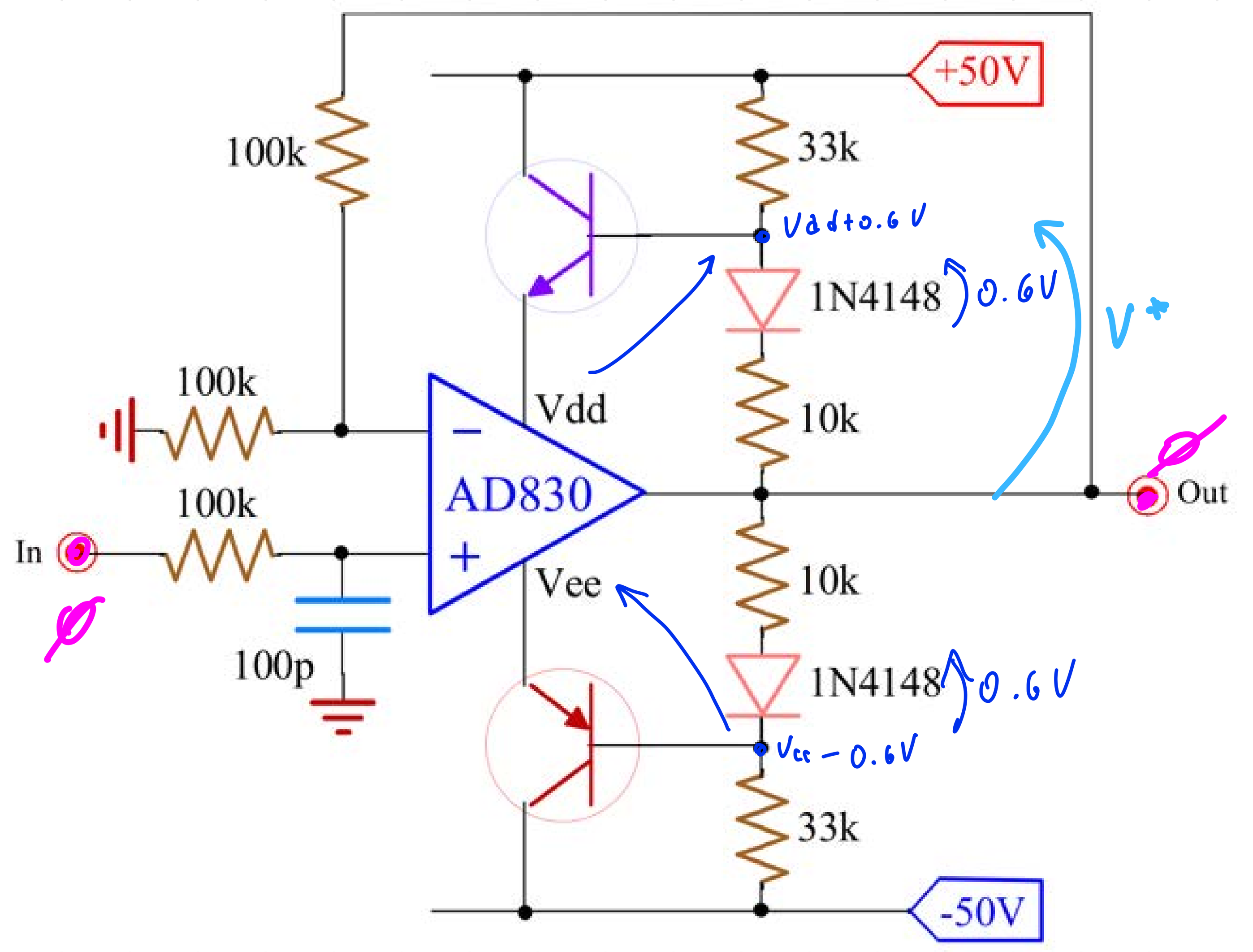
In this case both input and output



It has a negative feed. → Let's first apply $In = \emptyset$ → $Out = \emptyset$



→ Let's now consider the different components

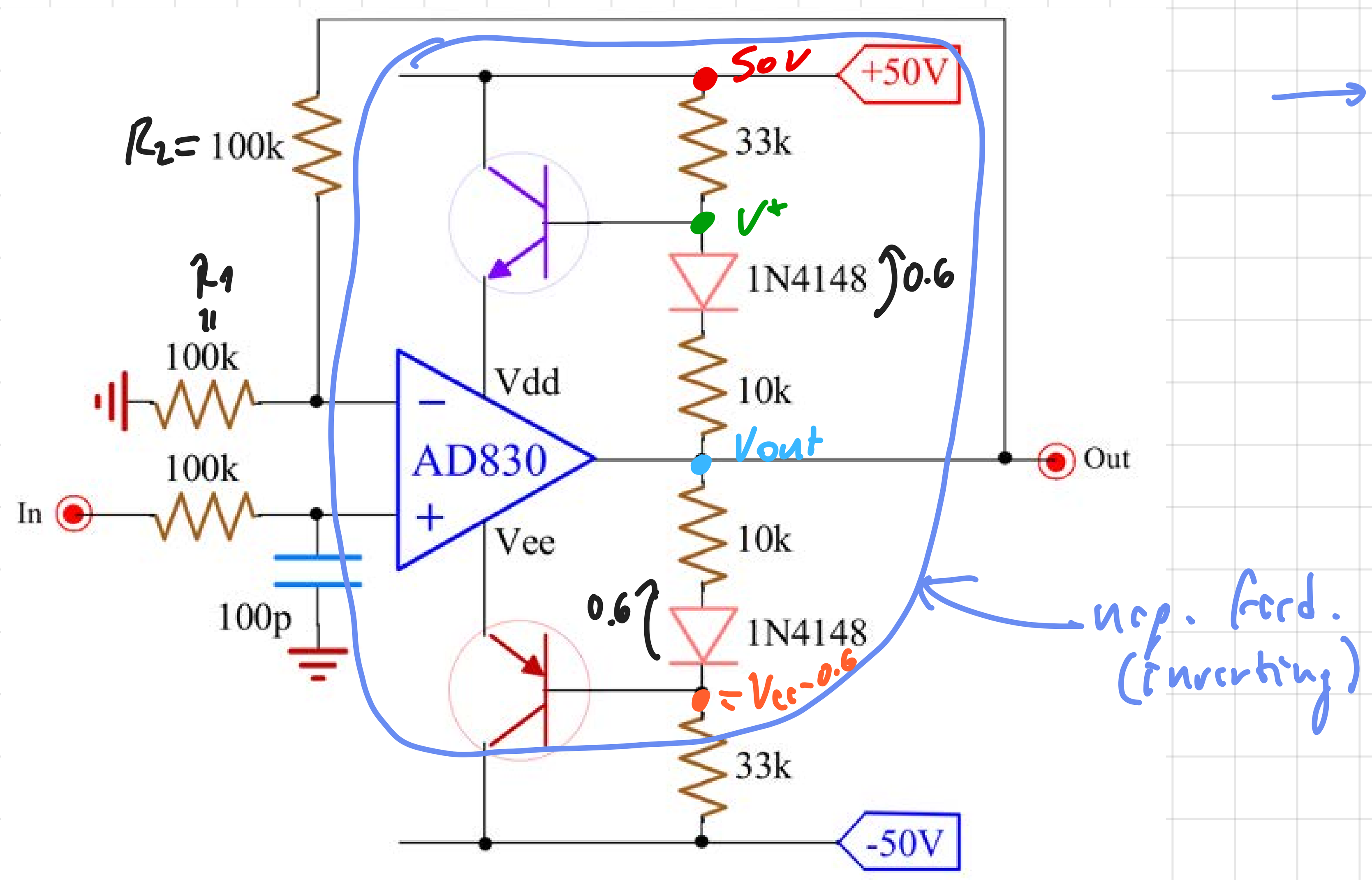


$$V^+ = (50V - 0.6V)\cdot\frac{10k}{10k+33k} + 0.6V \longrightarrow V_{dd} = V^+ - 0.6V = 49.4V\cdot\frac{10}{43} = 11.5V < 14 \text{ (max P.S.)}$$

same reasoning for V_{ee} ⟶ $V_{ee} = \dots = -11.5V < 14$ (max P.S.)

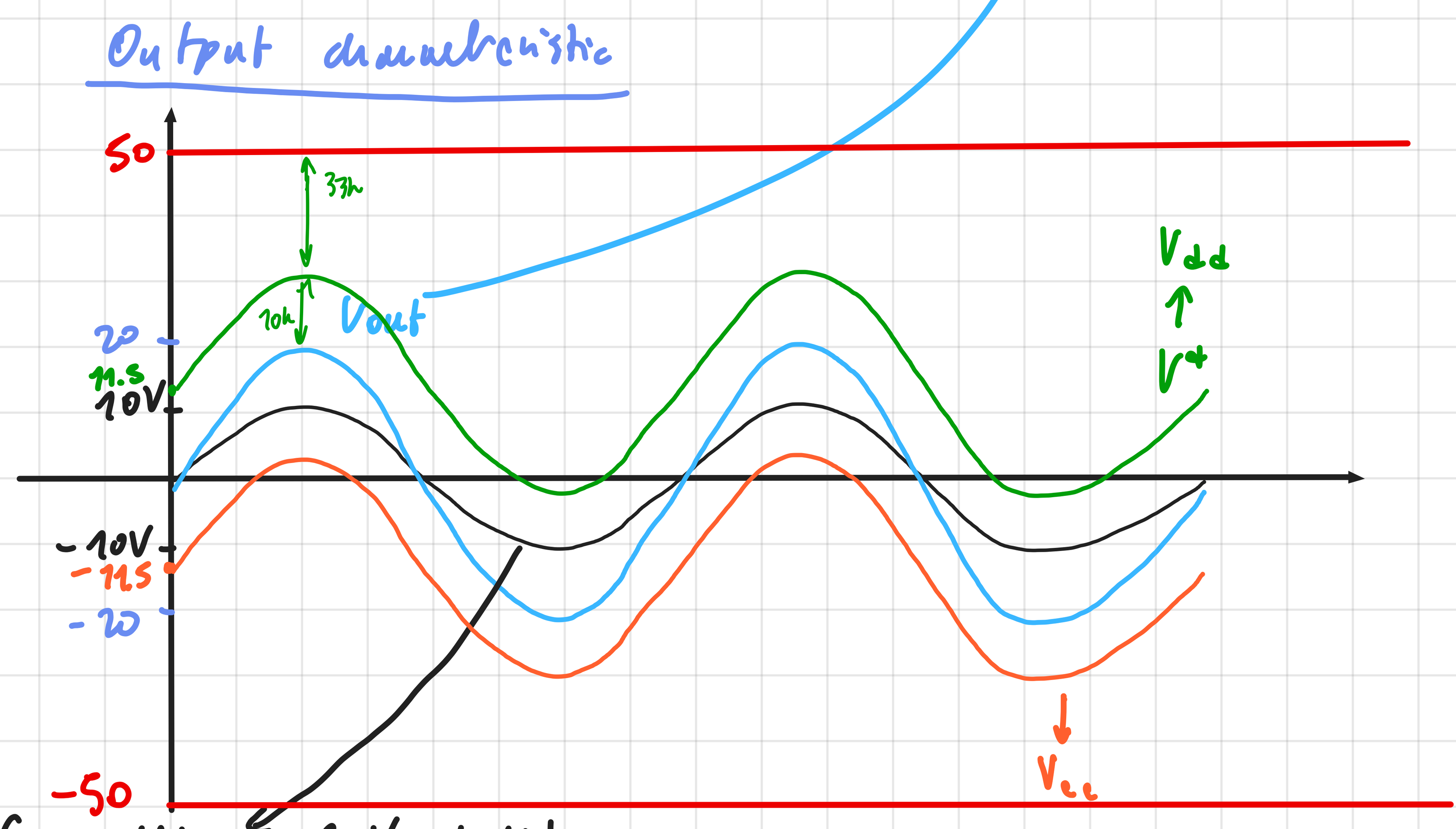
a)

Now what happens when $V_{in} \neq 0$



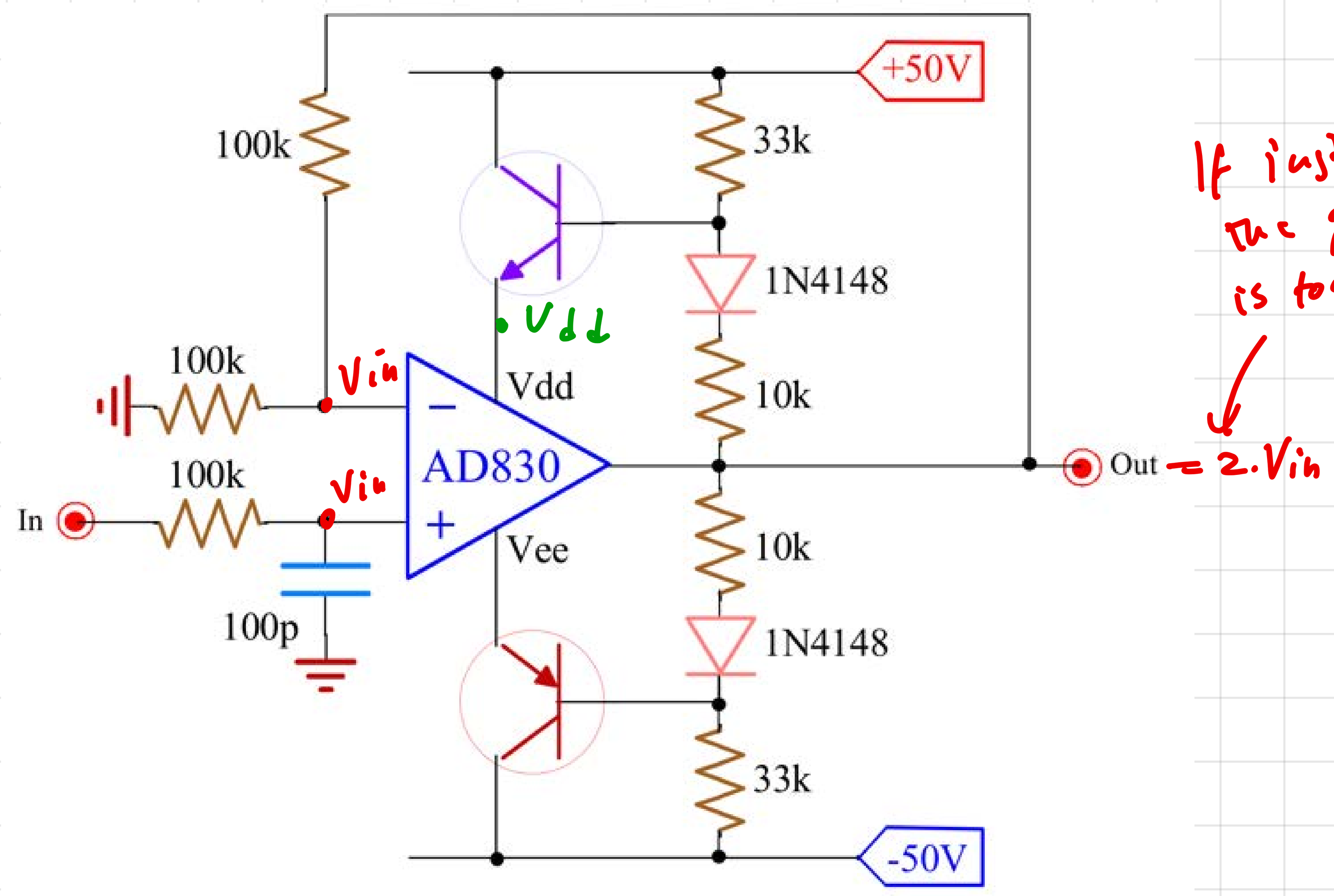
$$\text{Gain} = \frac{V_{out}}{V_{in}} = 1 + \frac{R_2}{R_1} = 1 + \frac{100k}{100k} = 2$$

$$\underbrace{V^+}_{V_{dd}+0.6V} = V_{out} + (\underbrace{V}_{50V} - \underbrace{V}_{V_{out}} - 0.6)\cdot\frac{10k}{43k}$$

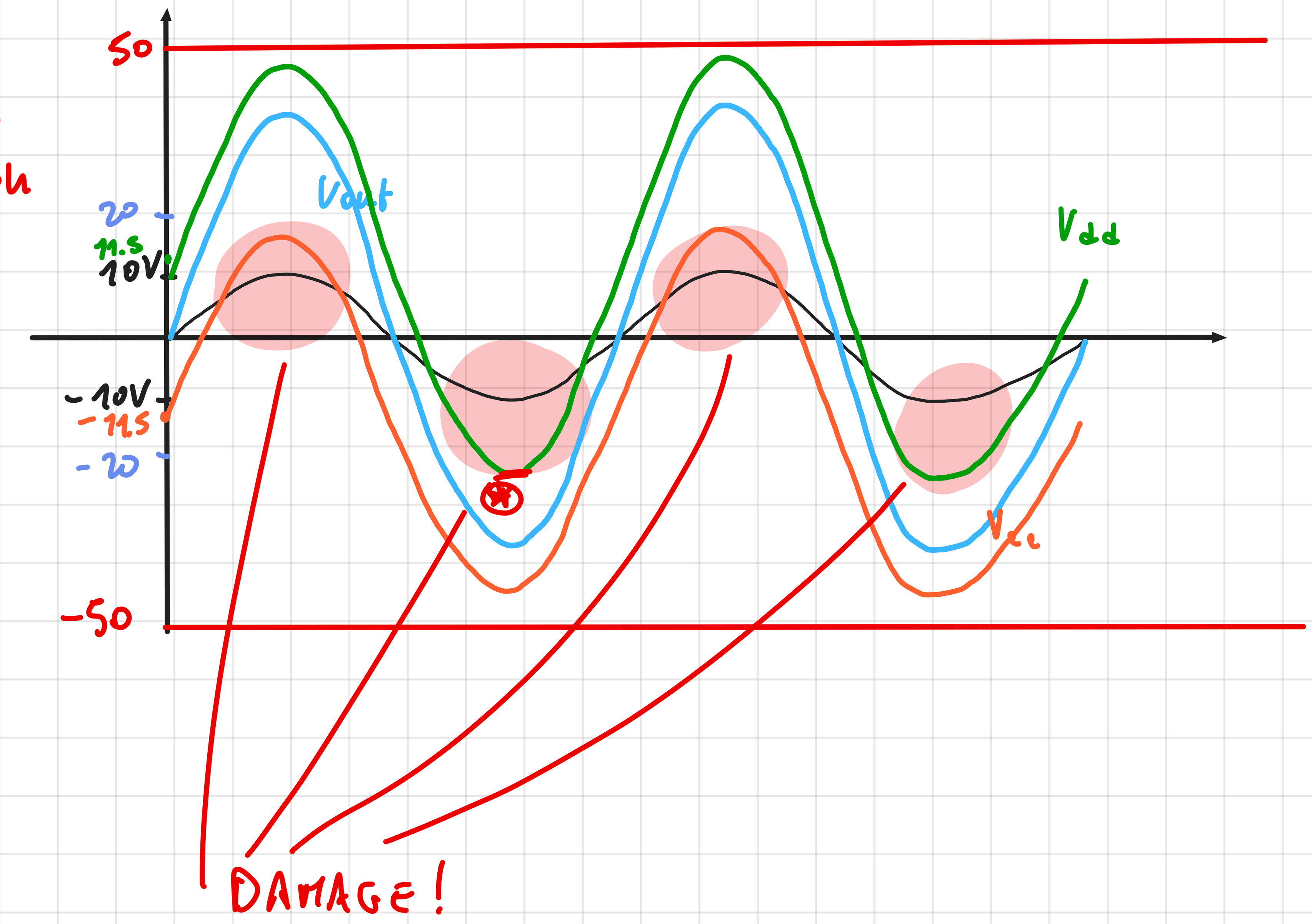


e.g. $V_{in} = 10V \sin(t)$

b)



If instead the gain is too high



↳ $V_{out} = G \cdot V_{in}$

$V_{dd} = (50 - G\cdot V_{in} - 0.6)\cdot \frac{10k}{43k} + G\cdot V_{in} \geq V_{in}$

↳ $49.4 - G\cdot V_{in} \geq V_{in}(1-G)4.3$ .... ⟶ G_{max} for wich we don't have damage

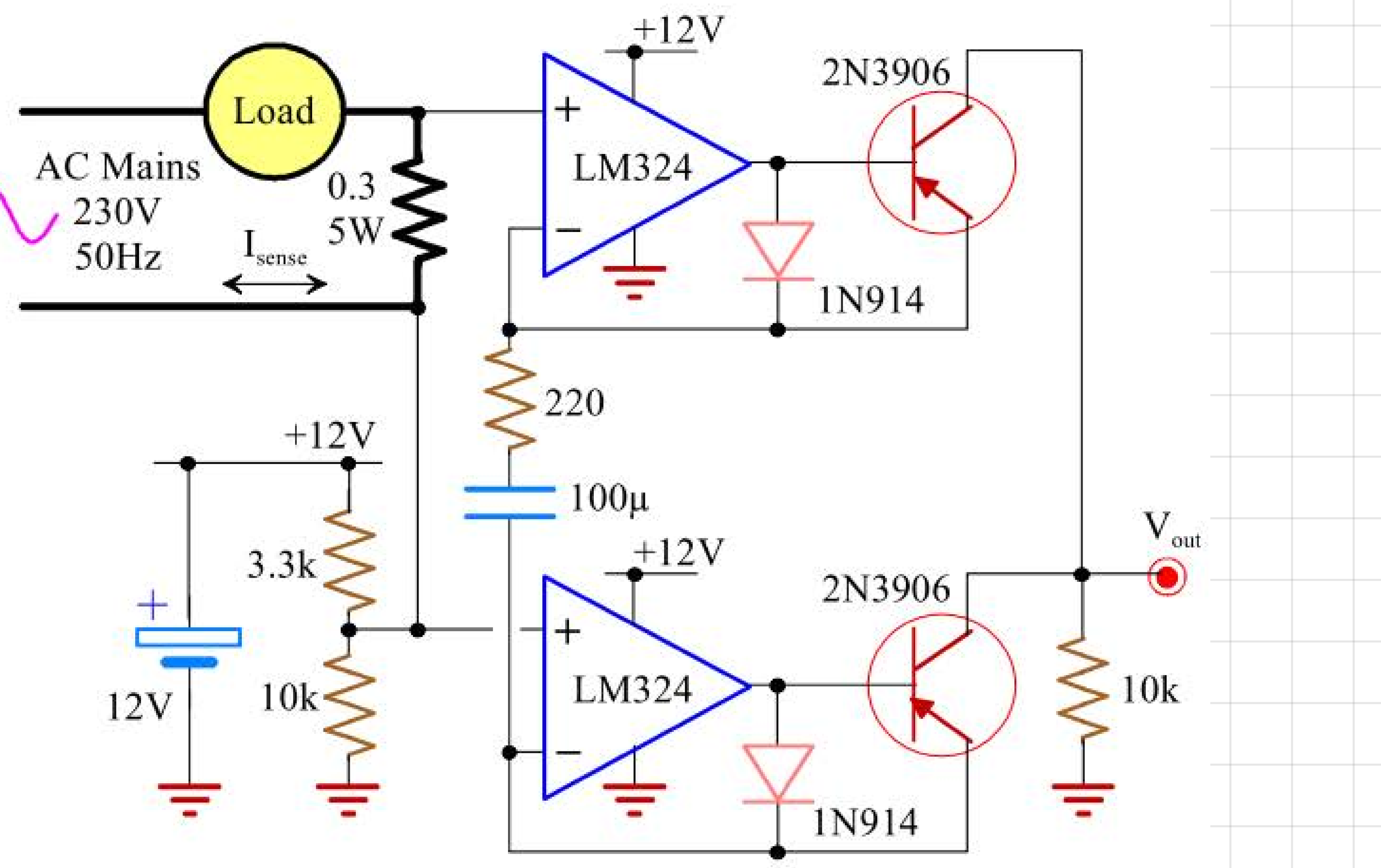
③ From 5/02/2008

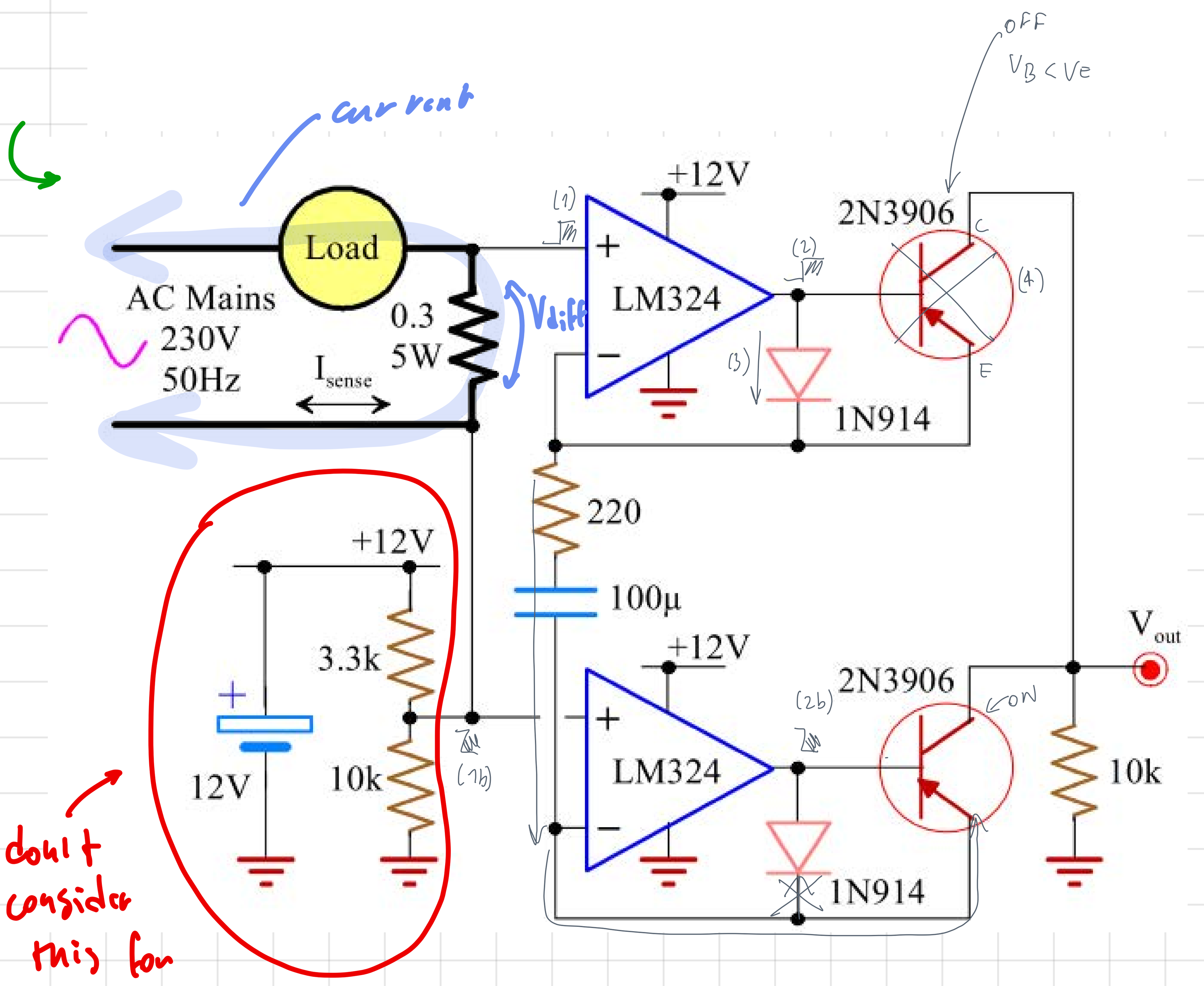
Es. 2

Il circuito monitora l'assorbimento di un carico in alternata a 50Hz. L'alimentazione è flottante a batteria.

a) Disegnare la forma d'onda quotata di V_{out} nel caso sia collegato un carico resistivo di 50W e determinare il guadagno V_{out}/I_{sense}.

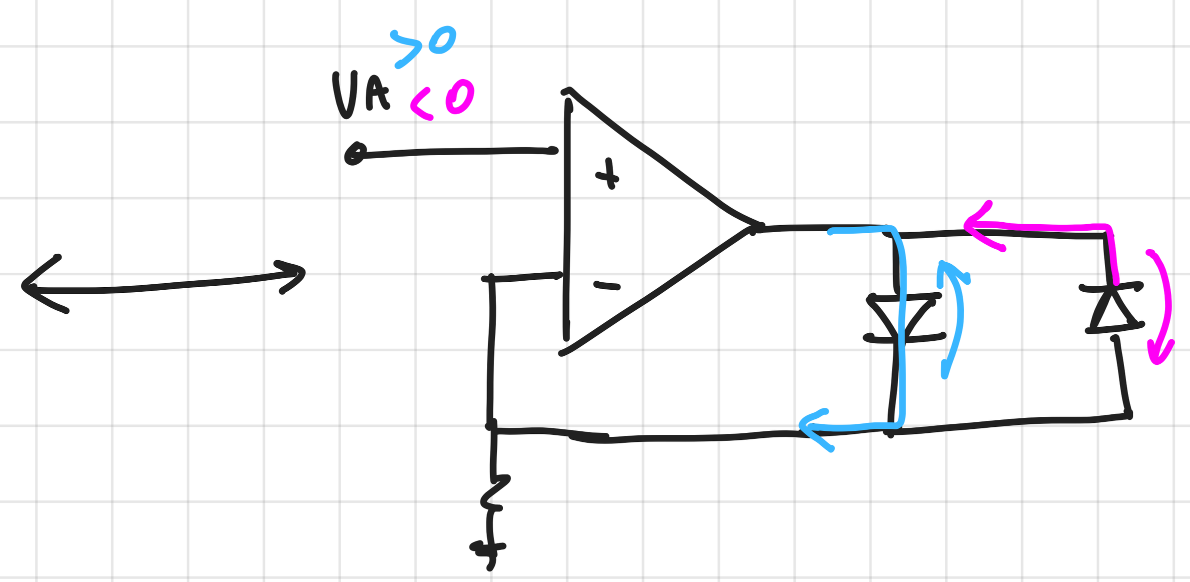
b) Realizzare l'alimentazione continua del circuito (circa 12V) partendo dalla tensione di rete, senza usare alcun trasformatore.





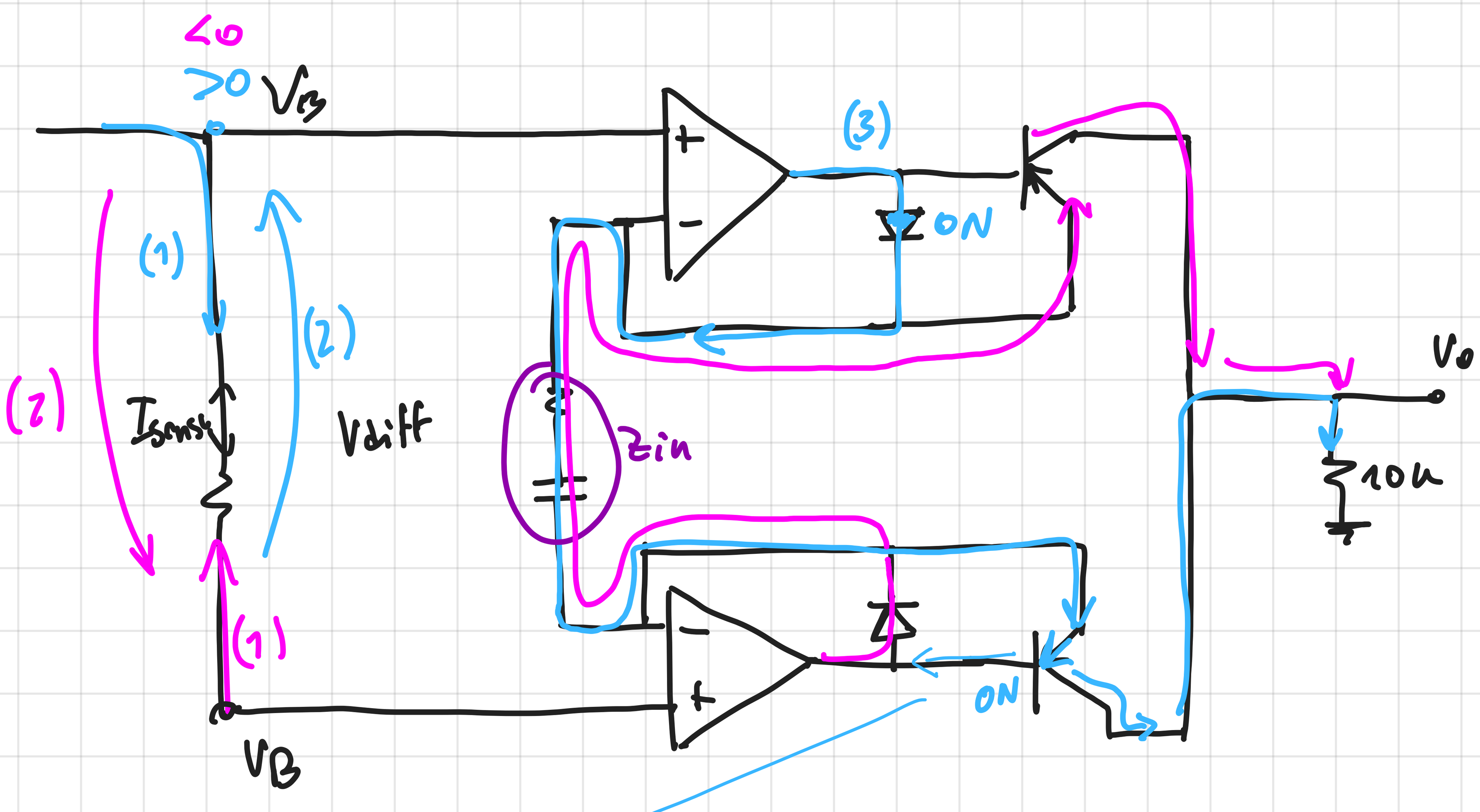
don't consider this for now

$\rightarrow V_{diff} = i \cdot 0.3\,\Omega$



↳ So we have

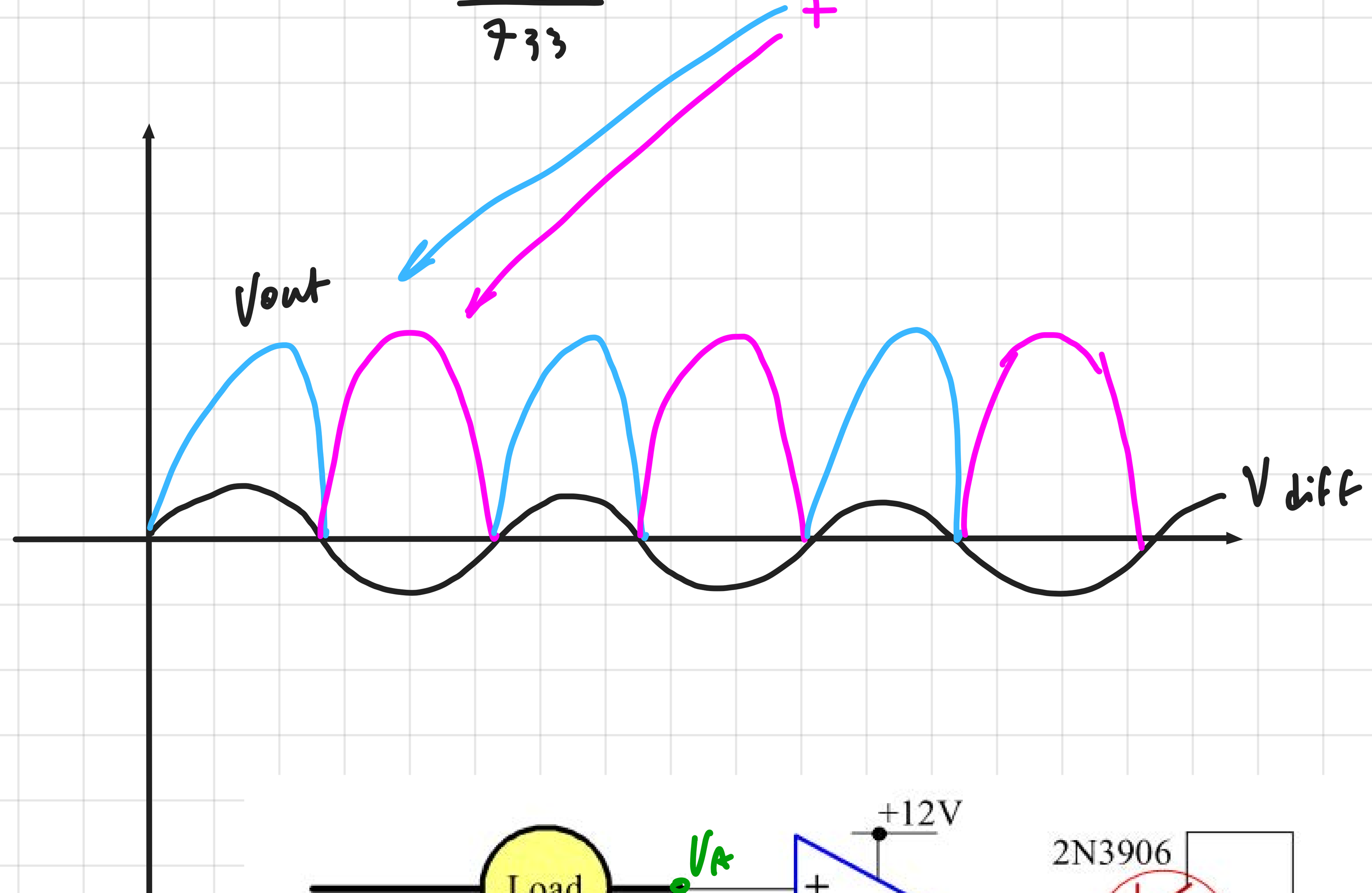
a)



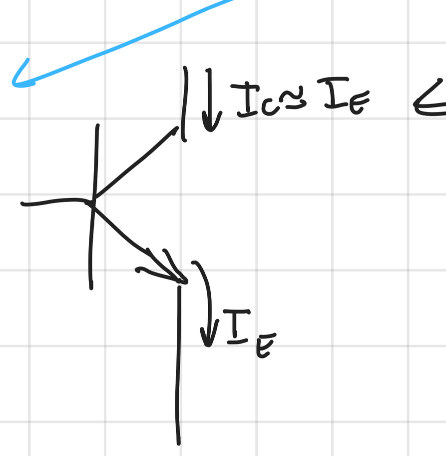
$V_{diff} = I_{sense} \cdot 0.3\,\Omega$

$i^* = \frac{V_{diff}}{Z_{in}} \simeq \frac{V_{diff}}{R} = \frac{I_{sense} \cdot 0.3\,\Omega}{220\,\Omega} = \frac{i_{sense}}{733}$

$\hookrightarrow V_{out} = \frac{I_{sense}}{733} \cdot 10k = +I_{sense} \cdot 13.6$

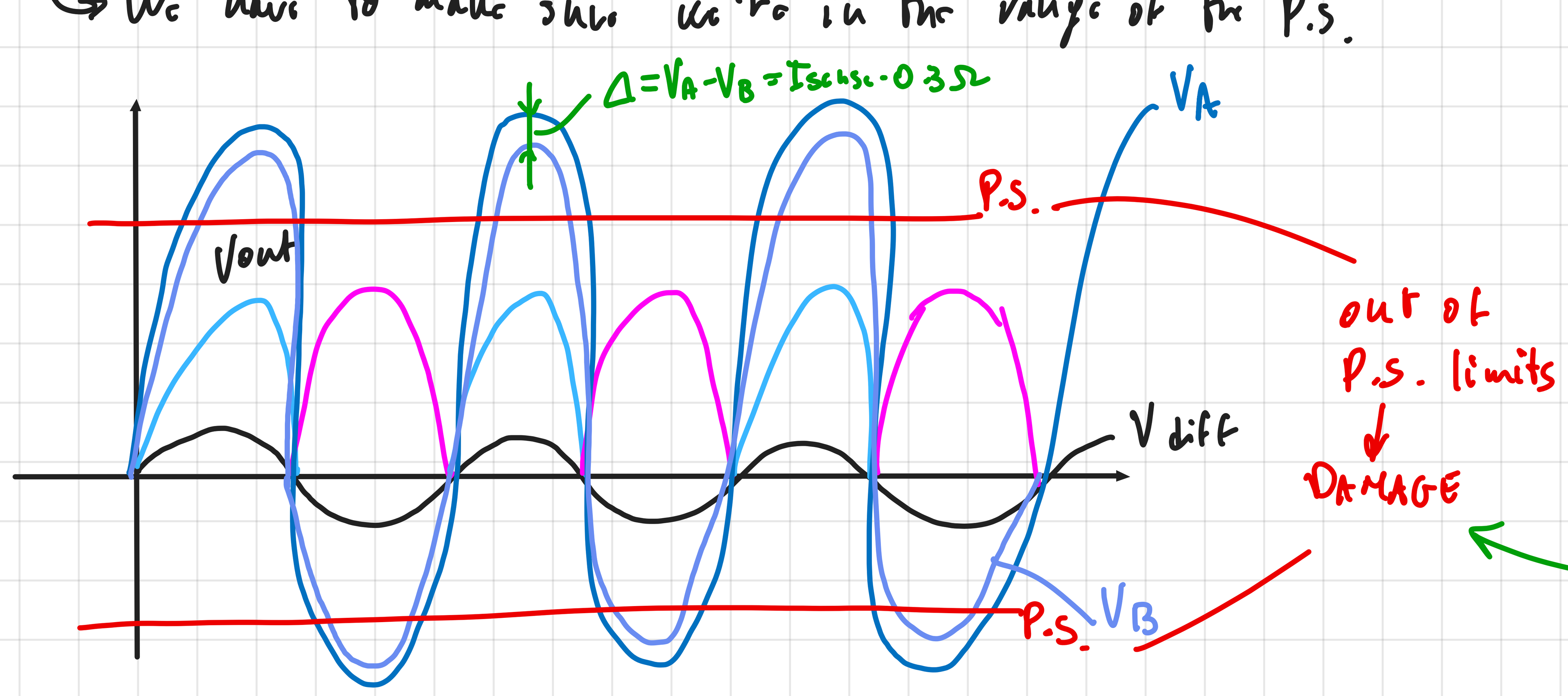


Note:



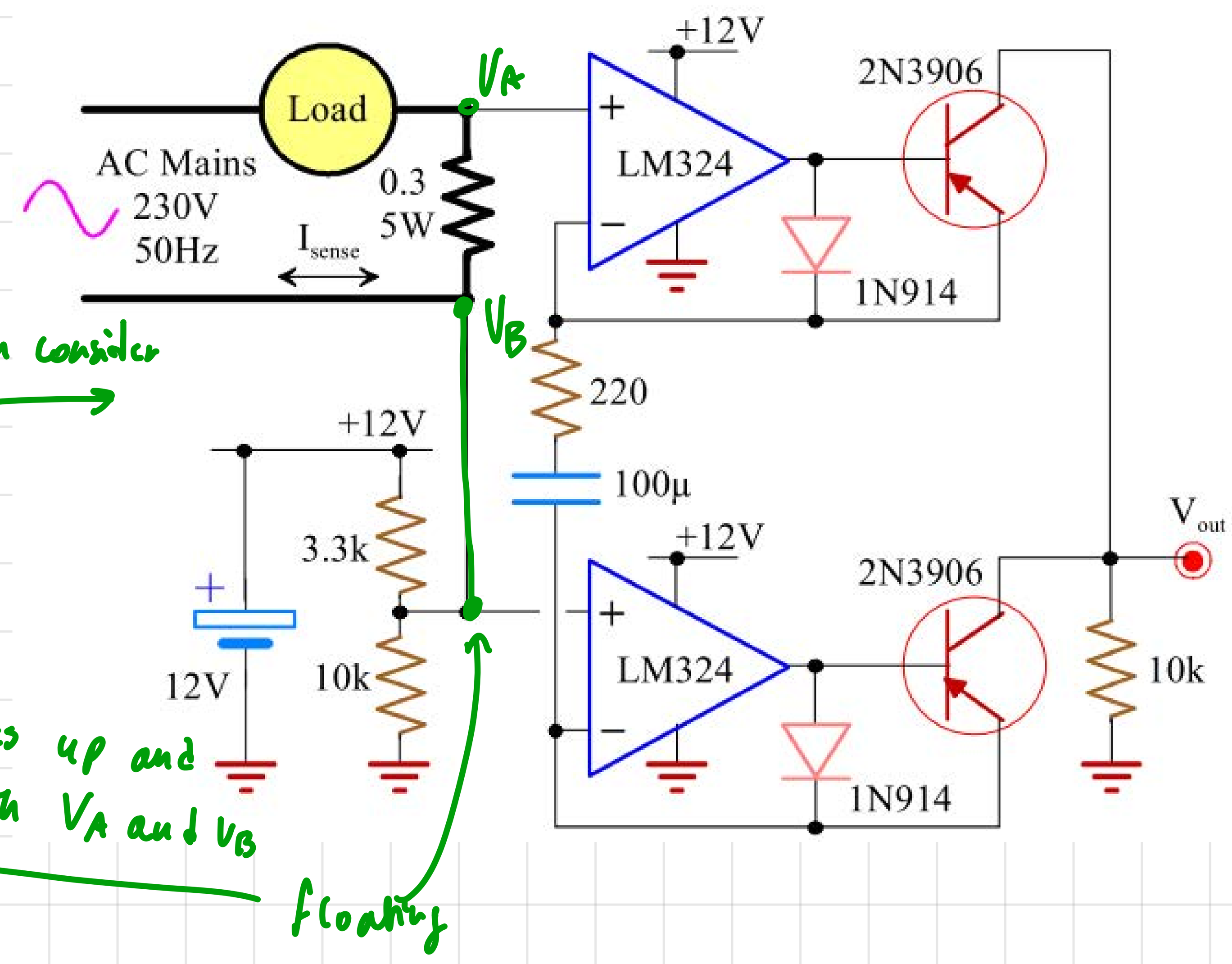
← basically all the currents goes to the collector

b) ↳ We have to make sure we're in the range of the P.S.



out of P.S. limits → DAMAGE

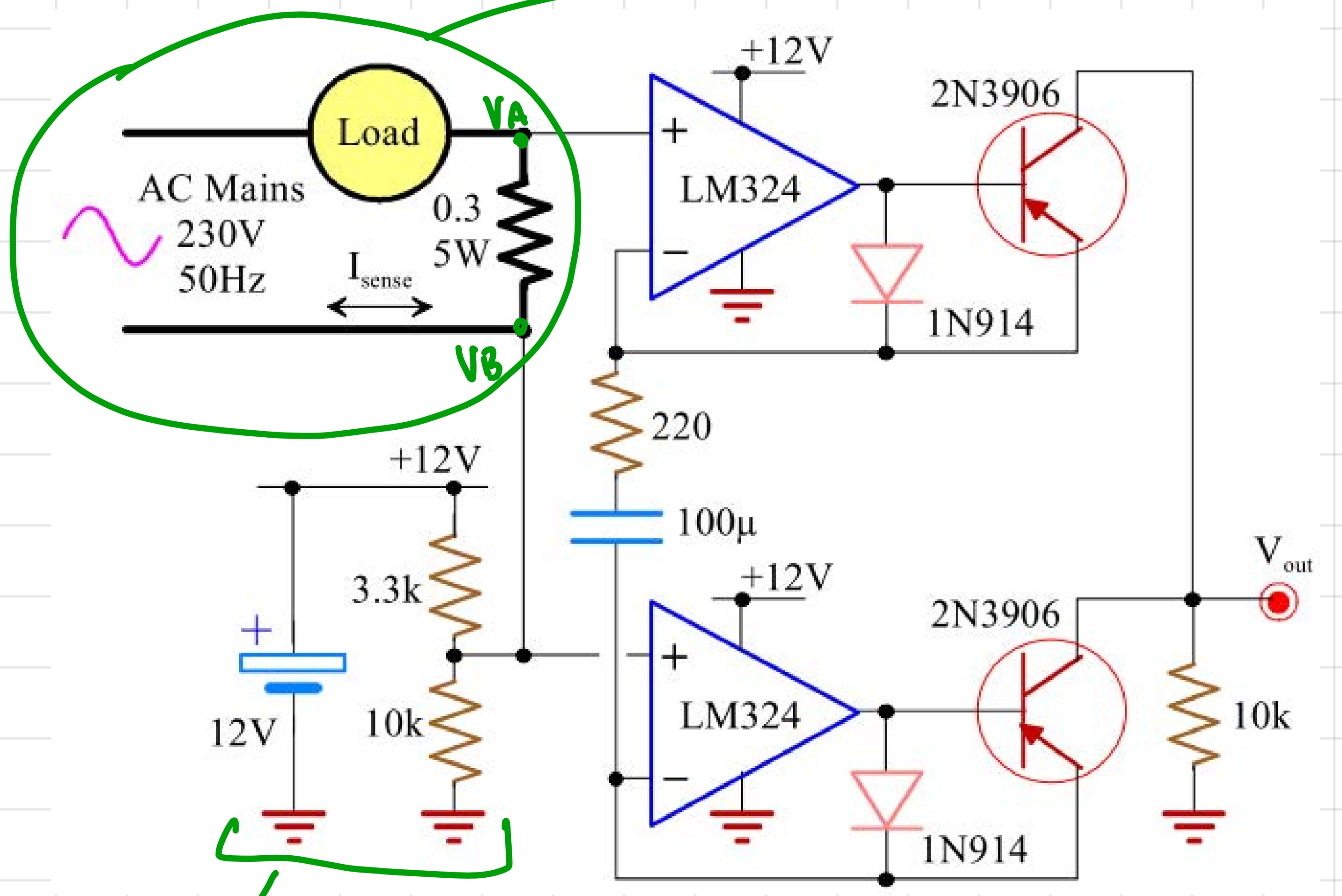
we can consider →

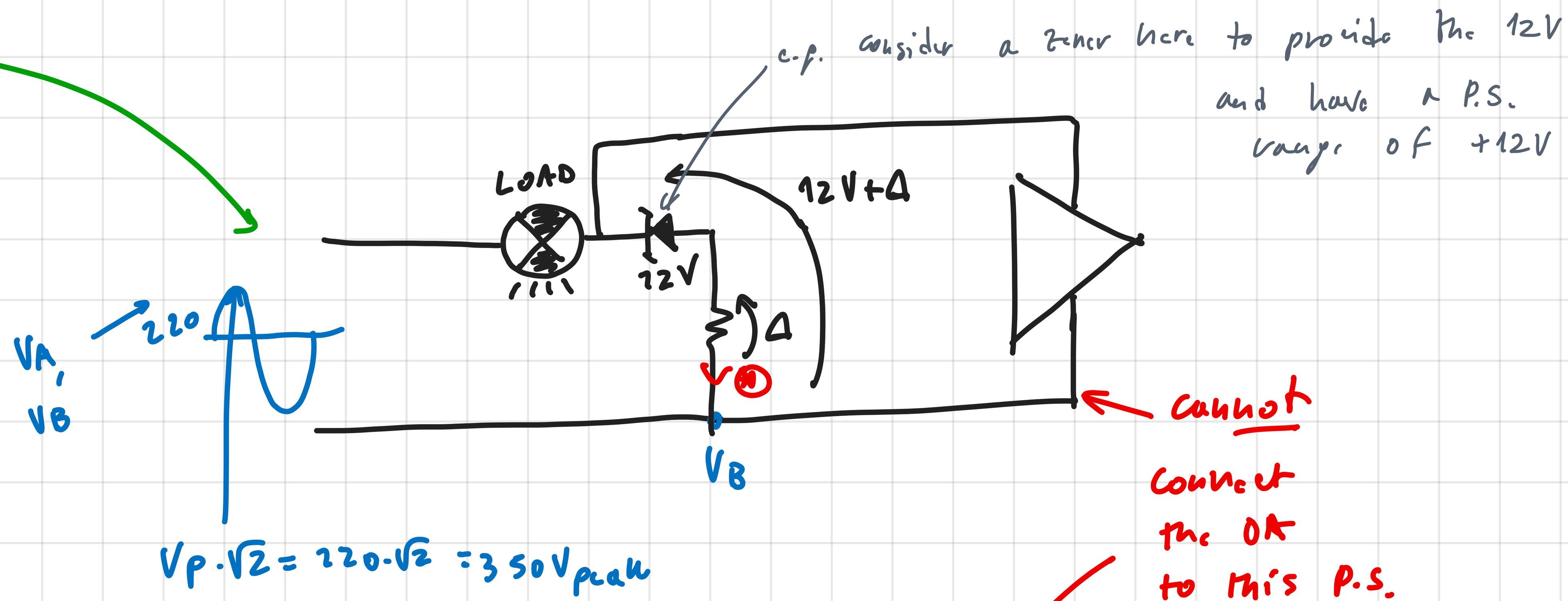


P.S. goes up and down with V_A and V_B

floating

Indeed consider:

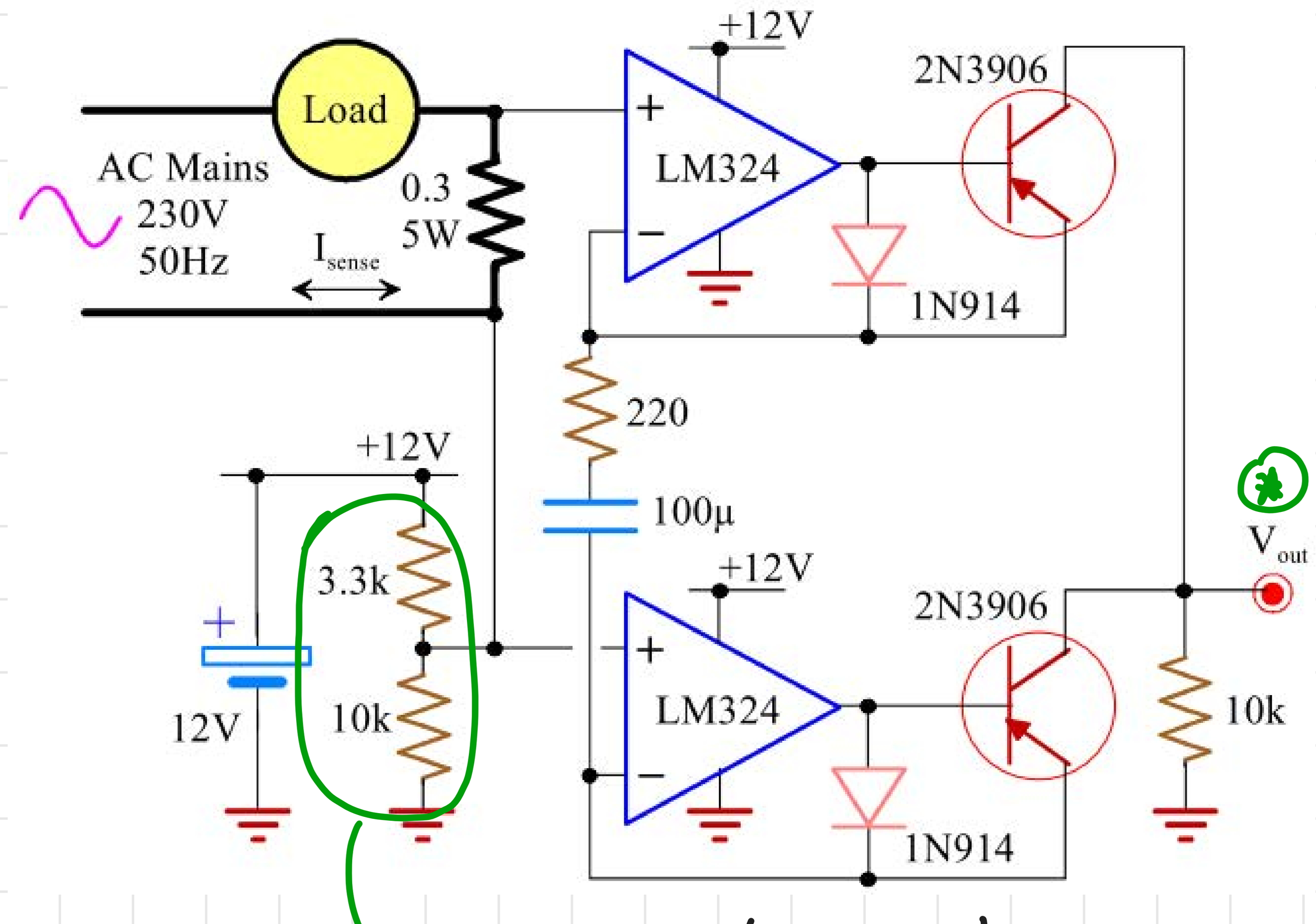




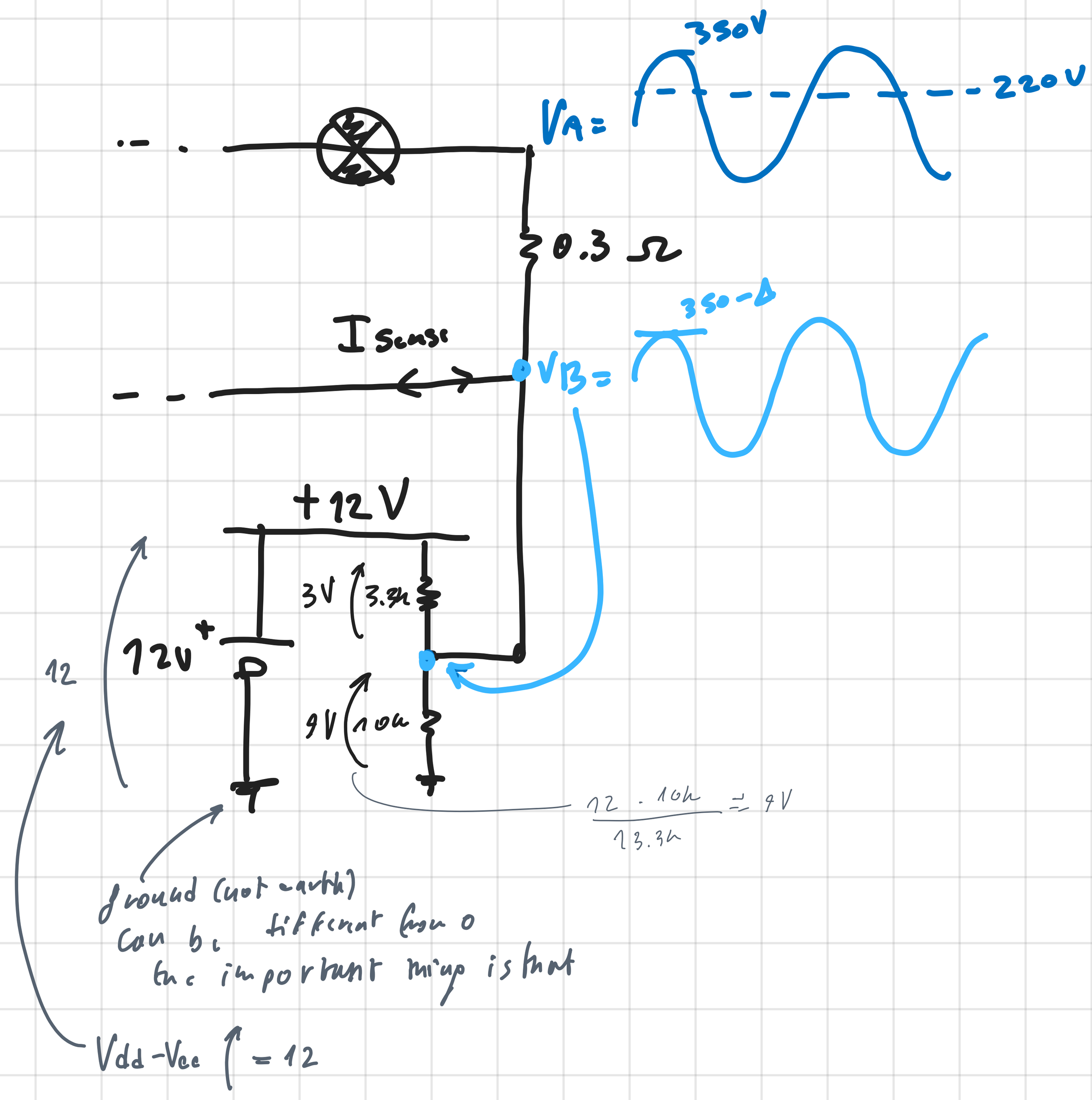
because when the current connection reverse ⊕ the voltage (12V + Δ) drops to zero

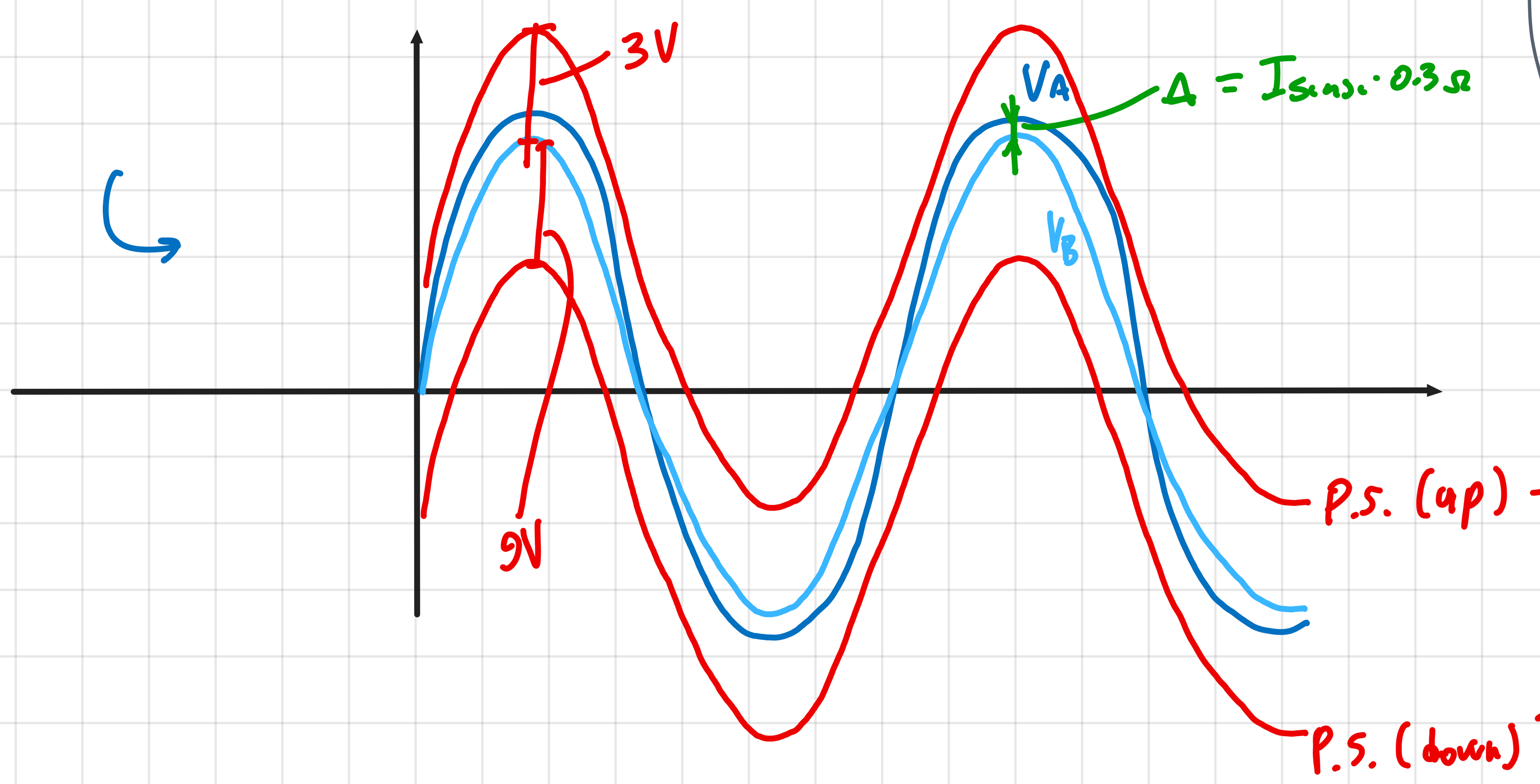
→ we can connect here a battery to provide 12V to VB node

→ in this way the P.S. keeps moving up and down compared to that node



→ thanks to these resistors we can





→ the signals are always in P.S. limits

→ BUT consider that with moving P.S. wrt the earth (0V) we'll have that Vout ⊛ will move wrt the ground (P.S. down) ⟶ if Vout must be used in other circuits it keeps changing and it's not wrt earth (can be dangerous!)

4

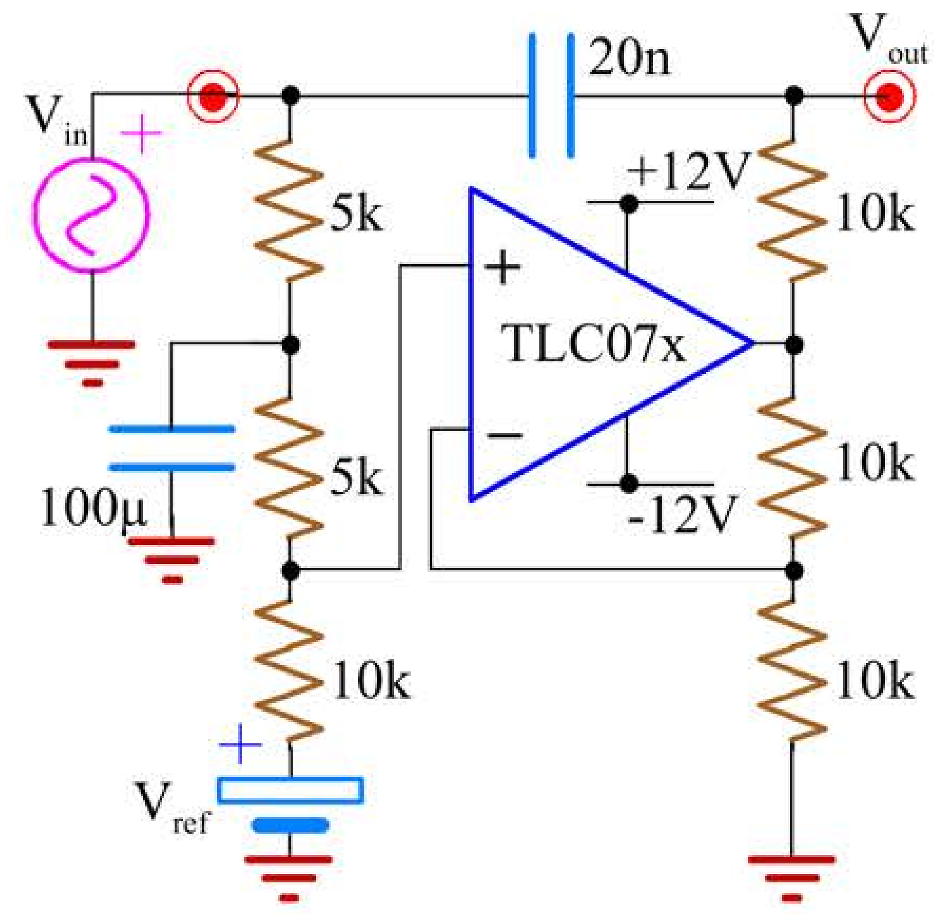
Es. 1

L'OpAMp ha A_0=120dB, GBWP=10MHz, I_{OS}=100pA, V_{OS}=0.5mV. L'uscita è lasciata aperta.

a) Determinare V_{out}/V_{in} in continua e ad alta frequenza ed il guadagno V_{out}/V_{ref}. Disegnare il trasferimento $V_{out}/V_{in}(f)$ e commentare il ruolo del circuito.

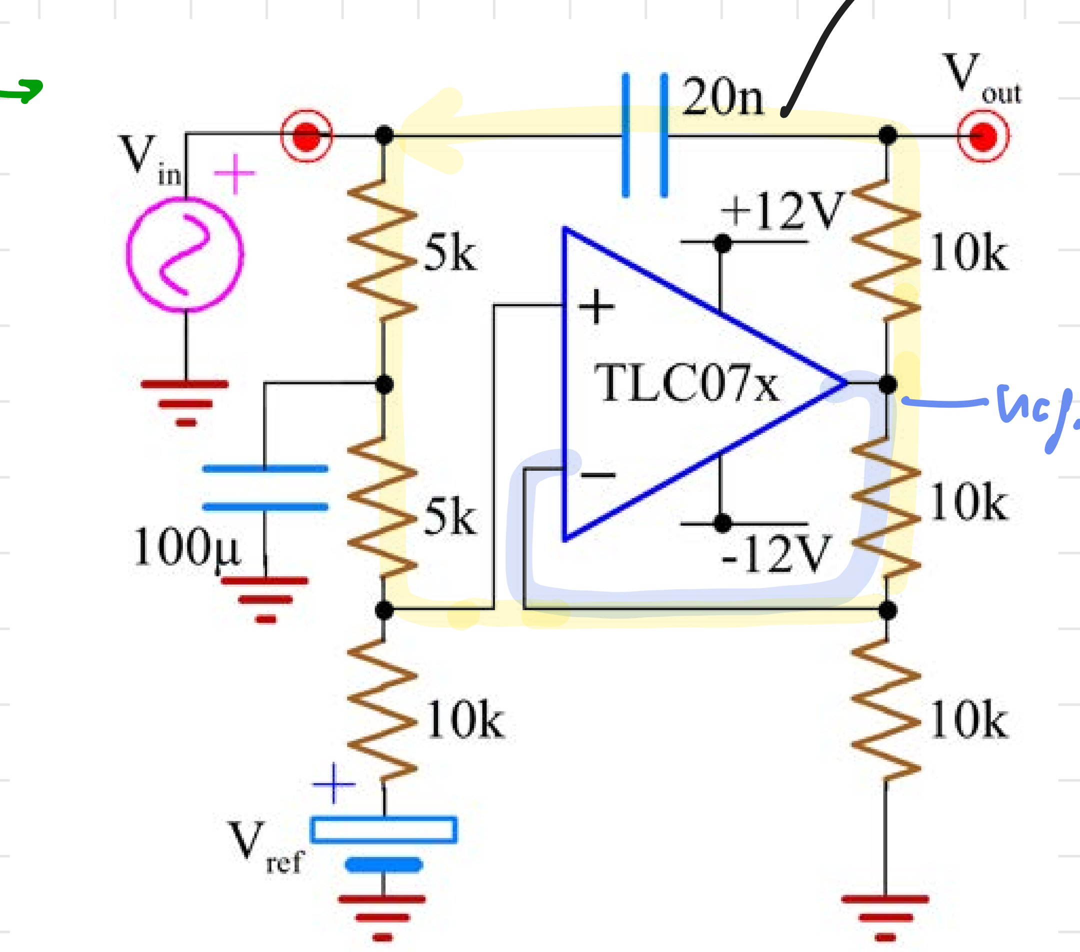
b) Calcolare l'impedenza di uscita del circuito a 10Hz quando V_{in}=+2V.

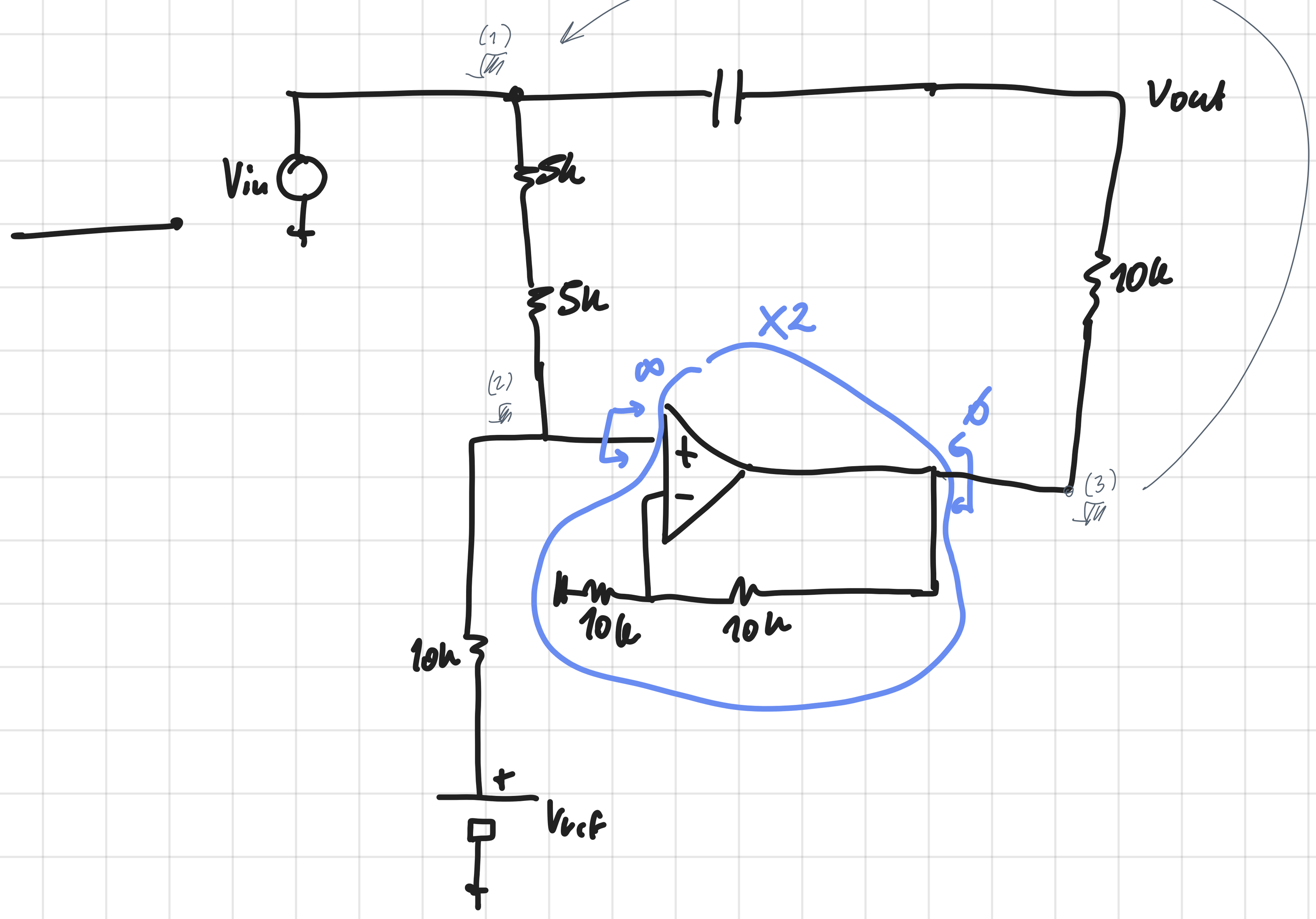
c) Calcolare l'errore in uscita dovuto all'offset di corrente (NON alle I_B) ed a quello di tensione.



so no pos. or neg. feed.

but we cannot vary (in this case increase)

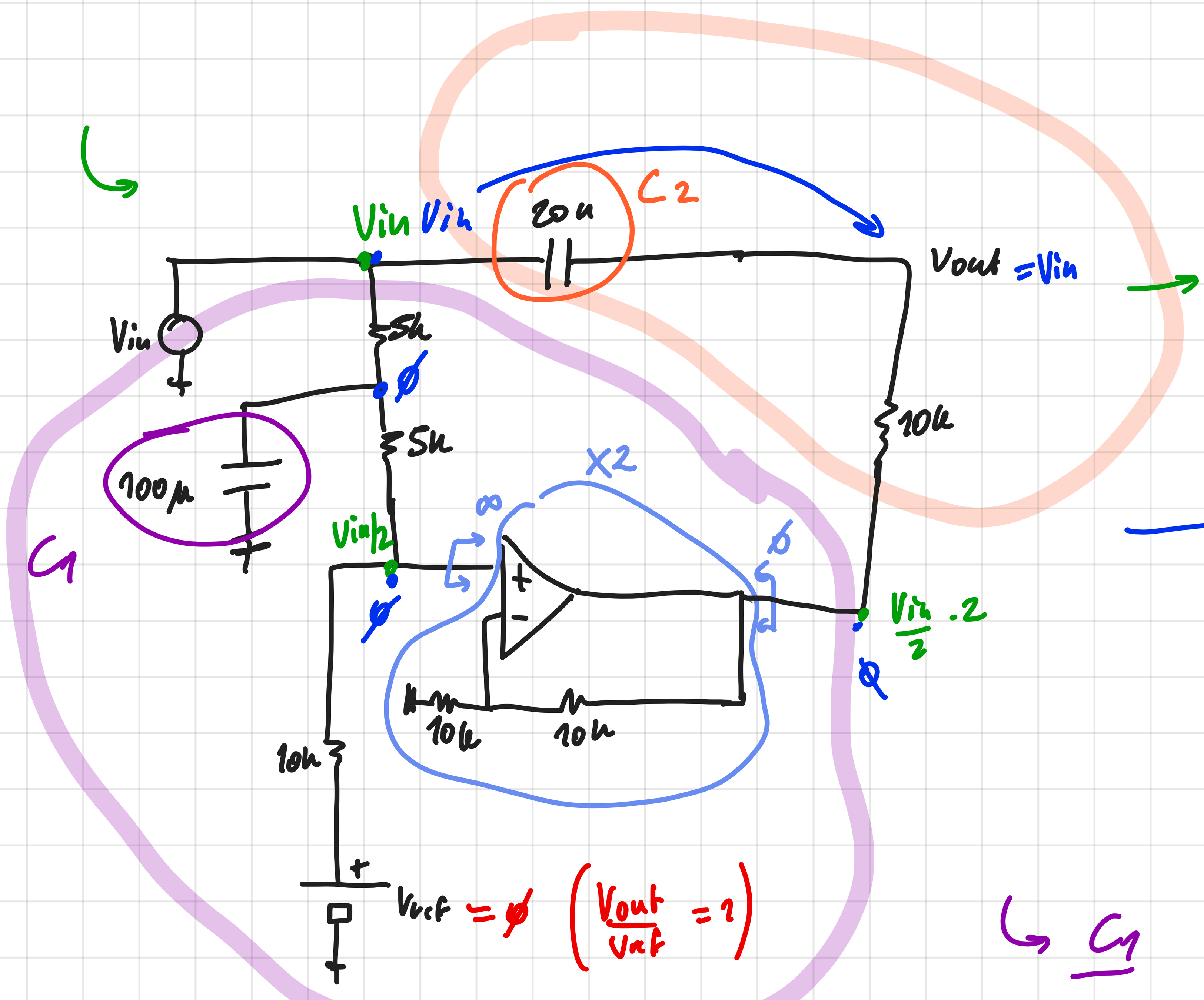




Vin ideal volt. gen

If there where a resistor

would have been a pos. feed.



DC

$$\frac{V_{out}}{V_{in}}(0)=1$$

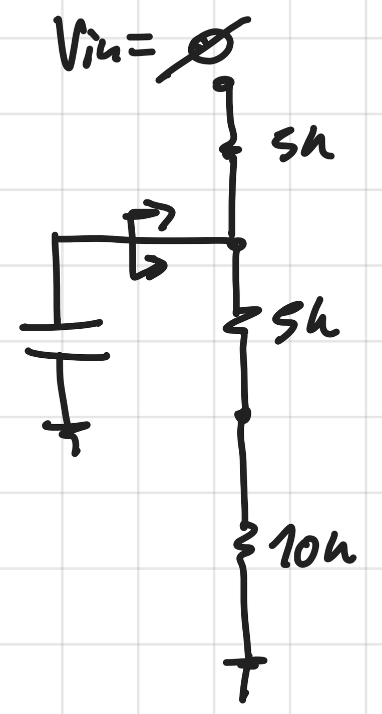
AC

$$\frac{V_{out}}{V_{in}}(\infty)=1$$

but could not be always 1

we have to study the capacitors

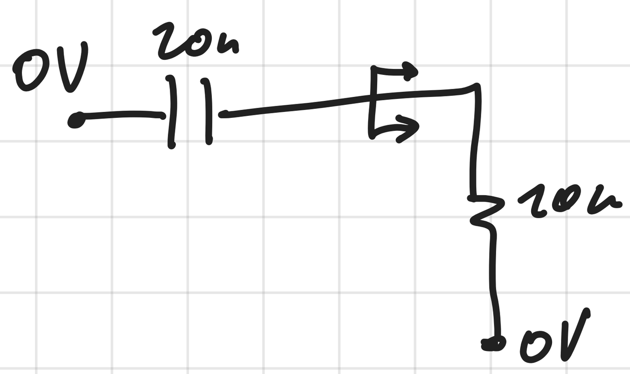
↳ C1 pole:



$$R_{eq} = 5k \,//\, (5k + 10k)$$

$$\hookrightarrow f_{p_1} = \frac{1}{2\pi\,(5k\,//\,15k)\cdot 100\mu} = 0.42\text{Hz}$$

↳ C2 pole:

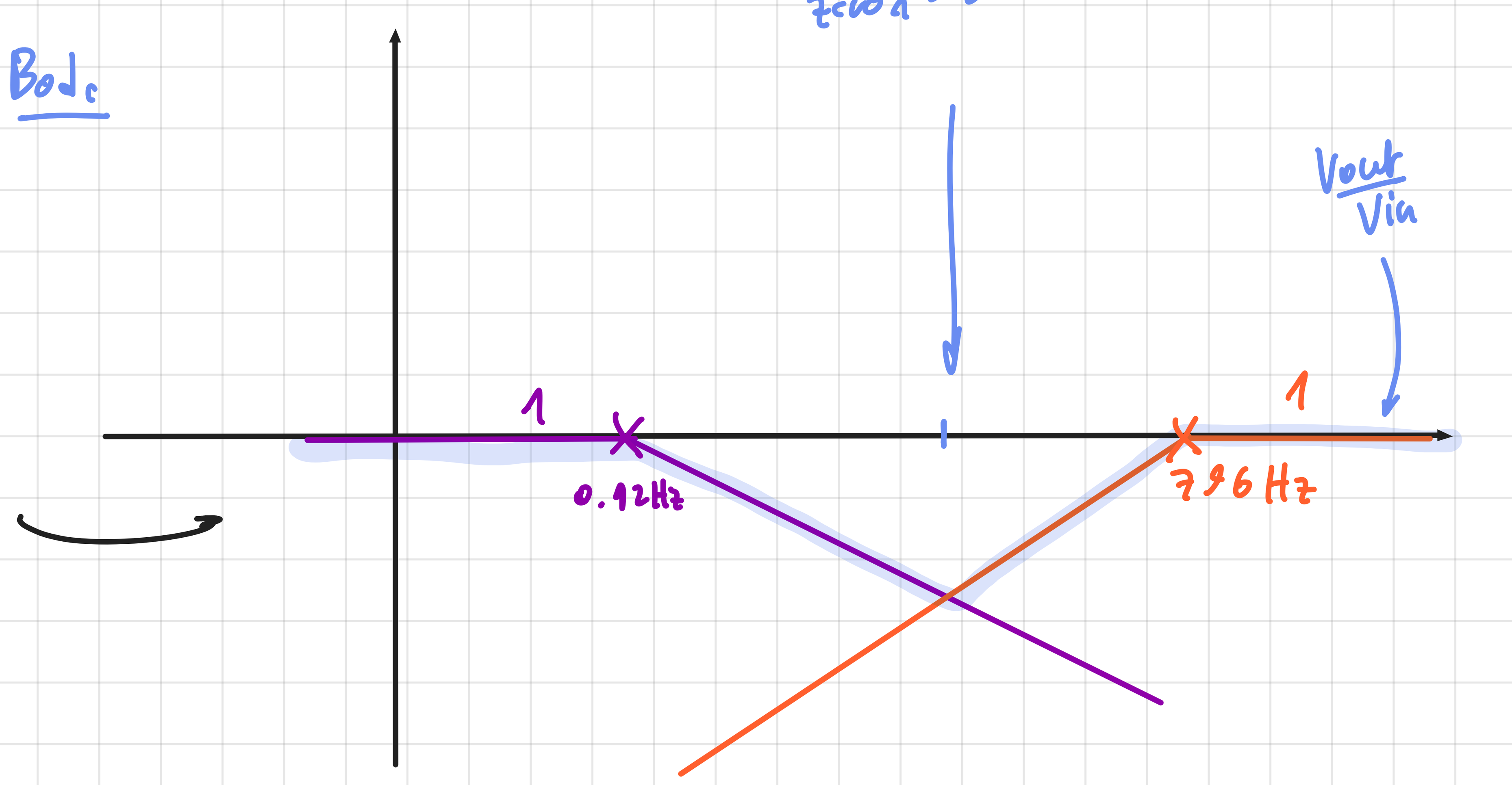


$$f_{p_2} = \frac{1}{2\pi \cdot 20n \cdot 10k} = 796\text{ Hz}$$

$$\text{zero}_1 = \text{zero}_2 = \sqrt{f_{p1}\cdot f_{p2}} = 18.3\text{ Hz}$$

Bode

because they're parallel paths



(5) From 2/09/2010

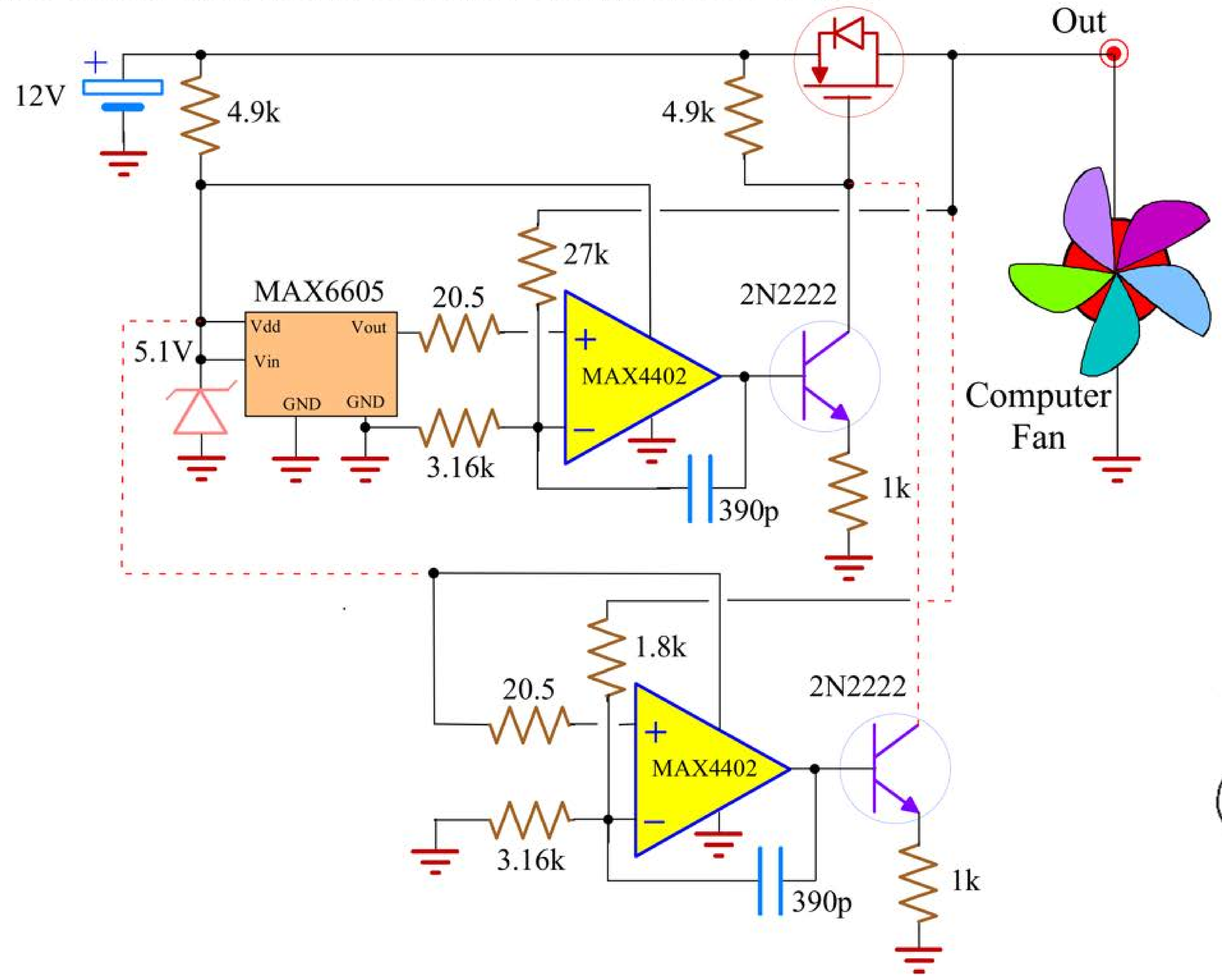
Es. 3

Il sensore di temperatura MAX6605 fornisce $V_T(T)=744mV+T\cdot 11.9mV/°C$.

a) Scollegando il circuito in basso, disegnare il grafico quotato di $V_{out}(T)$ nell'intervallo 0°C÷50°C.

b) Determinare l'intervallo di temperature per cui il circuito è in zona lineare, sapendo che il MAX4402 è *rail-to-rail*.

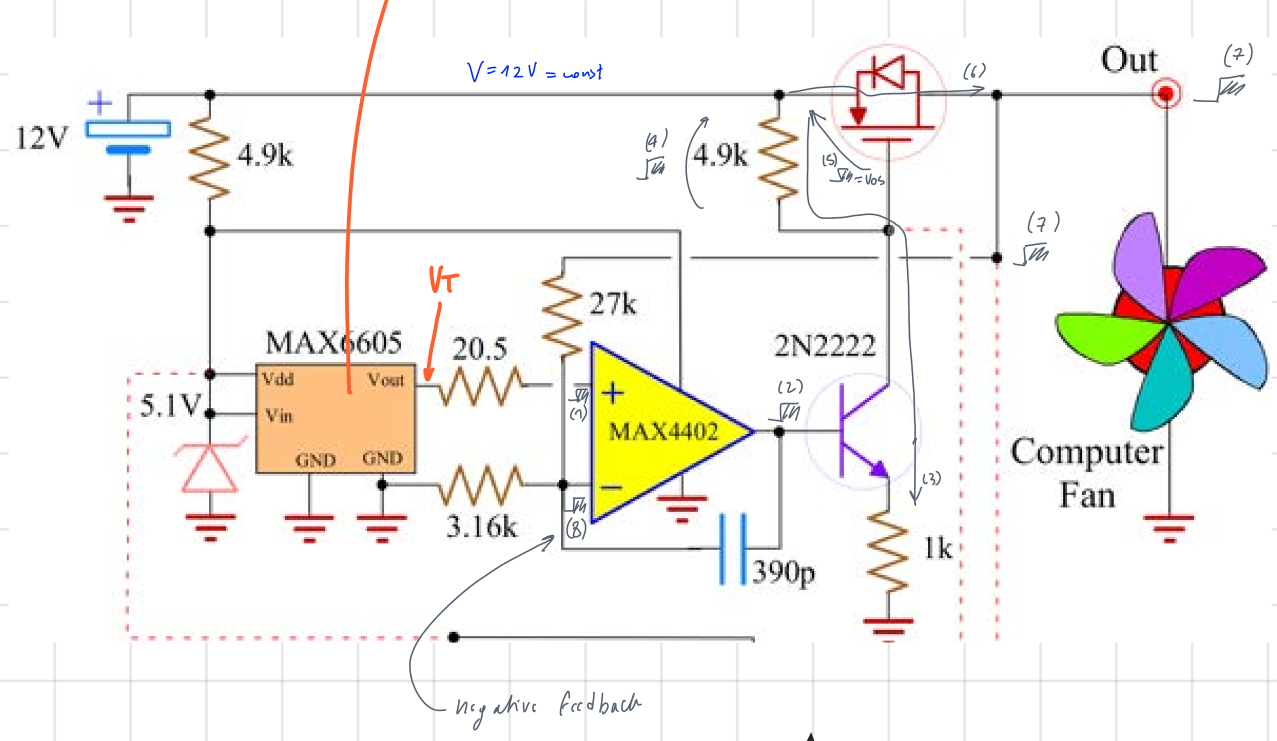
c) Includere ora il circuito in basso e spiegarne dettagliatamente il ruolo.

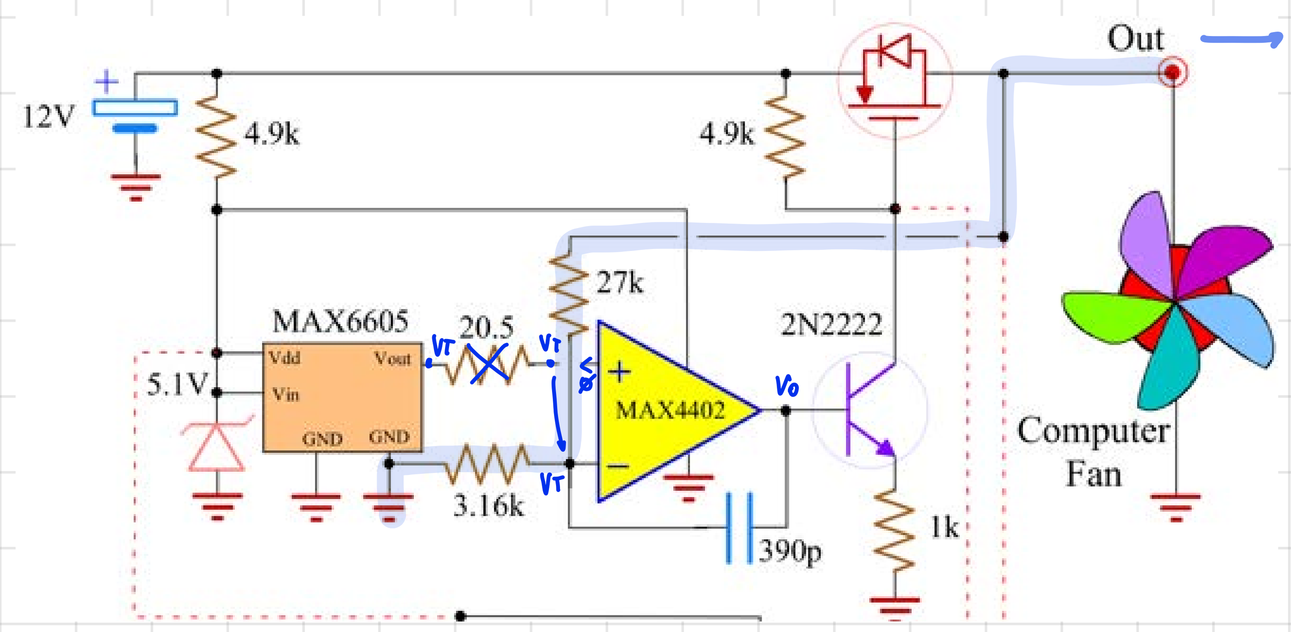


↓ means that the output can reach the P.S.

a)

Temp. sensor → Vout depends on temperature



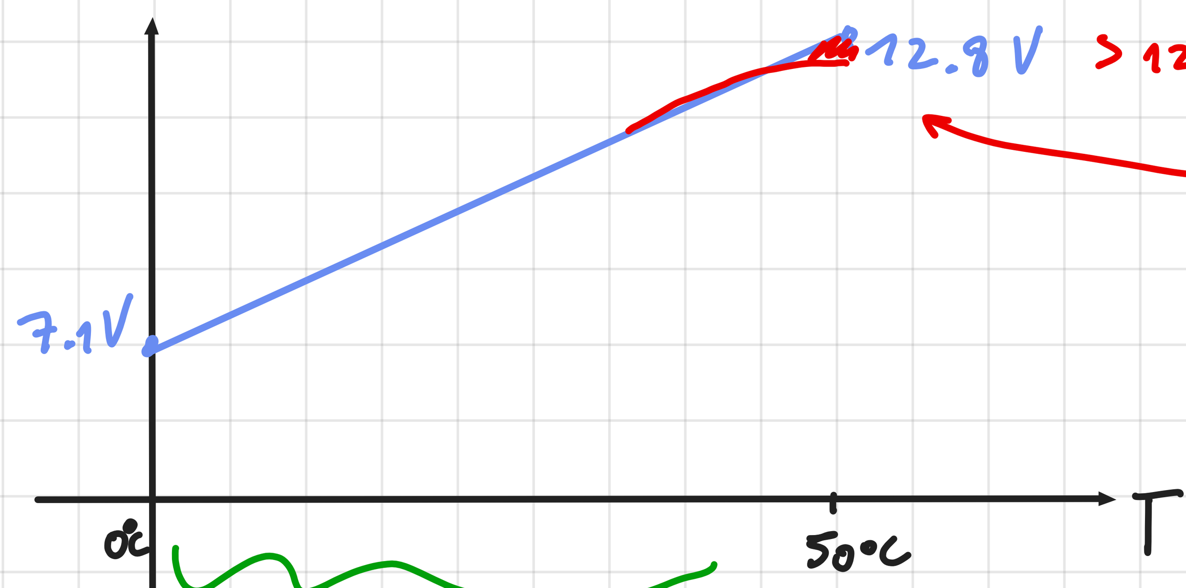


$V_{out}\cdot\frac{3.16k}{3.16k+27k}=V_T$

$\hookrightarrow V_{out}=(744\,mV+11.9\,\frac{mV}{°C}\,T)\cdot 9.5=$

$=7.1\,V+113\,\frac{mV}{°C}\cdot T$

↳ Plot (wrt T):



12.8 V $>12-V_{T_{MOS}}$ → saturates

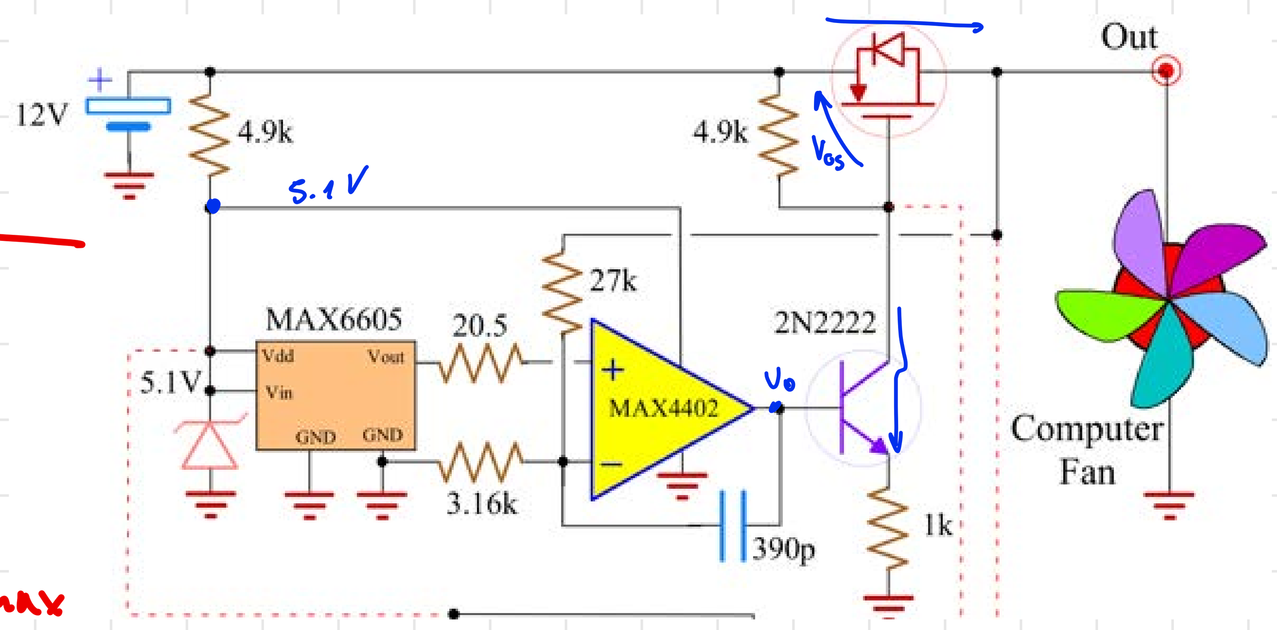
↓ we have to check the limits

zona lin. → T range?

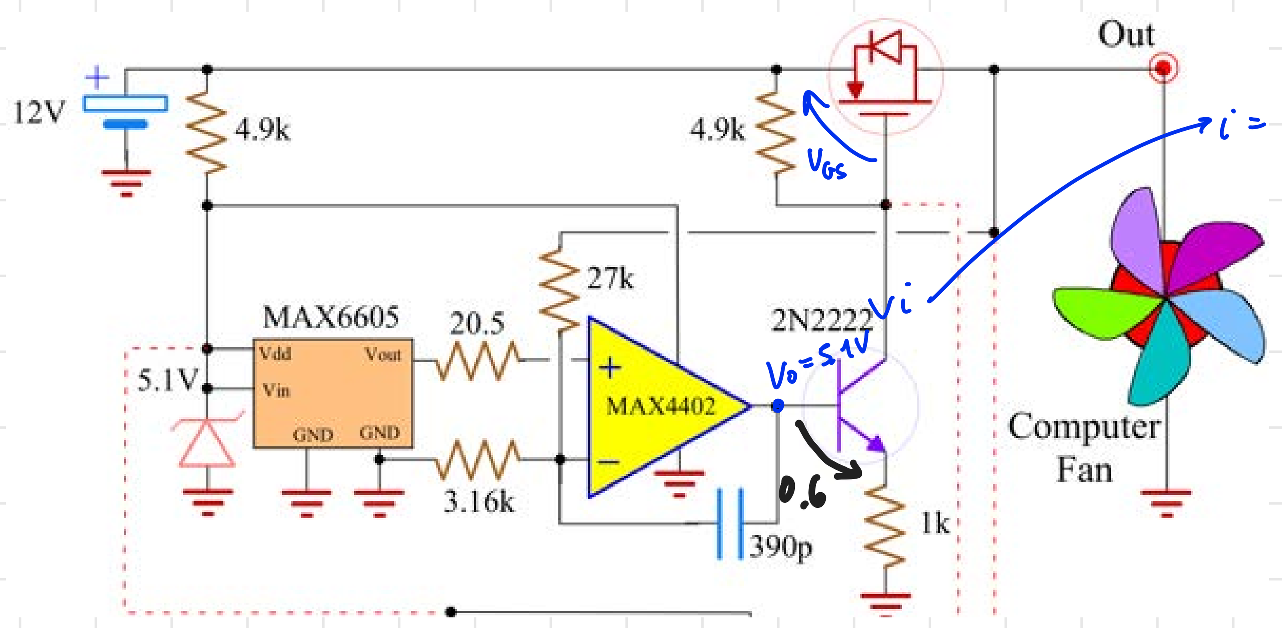
we don't have data, he could have told us to give a current of 200mA to the fan

↓ compute Vos

↓ compute Voutmax and if it's in range

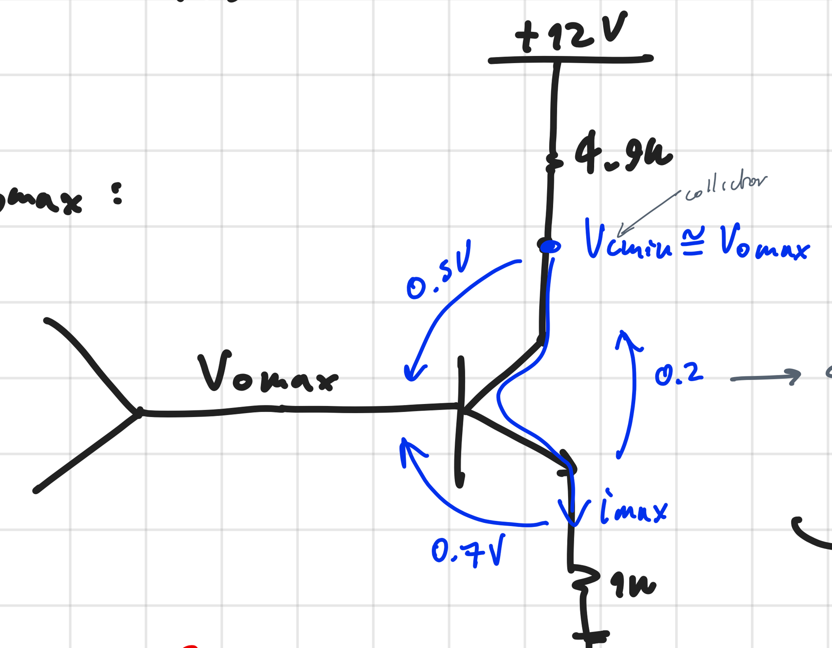


b) Vedere per che range è in zona lin.



$i=\frac{5.1V-0.6}{1k}=4.5mA$ → $V_{OS}=i\cdot 4.9k$

↳ Compute V_{omax}:



$\hookrightarrow 12V-\left(\frac{V_{omax}-0.7}{1k}\right)\cdot 4.9k \geq V_{omax}-0.5$

$\rightarrow 12-V_{omax}\cdot 4.9+3.43\geq V_{omax}-0.5$

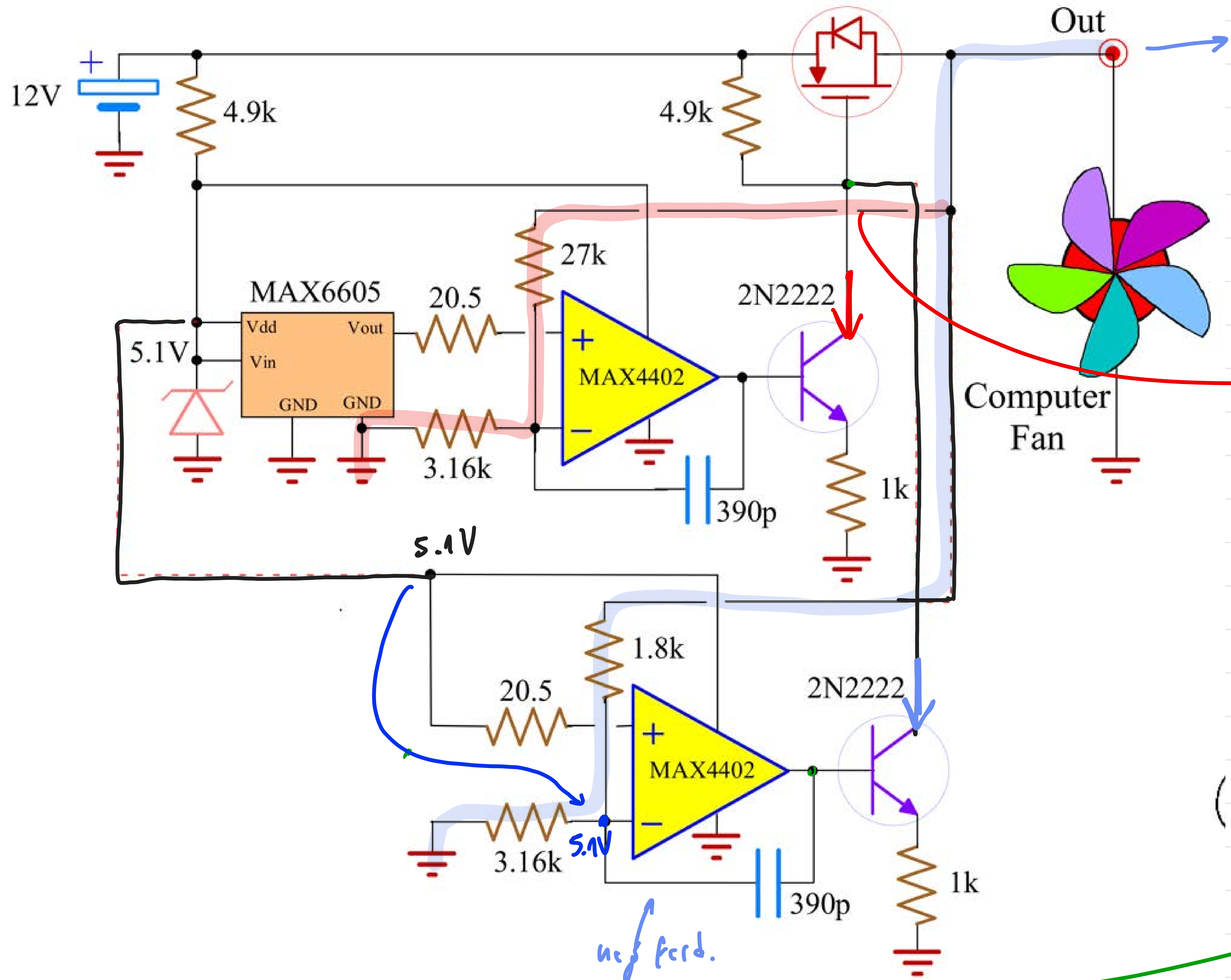
$\hookrightarrow V_{omax}\leq\frac{16}{5.9}=2.7\,V$

If $V_{omax}>2.7$ → BJT enters in saturation

↳ with INFO about the rcos we could have compute the V_{os} and i_{max} and the $V_{out\,max}$ → that depends on T → temp. range

↳ but not given in data → so cannot compute it

c)



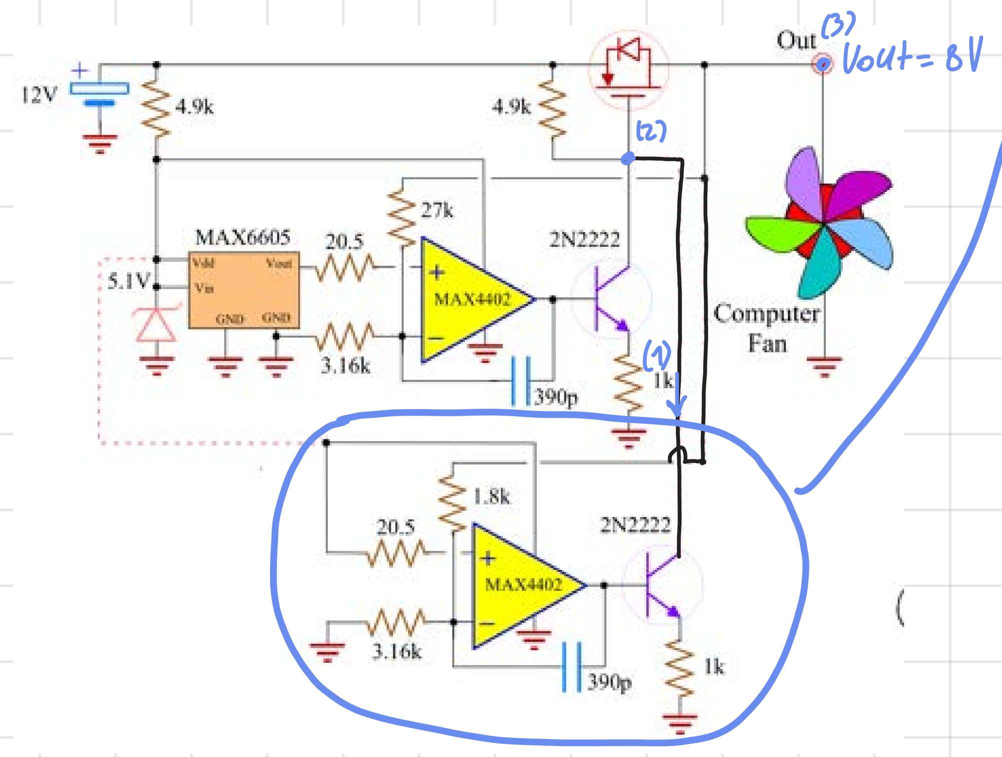
$$V_{out} \cdot \frac{3.16k}{3.16k + 1.8k} = 5.1\,V$$

↳ $V_{out} = 8\,V$

but from the previous circuit

$$V_{out} = 7.1\,V + 113\,\frac{mV}{°C} \cdot T$$

Which one is going to win?

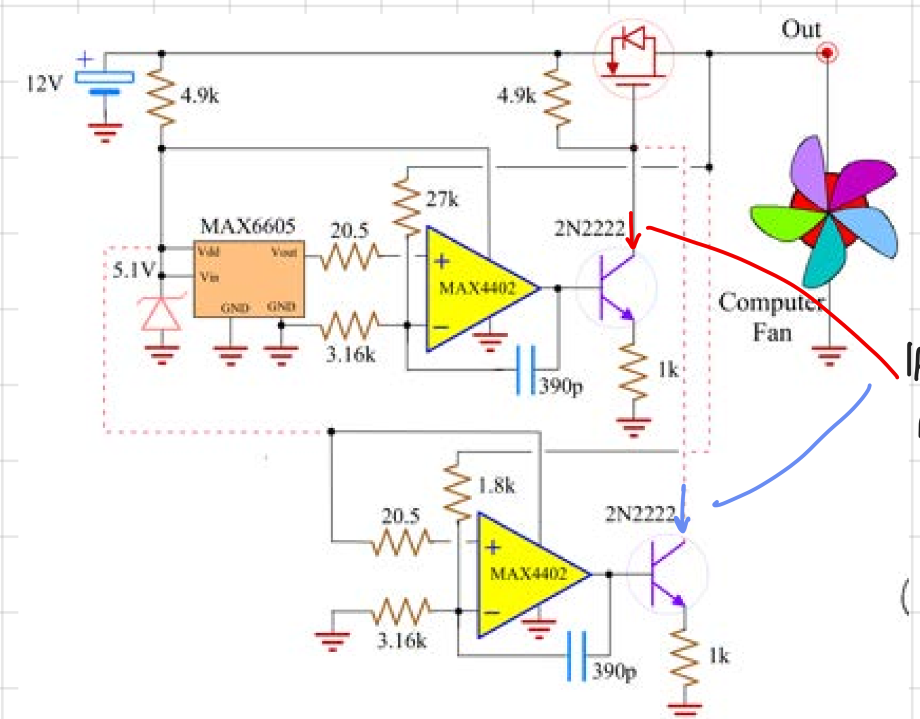


this stage:

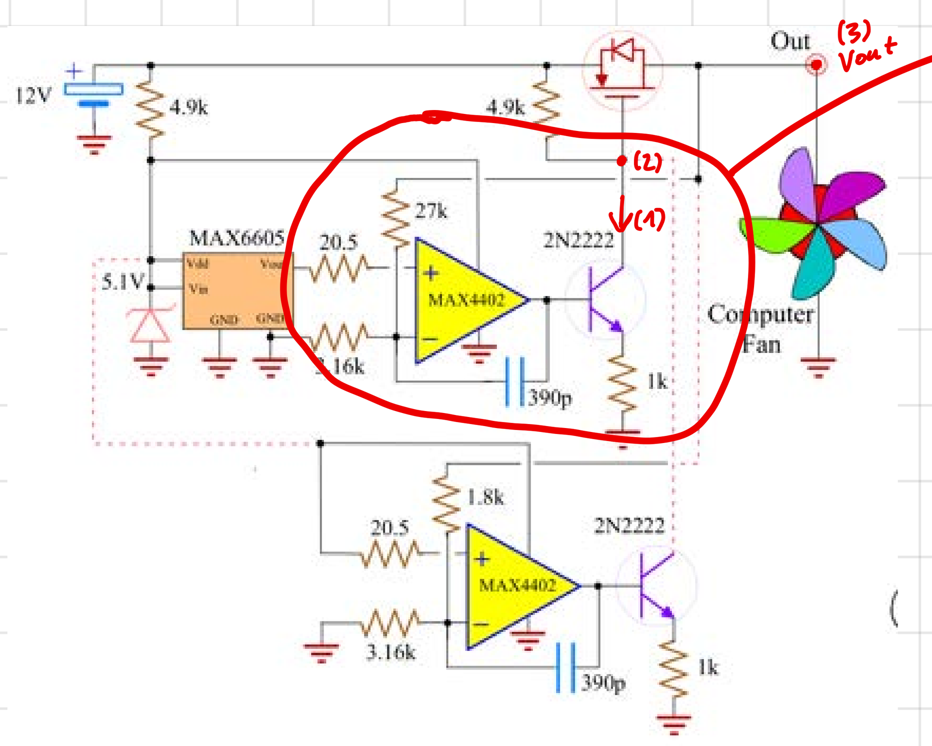
(1) try to set this current here

(2) to adjust the voltage here

(3) in order to have $V_{out} = 8V$



If the currents provided to the mos are different we won't have the desired outputs



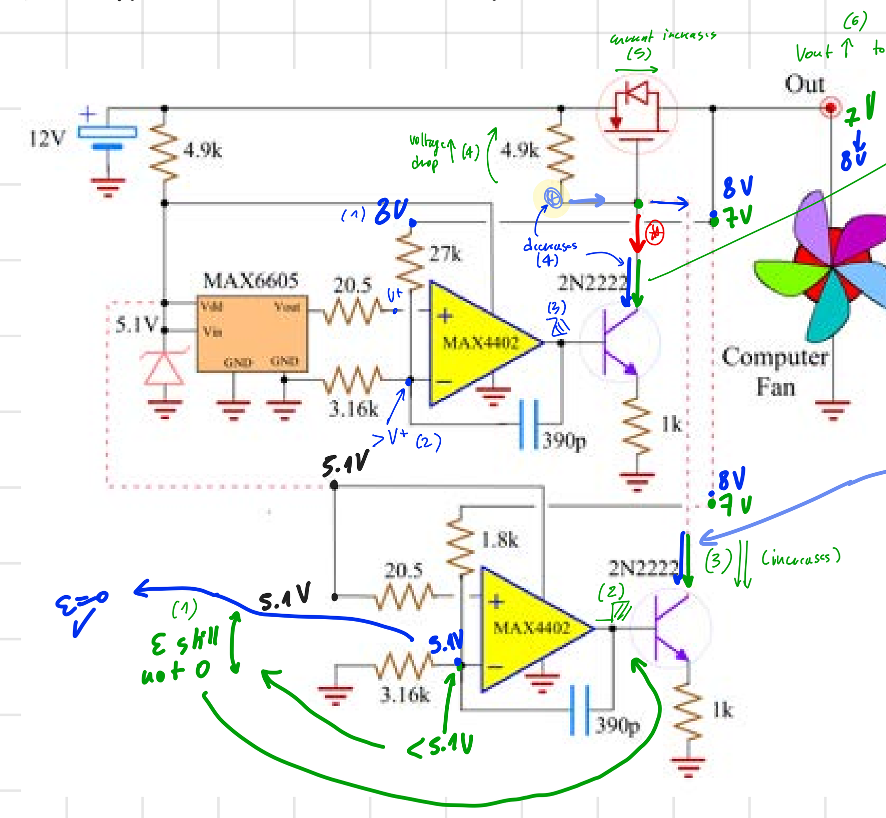
this stage:

(1) try to set this current

(2) in order to set this voltage

(3) in order to have $V_{out} = 7.1V + 113\,\frac{mV}{°C}\,T$

↳ for ex. consider when $T = 0°C$ → $V_{out} \simeq 7\,V$



consider now with 8V

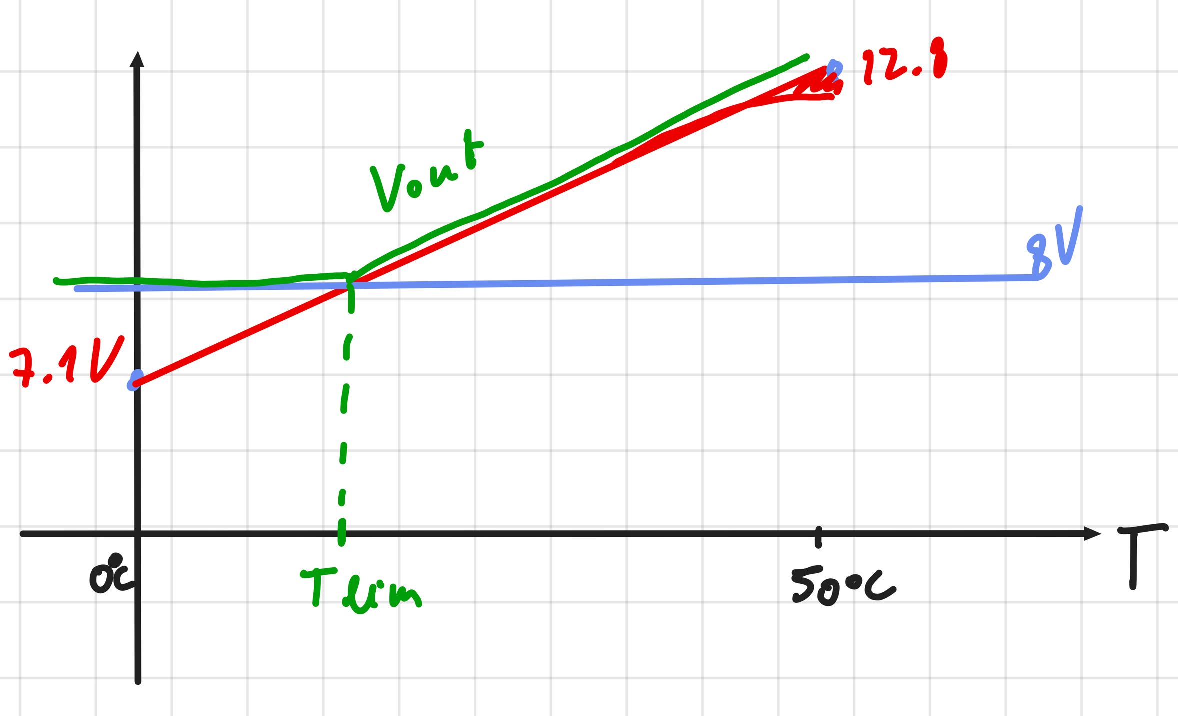
but this current is set by the bottom stage

↳ we cannot reduce this current to have $V_{out} < 8V$

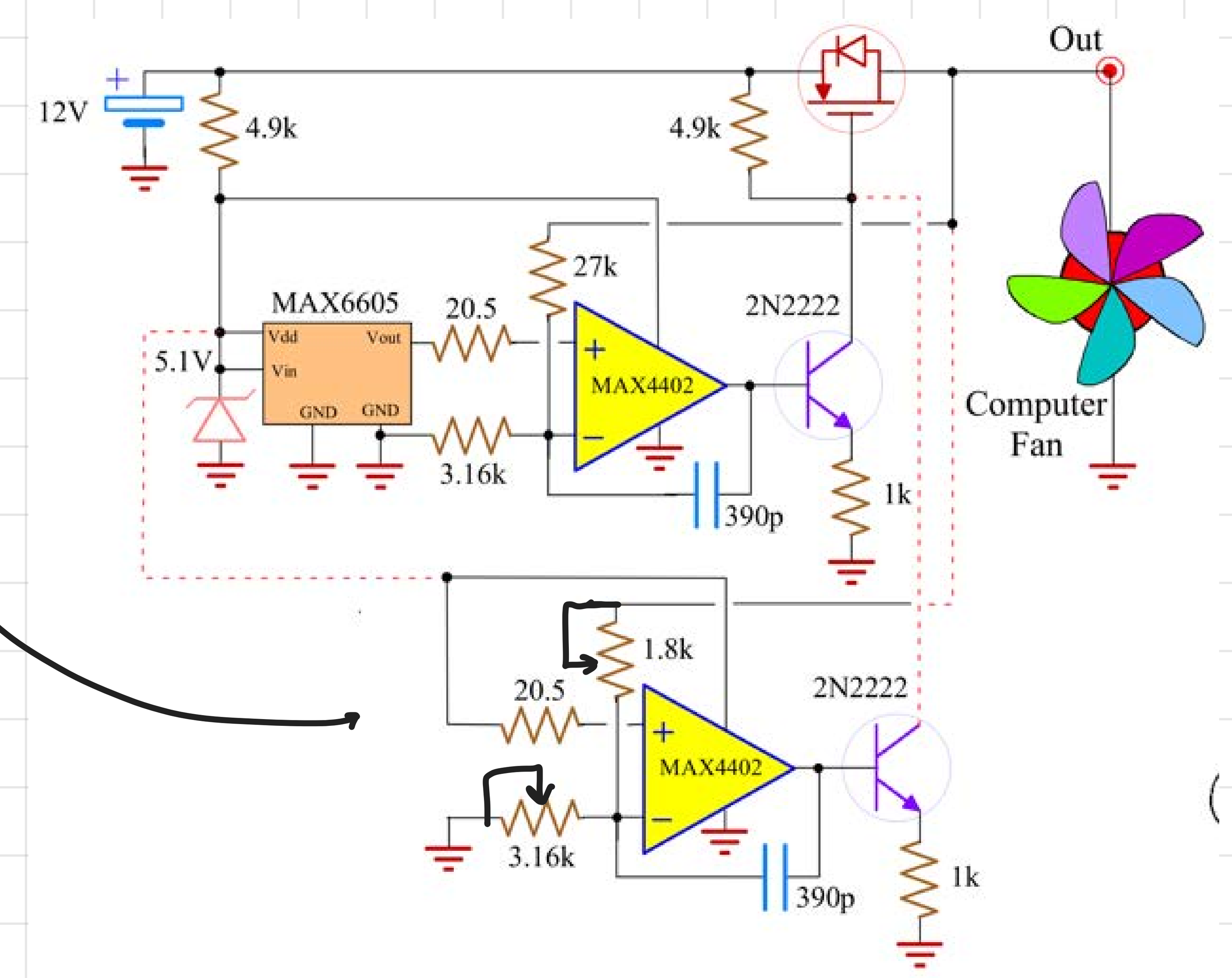
↓

then we can apply a higher curr. and have Vout following the characteristic based on T

↳ the 2 stages are in parallel



→ we can put trimmers to make Vout dependent on T



$$\hookrightarrow \frac{(12.8 - 7.1\,V)}{50°C} = \frac{(8 - 7.1)}{T_{cm}}$$

6

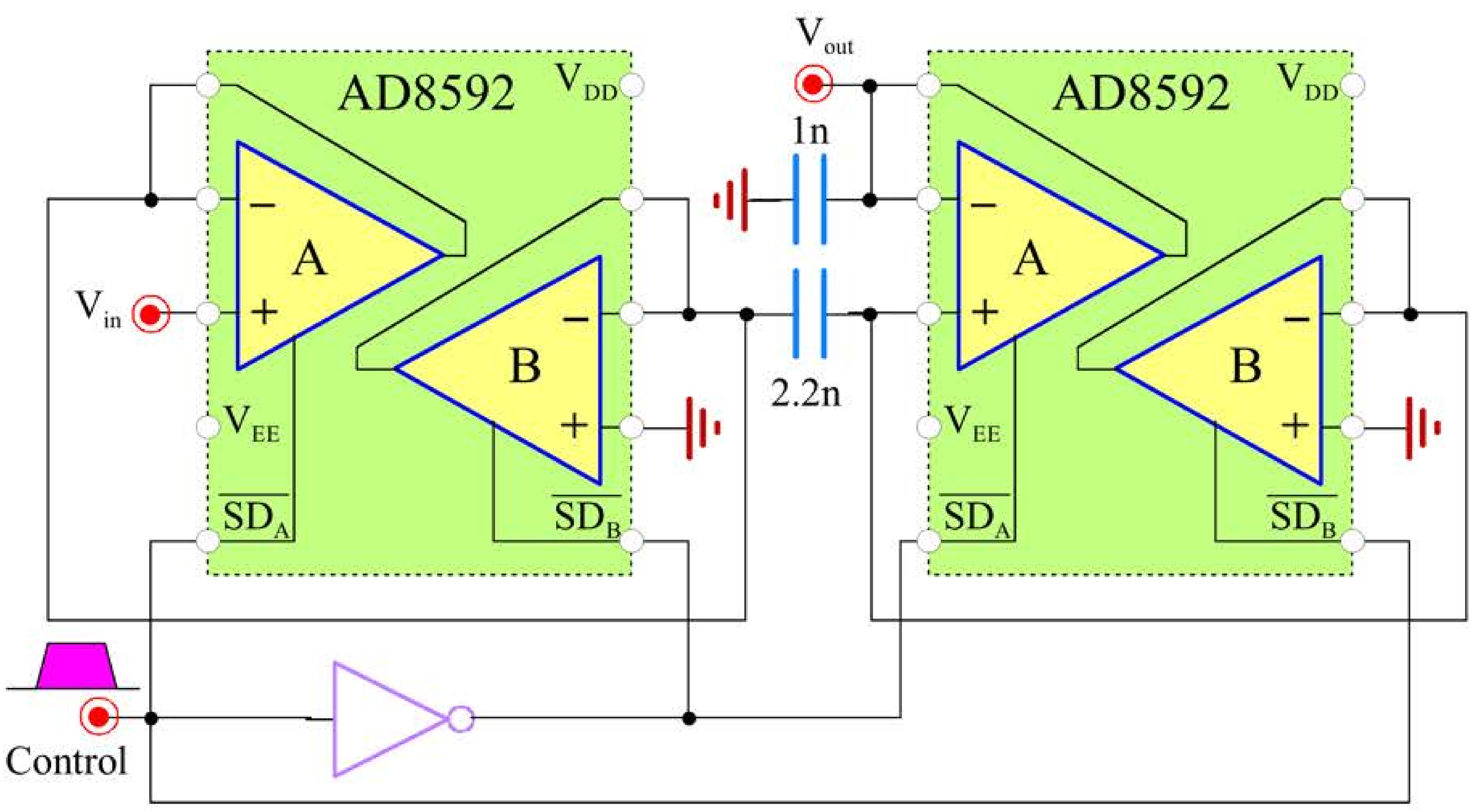
From 23/09/2008

Es. 2

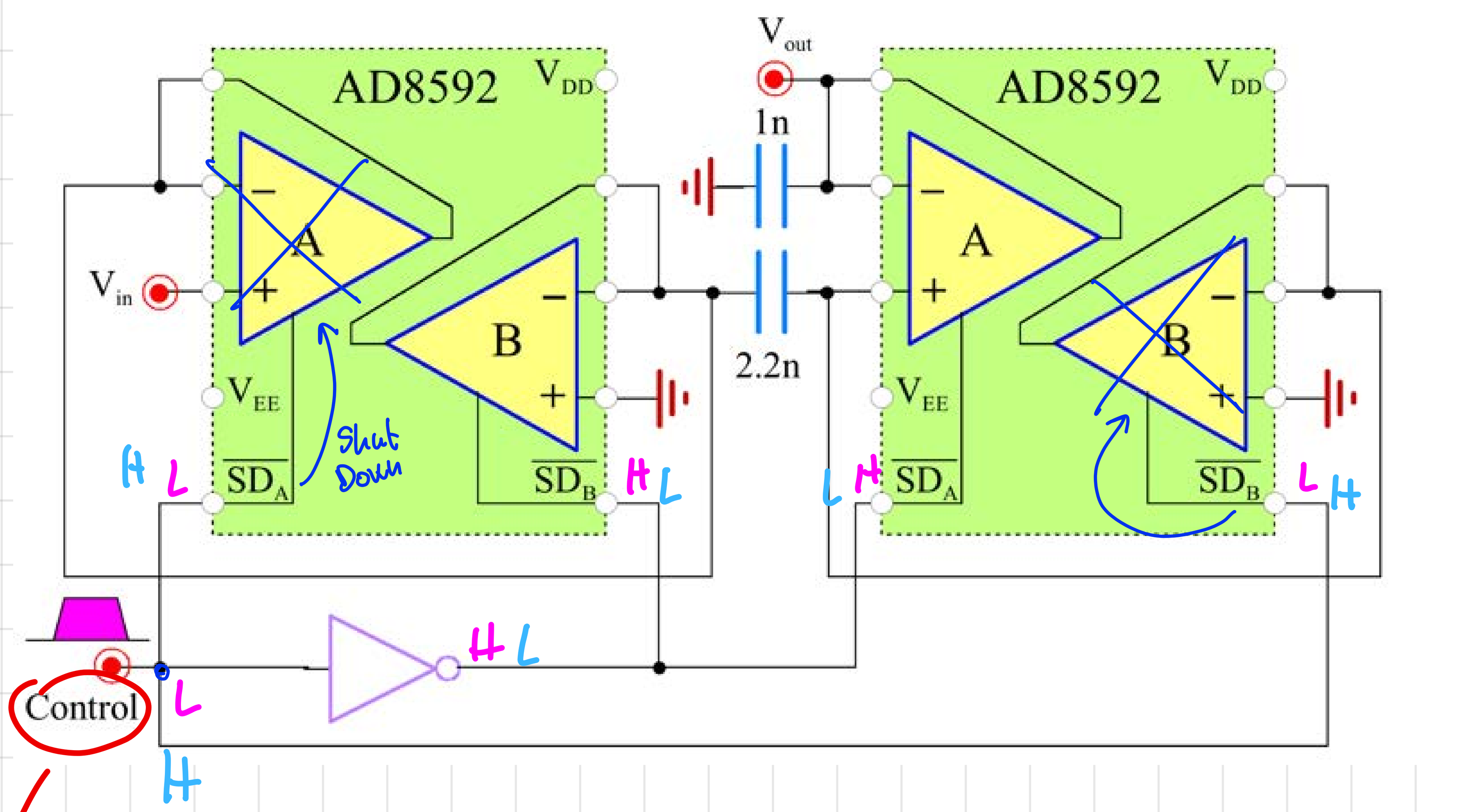
I piedini di ShutDown (SD) *active-low* mandano in *three-state* la rispettiva uscita. Il segnale Control è a 1kHz.

a) Determinare la funzione svolta dal circuito e il legame tra V_{out} e V_{in}. Si consiglia di studiare separatamente il caso Control=*low* e poi Control=*high*.

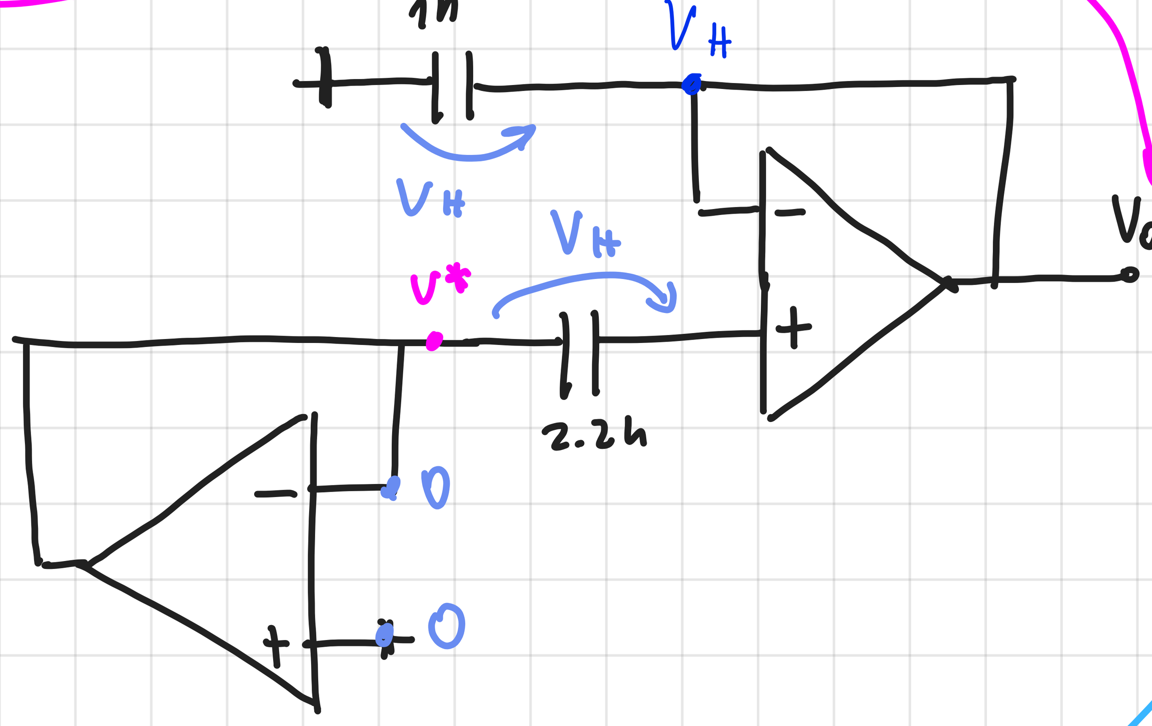
b) Dire cosa accade quando Control=*low* per 1ms e si considerano tutte le I_B=100pA.



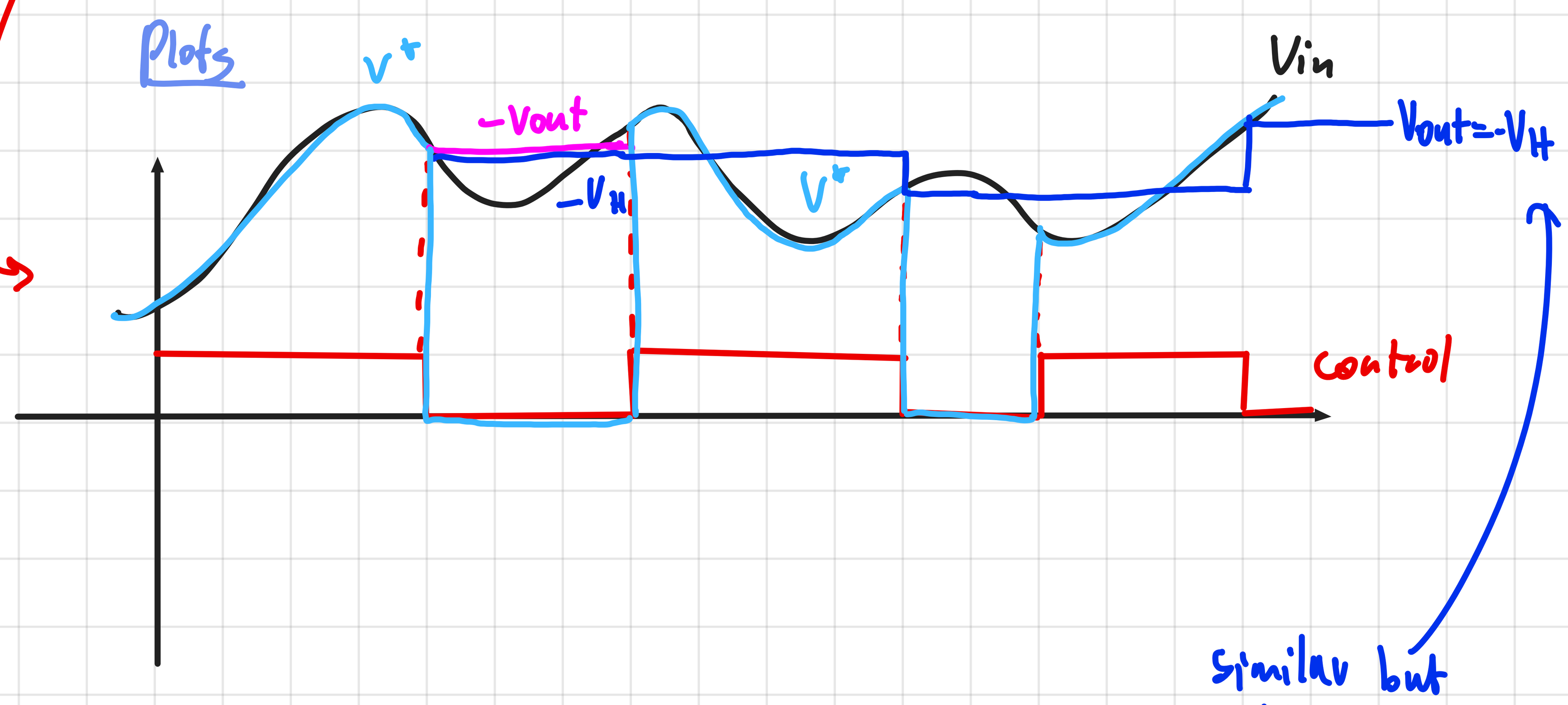
a)



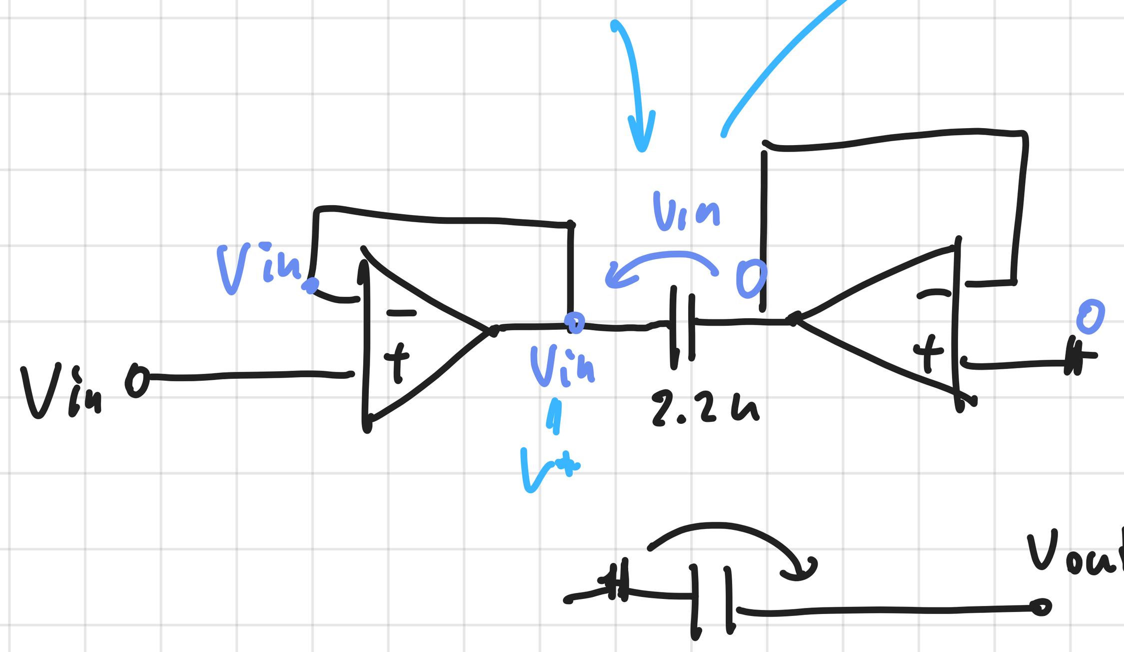
Control = Low → Hold



on the output $V_{out} = V_H = -V_{in}$



Control = HIGH → Sample



$V_{out} = V_H(t-1)$
↑
Value stored previously

Similar but it's NOT a S&H

It's like always in HOLD