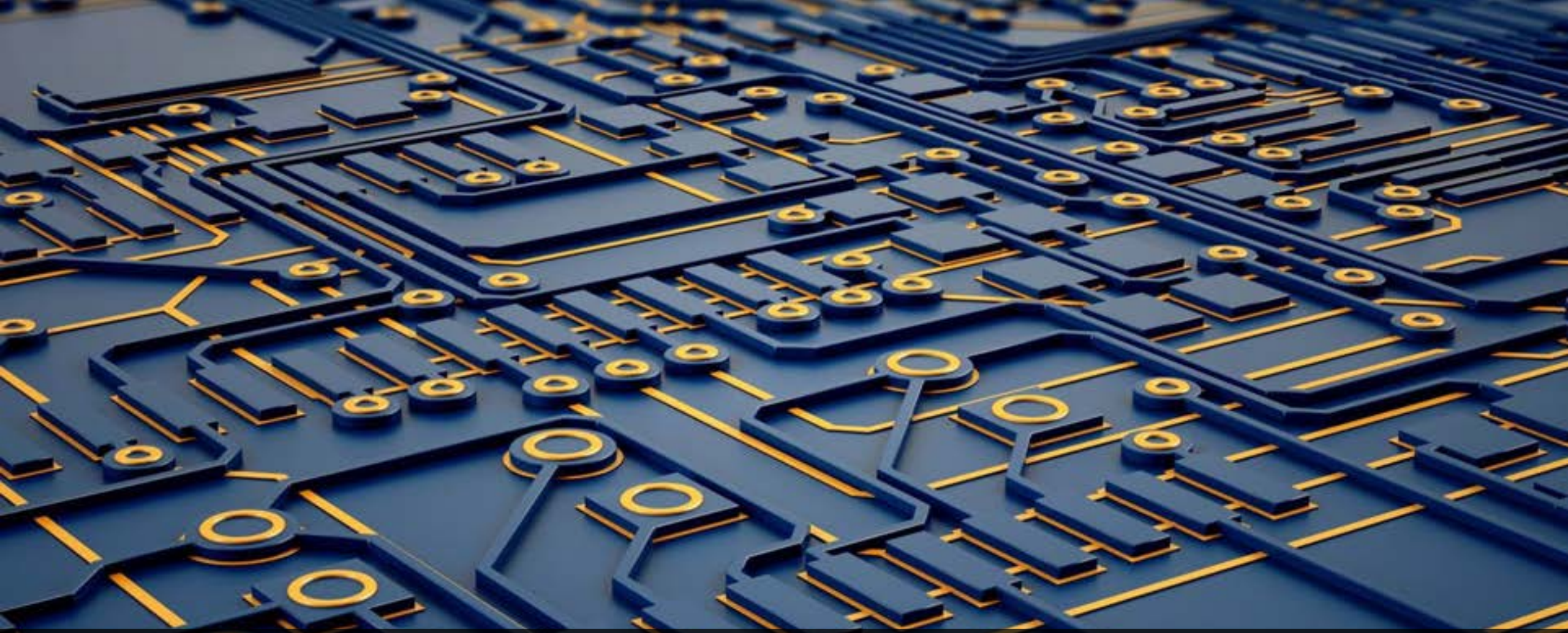


(Prof: Franco Zappa)

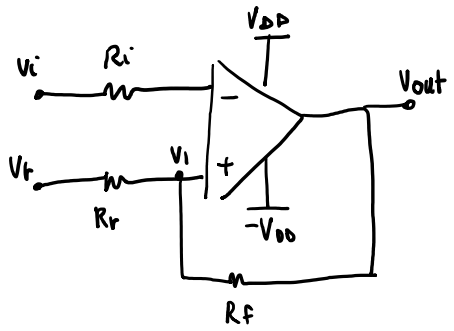
Electronic Systems
Possible oral questions

INDEX

Different OpAmp stages

- e.g. Schmitt trigger

INVERTING

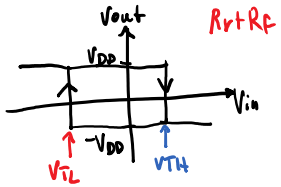


- $V_{in} < V_I \rightarrow V_{out} = V_{DD}$

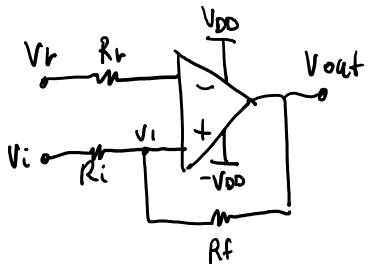
$\hookrightarrow V_I = V_{TH} = V_{DD}\frac{R_r}{R_r+R_f} + V_r\frac{R_f}{R_r+R_f}$

- $V_{in} > V_I \rightarrow V_{out} = -V_{DD}$

$\hookrightarrow V_I = V_{TL} = -V_{DD}\frac{R_r}{R_r+R_f} + V_r\frac{R_f}{R_r+R_f}$



NON-INVERTING



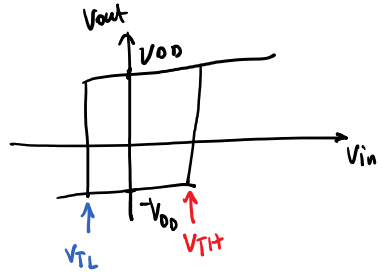
$V_I = V_{in}\frac{R_f}{R_i+R_f} + V_{out}\frac{R_i}{R_i+R_f}$

- $V_I > V_r \rightarrow V_{out} = V_{DD}$

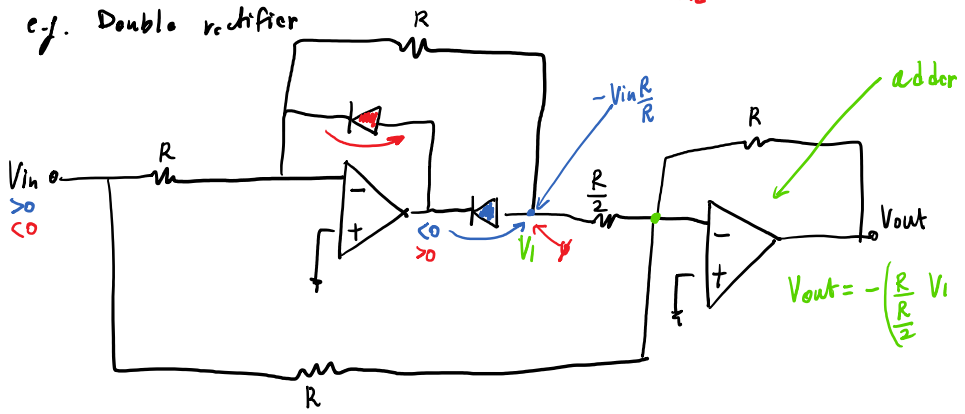
$\hookrightarrow V_{in} = V_{TL} = \frac{R_r+R_f}{R_f}V_r - \frac{R_r}{R_f}V_{DD}$

- $V_I < V_r \rightarrow V_{out} = -V_{DD}$

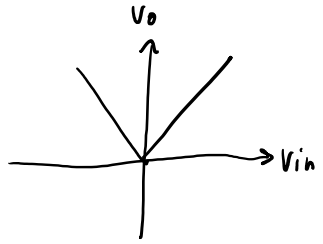
$\hookrightarrow V_{in} = V_{TH} = \frac{R_r+R_f}{R_f}V_r - \frac{R_r}{R_f}(-V_{DD})$

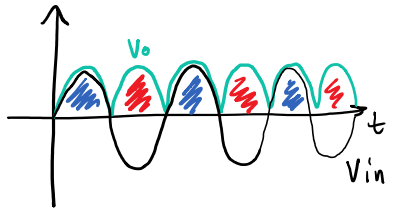


- e.g. Double rectifier



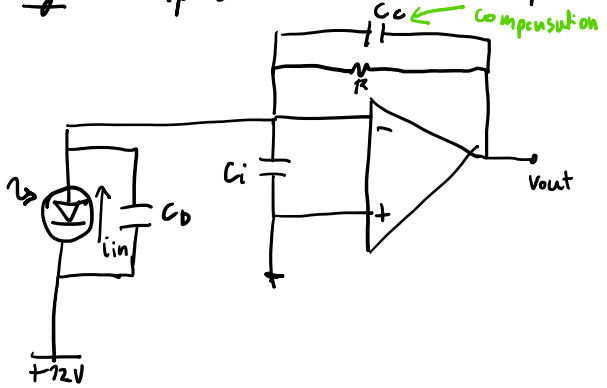
$V_{out} = -\left(\frac{R}{\frac{R}{2}}V_I + V_{in}\frac{R}{R}\right) = \begin{cases} 2V_{in} - V_{in} = V_{in} & >0,\ V_{in}>0 \\ -V_{in} & >0,\ V_{in}<0 \end{cases}$

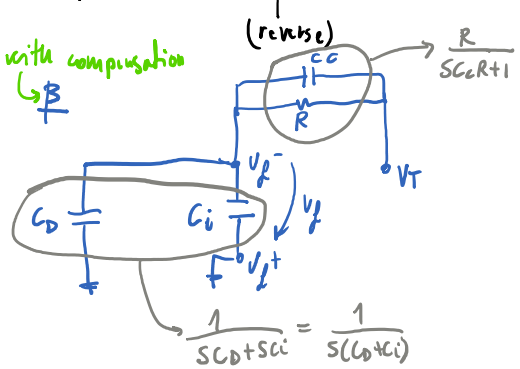




Compensation of particular stages

e.g. Compensation of transimpedance amplifier (photo diode amplifier)



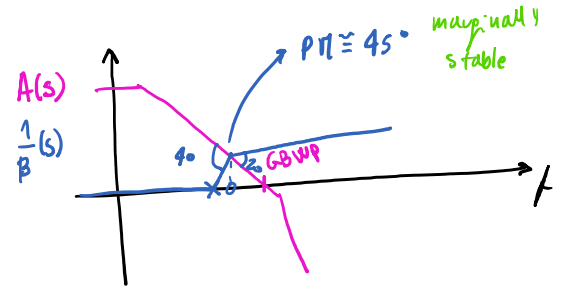


$$V_f^- = -V_f = \frac{\frac{1}{S(C_D+C_i)}}{\frac{1}{S(C_D+C_i)}+\frac{R}{SC_cR+1}} V_T = \frac{SC_cR+1}{S(C_D+C_i)R+SC_cR+1} V_T = \frac{SC_cR+1}{S(C_c+C_D+C_i)R+1} V_T$$

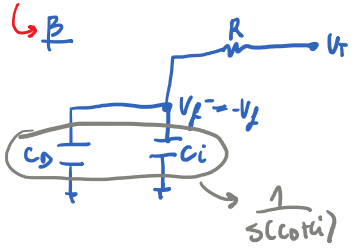
$$\beta_{comp} = -\frac{SC_cR+1}{S(C_c+C_D+C_i)R+1}$$

zero 0

pole x



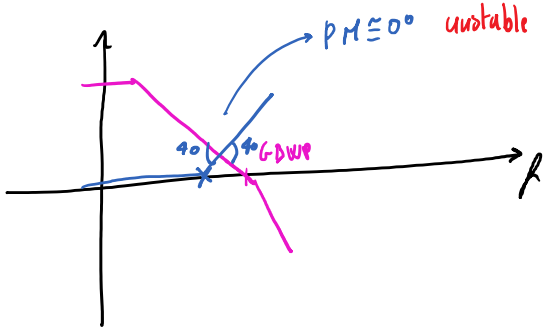
without compensation



$$V_f^- = -V_f = \frac{\frac{1}{SC(C_D+C_i)}}{\frac{1}{S(C_D+C_i)}+R} V_T = \frac{1}{S(C_D+C_i)R+1} V_T$$

$$\beta_{uncomp} = -\frac{1}{S(C_D+C_i)R+1}$$

pole x

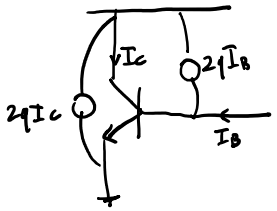


Noise: BJT, diodes

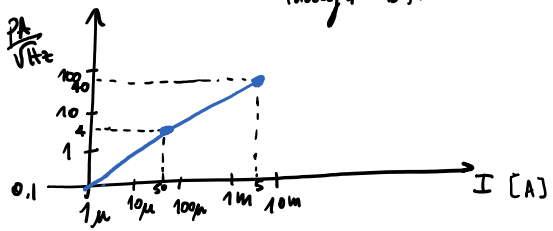
Shot noise : dominant in BJT and diodes

- BJT : shot noise power spectrum : $S(f) \cong 2qI = \frac{\sigma^2}{\Delta f} \rightarrow \sigma^2 = 2qI\,\Delta f$ (Δf: BW of measuring instrument) $\propto$ white noise

  (I: DC current through BJT)



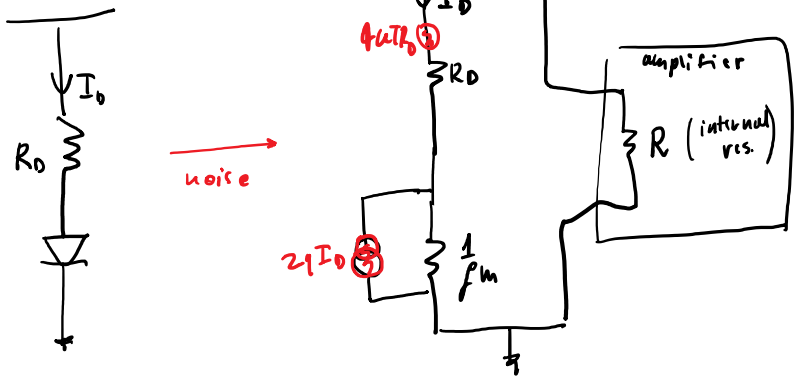
$2qI_C = 2q\beta I_B$



- diodes : dominant shot noise : $2qI_D\Delta f = \langle i^2 \rangle = \sigma^2 = 4kT\,\frac{1}{2kT}\,I_D\,\Delta f$ (also some flicker, but negligible) $\rightarrow$ like thermal noise with eq. resistance $R_{eq} = \frac{2}{g_m}$

  ($\frac{1}{2kT} = \frac{g_m}{2}$)

  $\sigma_{R,I}^2 = \frac{4kT}{R_{eq}}$



$\left(\frac{1}{g_m} = \frac{kT}{qI_D}\right)$

$\frac{V_{noise}^2}{\Delta f} = 2qI_D \left(\frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_D + R}\right)^2 \cdot R^2 + 4kTR_D \left(\frac{R}{R + \frac{1}{g_m} + R_D}\right)^2$

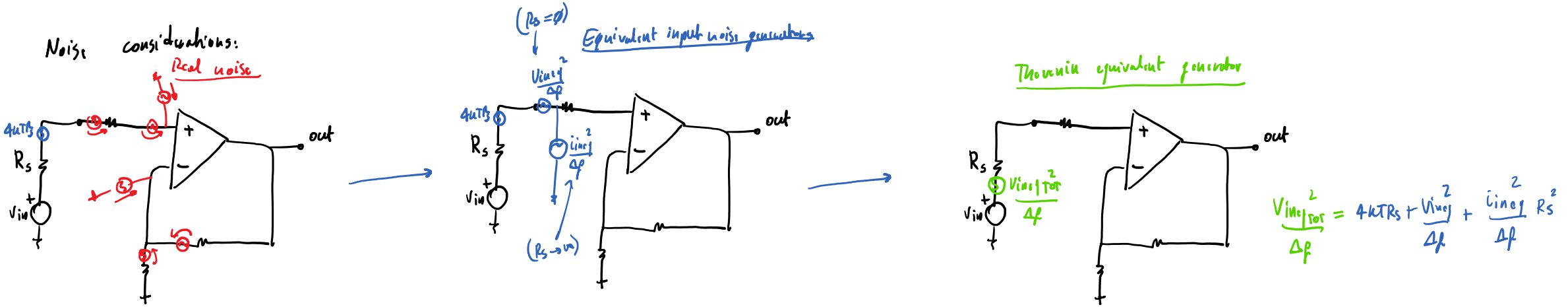
($\frac{1}{g_m} + R_D + R$: negligible)

$\frac{(kT)^2}{I_D^2}$

$\propto \frac{1}{I_D}$

$\propto I_D, R$

Noise: NF



NF = Noise Figure (F linear scale / NF log scale] → NF = 10 log10 F)

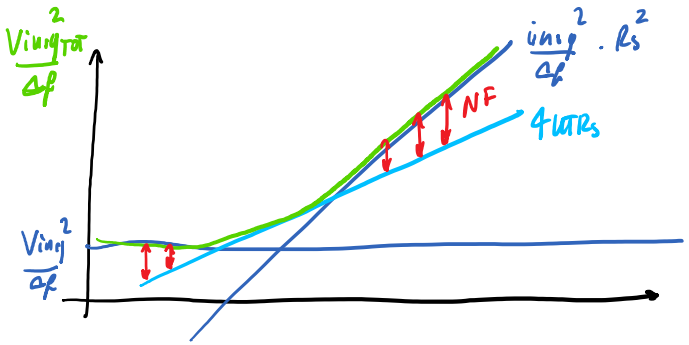
$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in}}{S_{out}} \frac{N_{out}}{N_{in}} = \frac{N_{out}}{G \cdot N_{in}} = \frac{\text{tot out noise}}{\text{out noise due just to } R_s} = \frac{V_{inoj\,tot}^2/\Delta f}{4kTR_s}$$

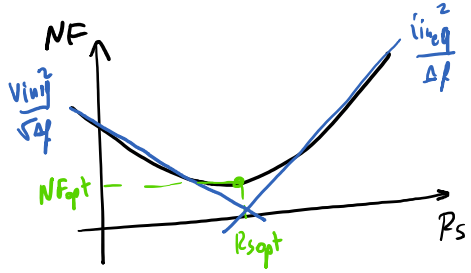
$$\hookrightarrow NF = 10\log_{10}\left(\frac{4kTR_s + \frac{V_{inoj}^2}{\Delta f} + \frac{i_{inoj}^2}{\Delta f} R_s^2}{4kTR_s}\right) = 10\log_{10}\left(1 + \underbrace{\frac{V_{inoj}^2}{\Delta f}\frac{1}{4kTR_s}}_{\propto \frac{1}{R_s}} + \underbrace{\frac{i_{inoj}^2}{\Delta f}\frac{R_s}{4kT}}_{\propto R_s}\right)$$

Optimum

$$\frac{dF}{dR_s} = -\frac{\left(\frac{V_{inoj}}{\Delta f}\right)^2 4kT}{(4kTR_s)^2} + \frac{\frac{i_{inoj}^2}{\Delta f}}{4kT} = 0$$

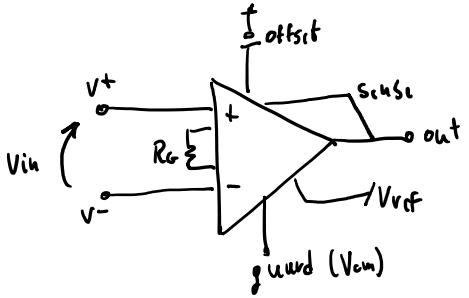
$$\hookrightarrow R_{sopt} = \sqrt{\frac{\frac{V_{inoj}^2}{\Delta f}}{\frac{i_{inoj}^2}{\Delta f}}}$$



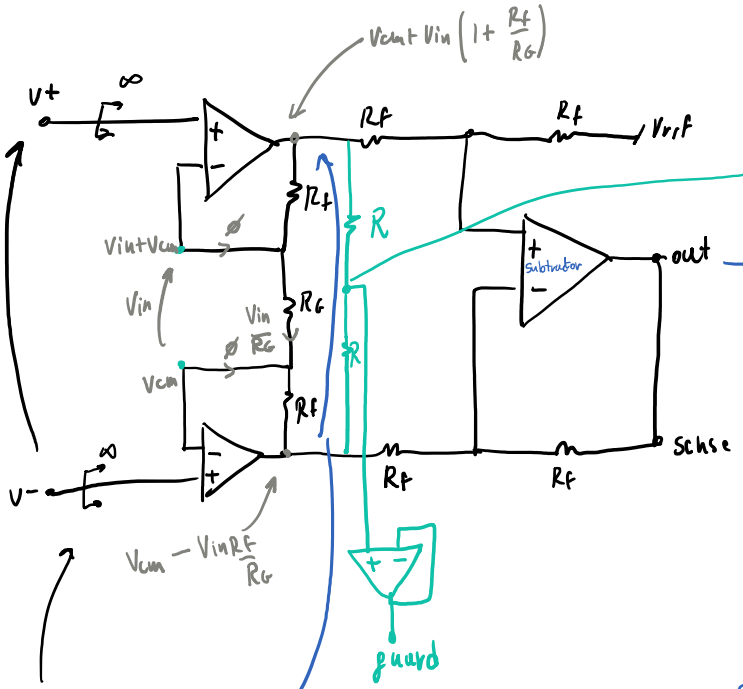


INA

INA = INstrumentation Amplifier



inside



Vin + Vcm — common mode

$V_{guard} = \left[V_{cm} + V_{in}\left(1 + \frac{R_f}{R_G}\right)\right]\cdot\frac{R}{2R} + \left[V_{cm} - V_{in}\frac{R_f}{R_G}\right]\frac{1}{2} = V_{cm}$ (for $V_{in} = 0$)

$V_{out} = V_{out,diff} + V_{ref} = G_{INA}\,V_{in} + V_{ref}$

$V_{out,diff} = \cancel{V_{cm}} + V_{in}\left(1 + \frac{R_f}{R_G} - \left(-\frac{R_f}{R_G}\right)\right) \cancel{- V_{cm}} = V_{in}\left(1 + 2\frac{R_f}{R_G}\right)$ (G_{INA})

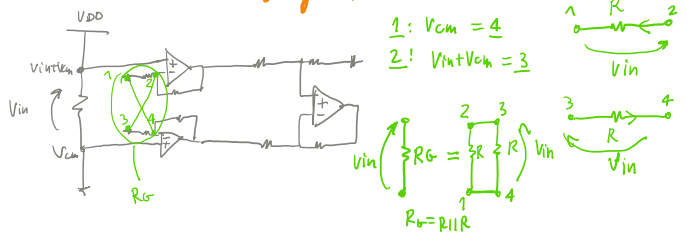
common mode rejection

Pros:
- finite, accurate and reliable gain
- train input impedance extremely high (voltage reader)
- extremely low output impedance
- extremely high CMRR (Common Mode Rejection Ratio)

Why the use of R_G?

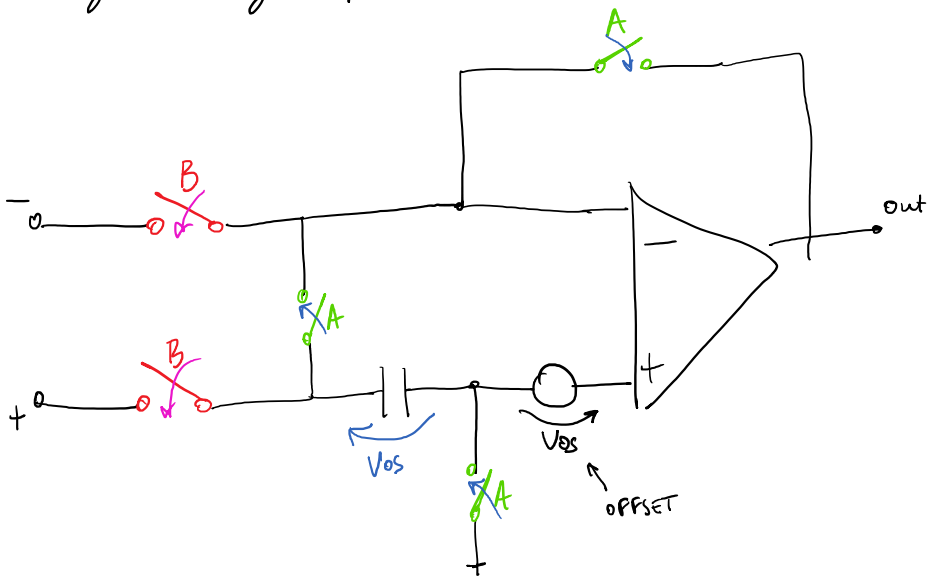
1st reason: • To read the differential input signal we could use buffer, but it's better to put the buffers at the end and amplify first. → so we don't have noise amplification

2nd reason: The previous solution if there's Vcm it could easily saturate due to the amplification G. So we can connect in this way the stages:



CAZ OpAmp

CAZ = Commutating Auto Zeroing OpAmp



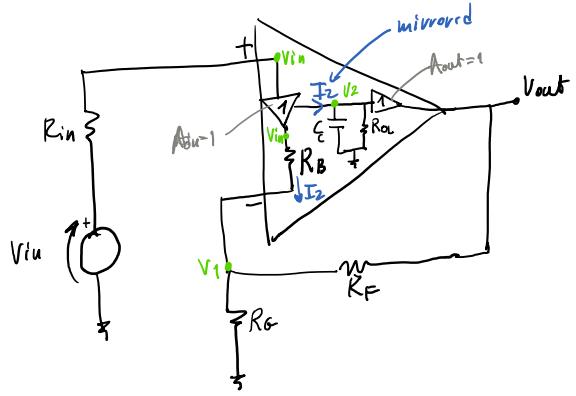
(not used in LNA → repeated switching creates disturbances)

Operation to cancel out the offset Vos:

- close A → Vos on capacitor
- close B → Vos cancel out

CFA

CFA = Current Feedback Amplifier



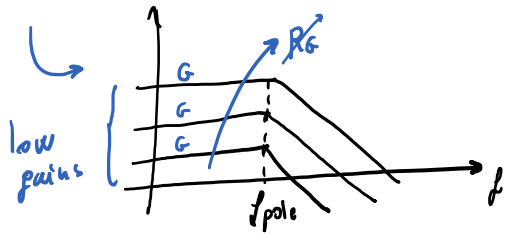
$$I_2 = \frac{V_{in}-V_1}{R_B} = \frac{V_1}{R_G} + \frac{V_1 - V_{out}}{R_F}$$

$$I_2 = \frac{V_2}{R_{OL}}\left(1+s C_c R_{OL}\right) = V_{out}\frac{(1+s C_c R_{OL})}{R_{OL}}$$

$V_2 = \frac{V_{out}}{A_{out}} \cong V_{out}$ ← buffer $A_{out}=1$

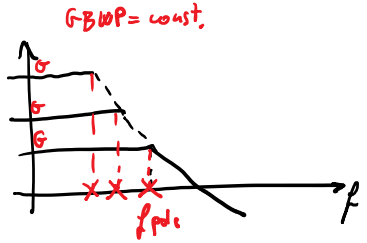
$$\dashrightarrow f_{pole} = \frac{A_{out}}{2\pi\left[R_F + \underbrace{\left(1+\frac{R_F}{R_G}\right)}_{G} R_B\right] C_c}$$

- At LOW GAIN ($G \ll \frac{R_F}{R_B}$) → $f_{pole} = \frac{1}{2\pi R_F C_c}$ → doesn't depend on gain (R_G varying)
  - ↳ $\beta \propto R_F$ (not on R_G)

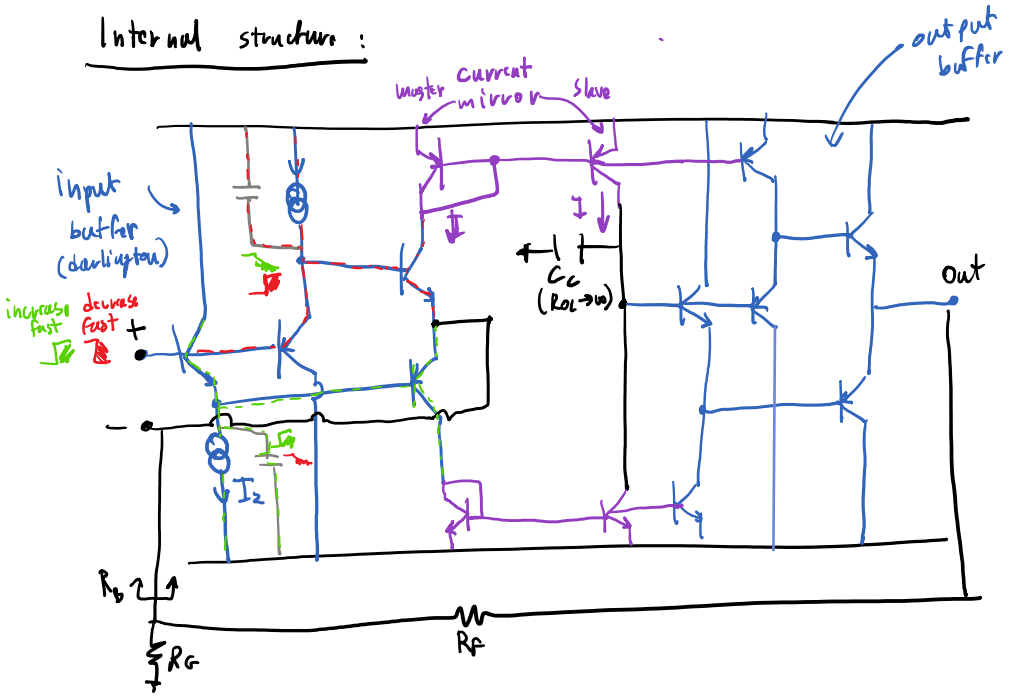


- At HIGH GAIN ($G \gg \frac{R_F}{R_B}$) → $f_{pole} = \frac{1}{2\pi G R_B C_c}$ → $GBWP = f_{pole}\cdot G = \frac{1}{2\pi R_B C_c} = \text{const}$

LIKE VOA



Internal structure:



$$SR = \left.\frac{dV}{dt}\right|_{max} = \frac{I_{max}}{C_c} \cong \frac{V_{step}}{R_F C_c}$$

Notes:
- To speed up the circuit we can use double emitter BJTs
- To reduce offset add transistors (e.g. diodes)

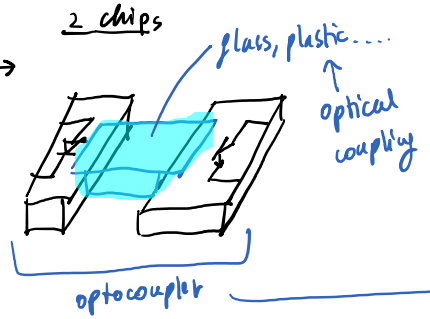
Pro:
- GBWP ≠ const. (for low gain)
- improve offset and SR

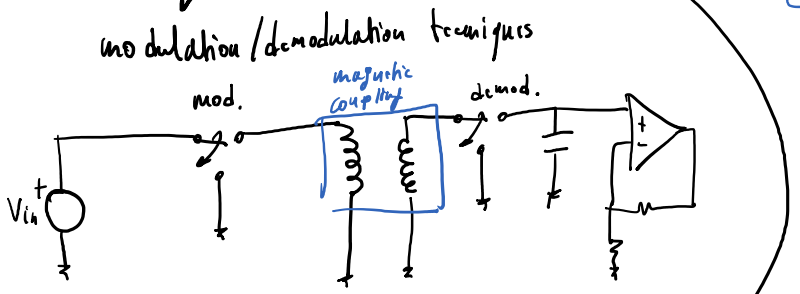
Cons:
- errors that can be comp. via proper circuits:
  - temp. offsets
  - SR due to slow dyn.
  - current mirrors can be i mismatch
  - criss-cross can be used
  - ....

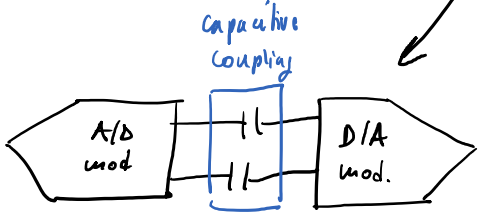
ISO

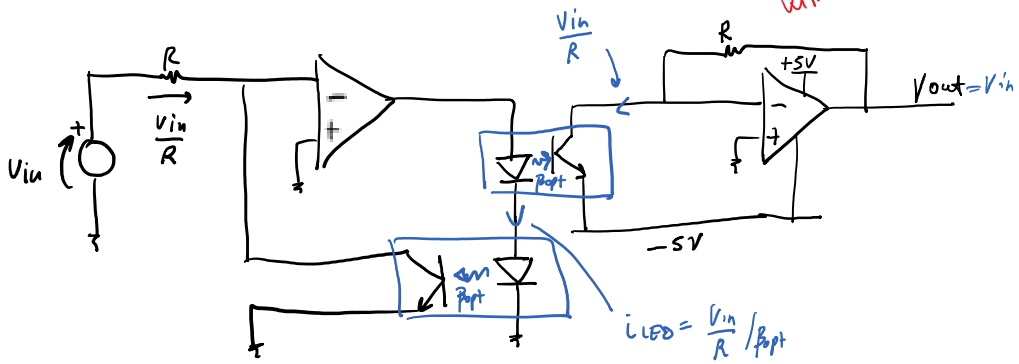
ISO = Isolation A lifier

Type of isolation:
- optical → most common →
- magnetic
- capacitive

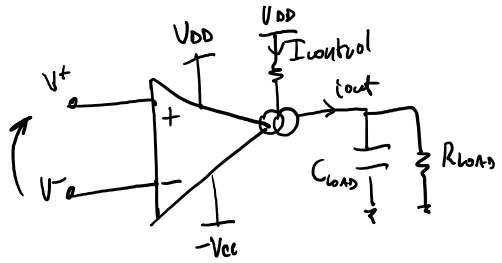








OTA

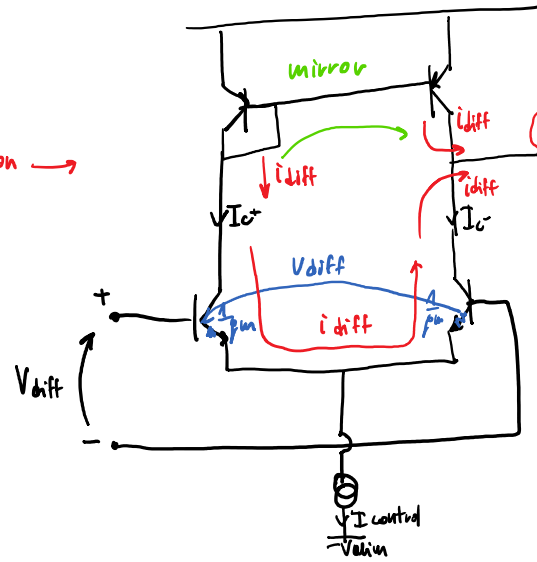


Pro:
- all low-impedance nodes
- wide BW → $f_p = \frac{1}{2\pi C_{LOAD} R_{LOAD}}$

Cons:
- no infinite gain
- no virtual ground
- it is used open-loop
- strong non-linearity

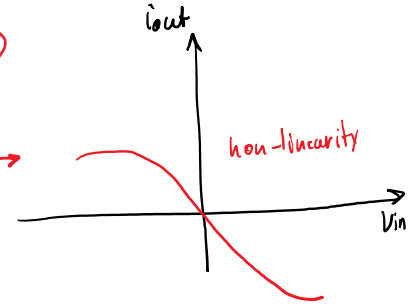
Internal Architecture

without linearization →



$i_{OUT} = 2 i_{diff} = \frac{2}{\frac{2}{g_m}} V_{diff} = G_m V_{diff}$

$G_m = \frac{I_{control}/2}{25mV}$



with linearization diodes →

Translinear principle

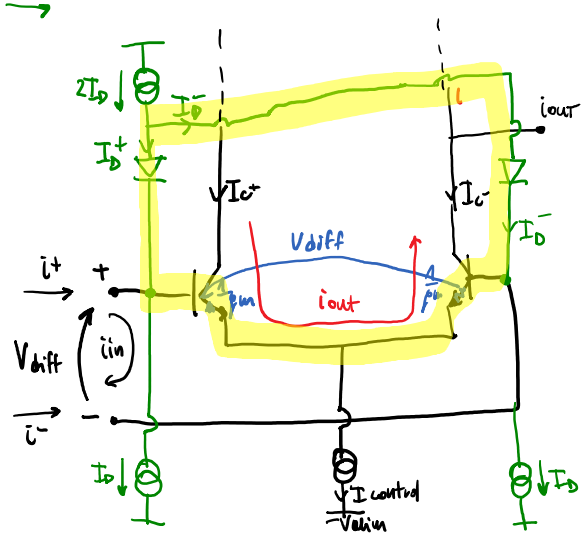
$I_D^+ I_C^+ = I_D^- I_C^-$

$$\begin{cases} I_D^+ = I_D - I_{in} \\ I_D^- = I_D + I_{in} \end{cases}$$

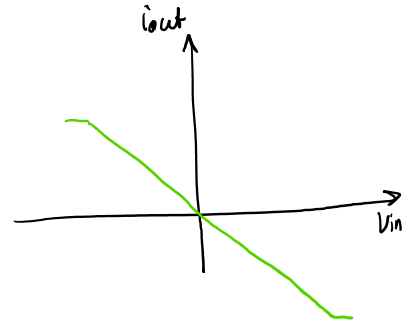
$(I_D - I_{in}) I_C^+ = (I_D + I_{in}) I_C^-$

$I_D (\underbrace{I_C^+ - I_C^-}_{i_{out}}) = I_{in} (\underbrace{I_C^+ + I_C^-}_{I_{control}})$

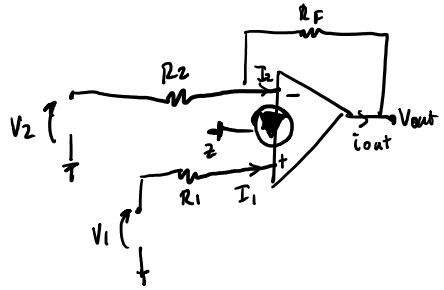
$\hookrightarrow i_{out} = \frac{I_{control}}{I_D} I_{in}$



linearization →



NORTON



$I_1 = \frac{V_1}{R_1}$ $\quad I_2 = \frac{V_2}{R_2} + I_{out}$

$I_{out} = \frac{V_{out}}{R_F}$ $\quad I_{out} = A_i (I_1 - I_2) = A_i \left(\frac{V_1}{R_1} - \frac{V_2}{R_2} - I_{out} \right)$

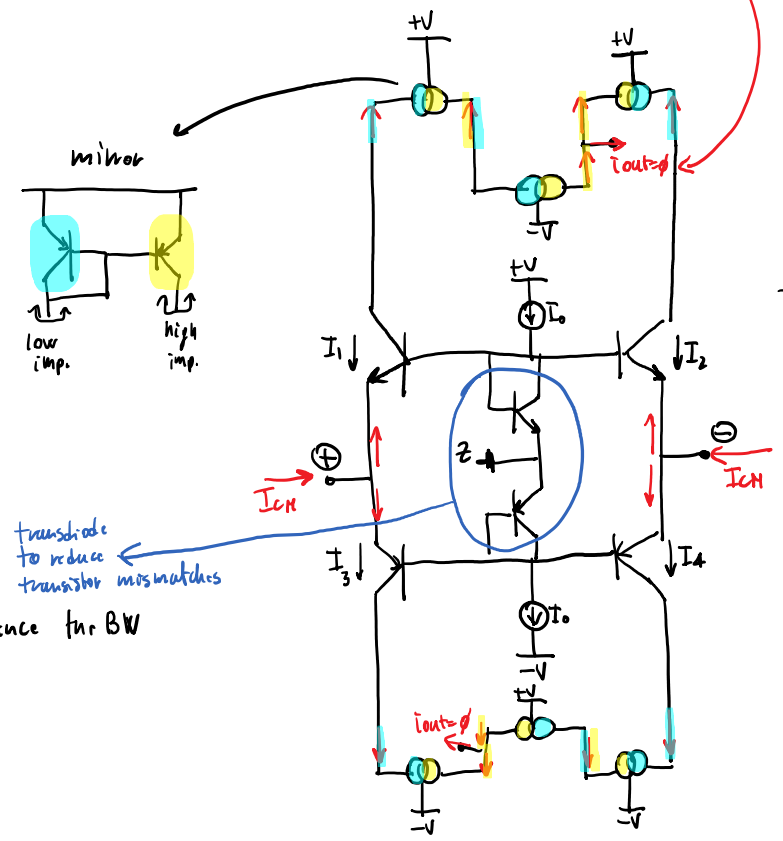
$\hookrightarrow I_{out} = \frac{A_i}{1+A_i} \left(\frac{V_1}{R_1} - \frac{V_2}{R_2} \right)$

$V_{out} = \frac{A_i}{1+A_i} \left(V_1 \frac{R_F}{R_1} - V_2 \frac{R_F}{R_2} \right)$

Pros:
- It is able to read current inputs
- all nodes have low impedance → parasitic C don't influence the BW
- very high BW (independent from closed-loop gain)

Cons:
- Finite and usually small A_i → No ideal gain behaviour
- Gain depends on external load

Internal Architecture



$I_1 = I_2 = I_o - I_{CM}/2$

$I_3 = I_4 = I_o + I_{cm}/2$

Translinear Principle

$I_1 \cdot I_3 = I_o \cdot I_o$

$I_2 \cdot I_4 = I_o \cdot I_o^2$

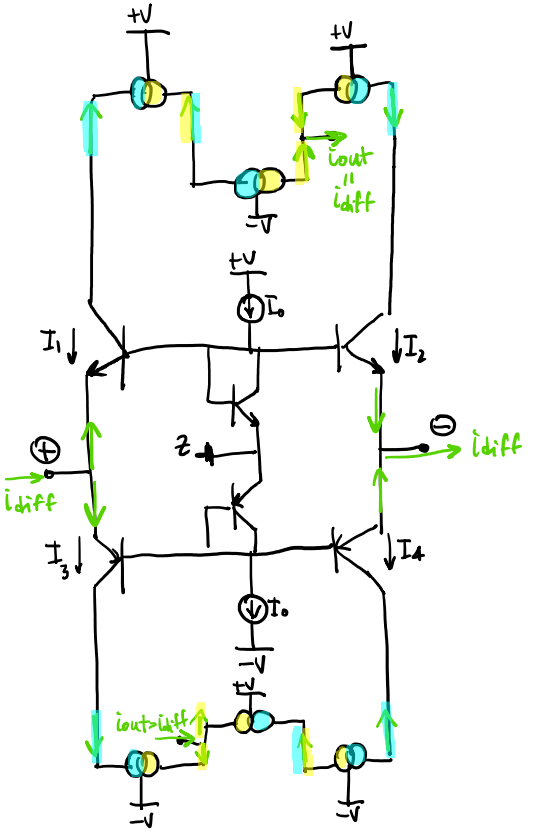
$\downarrow$

$I_1 I_3 = I_2 I_4$

$\parallel$

I_o^2

Differential signal

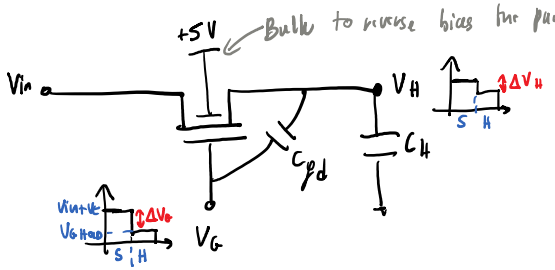


$I_1 = I_4 = I_o - I_{diff}/2$

$I_2 = I_3 = I_o + I_{diff}/2$

S/H: errors

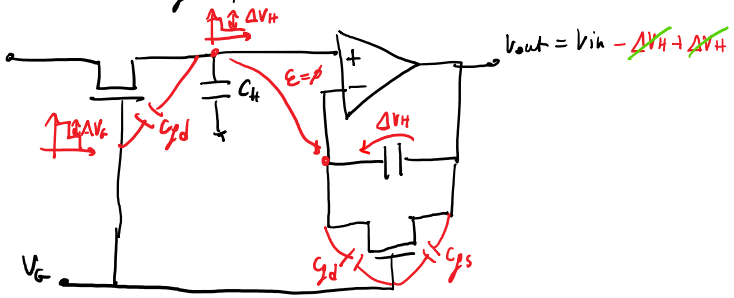
- **Charge injection**



→ When switch open we have a charge injection due to parasitic capacitance Cgd (error ∝ offset)

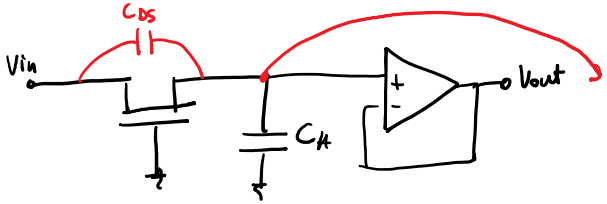
$$\Delta V_H = \Delta V_G \frac{C_{gd}}{C_{gd}+C_H}$$

↳ compensation:



- **Aperture induce non-lin.** → Actually charge injection is not const. (not offset but non-lin.)
  ↳ it depends on Vin ⇒ $\Delta V_G|_{max} = V_{in}|_{max} + V_t - V_{G\,Hold}$

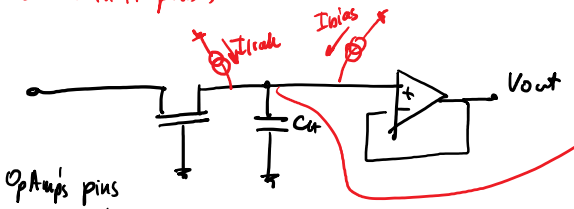
- **Signal feedthrough**



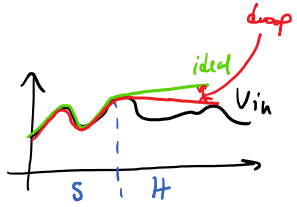
$$V_{feed} = \Delta V_{in} \frac{C_{OS}}{C_{OS}+C_H}$$

(perturbation in H phase)

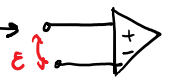
- **Droop**: C_H discharge during H phase due to I_{leak} (MOS) and I_{bias} (OpAmp)



$$\Delta V_H = \frac{I_{leak}+I_{bias}}{C_H} t_{droop}$$

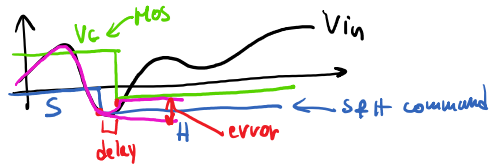


- **Buffer induced non-lin.**: Due to residual voltage difference ε bw the two OpAmp's pins

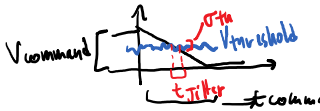


make sure $A_0 > \frac{V_{out,max}}{\varepsilon}$

- **Aperture-delay time**: Due to propagation of the control command
  ↳ the actual opening of the switch (MOS) will have a delay wrt S&H command →

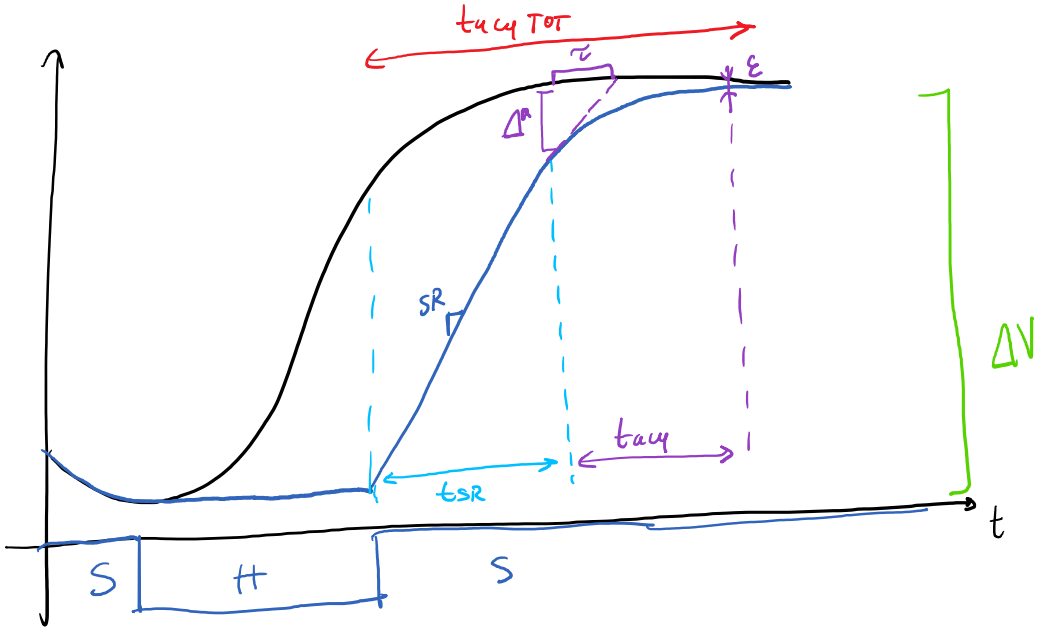


- **Aperture time jitter**: Actually aperture delay is not deterministic because of noise → fluctuations



$$t_{Jitter} = \frac{\sigma_{Vth}}{\frac{V_{command}}{t_{command}}}$$

S/H: Acquisition time



$t_{acq\,TOT} = t_{SR} + t_{acq}$

1 SR
- $SR = \frac{dV_{out}}{dt}$
- $\left.\frac{dV_{out}}{dt}\right|_{max} = \frac{I_{out\,max}}{C}$

→ choose min

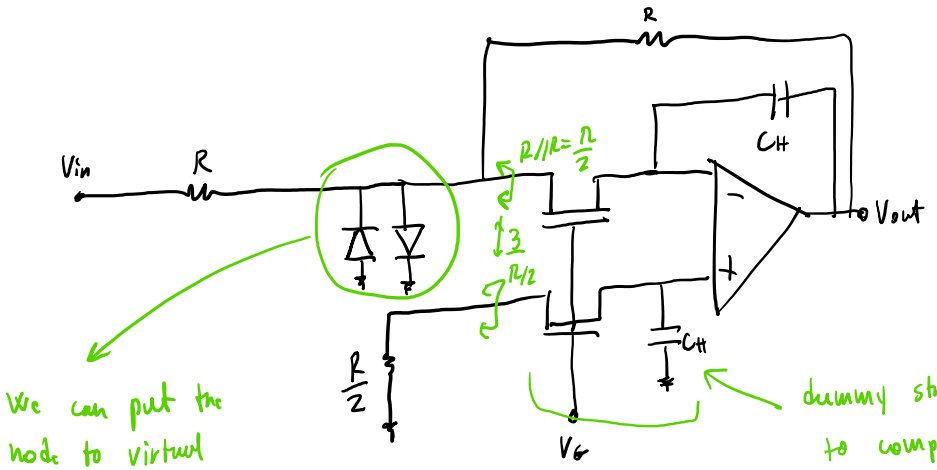
↳ $t_{SR} = \frac{\Delta V - \Delta^+}{SR}$

$SR = \frac{\Delta^+}{\tau} \rightarrow \tau = \frac{\Delta^+}{SR}$

2 Exponential charge

$t_{acq} = \tau \ln \frac{\Delta^+}{\varepsilon}$

S/H: simple driving

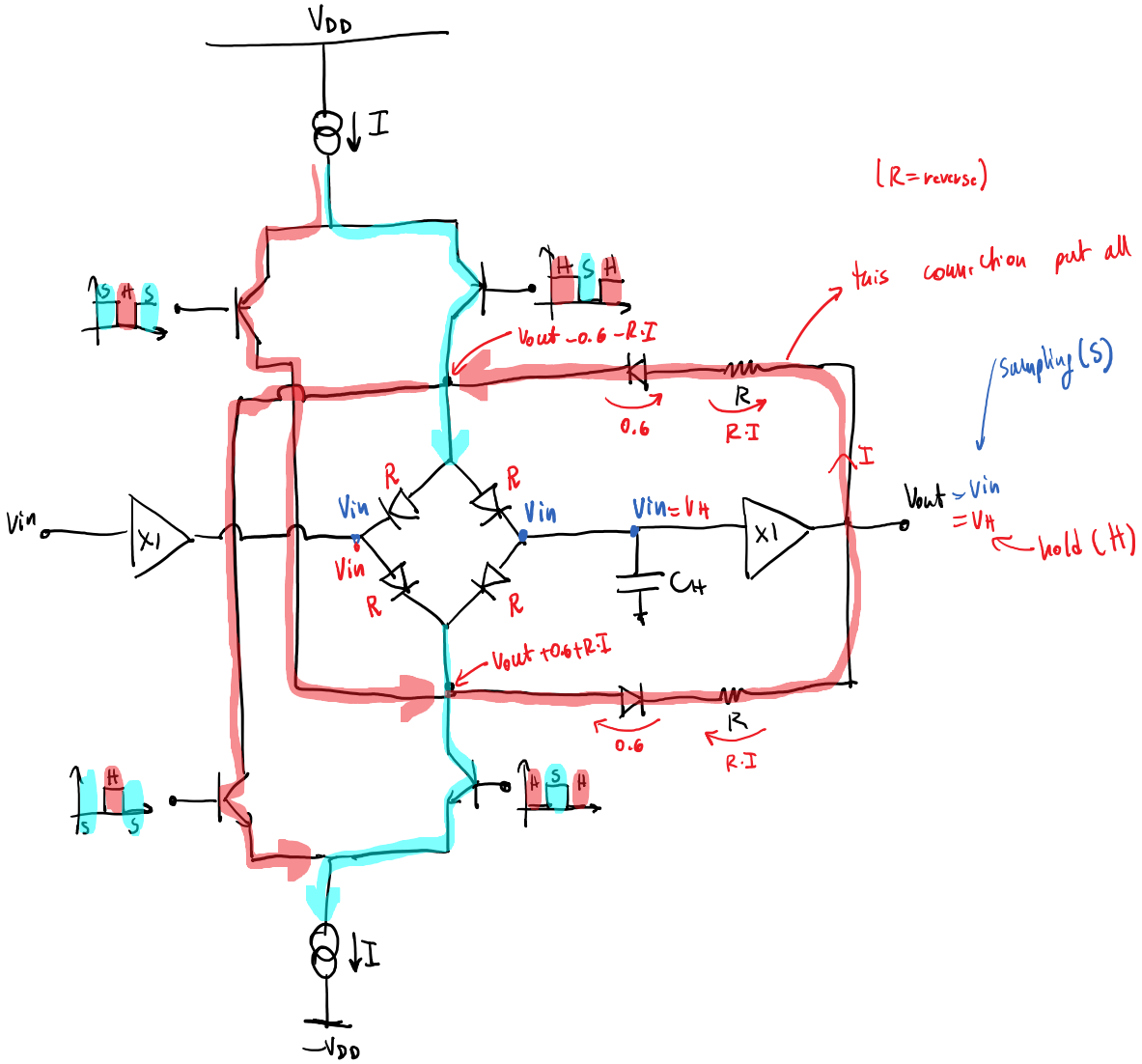


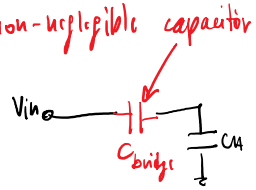
We can put the node to virtual ground when nMOS ON and that voltage is always ∈ [−0.6 ÷ 0.6 V]
↳ ΔV_G excursion is small and const → 1

dummy structure to compensate → 2 charge injection

Pro: 1. V_G simple CMOS levels (0 ÷ 3.3 V), indep. from Vin
2. reduction of Aperture induced non-lin.
3. compensates bias currents effects

S/H: fast switching





Pros:

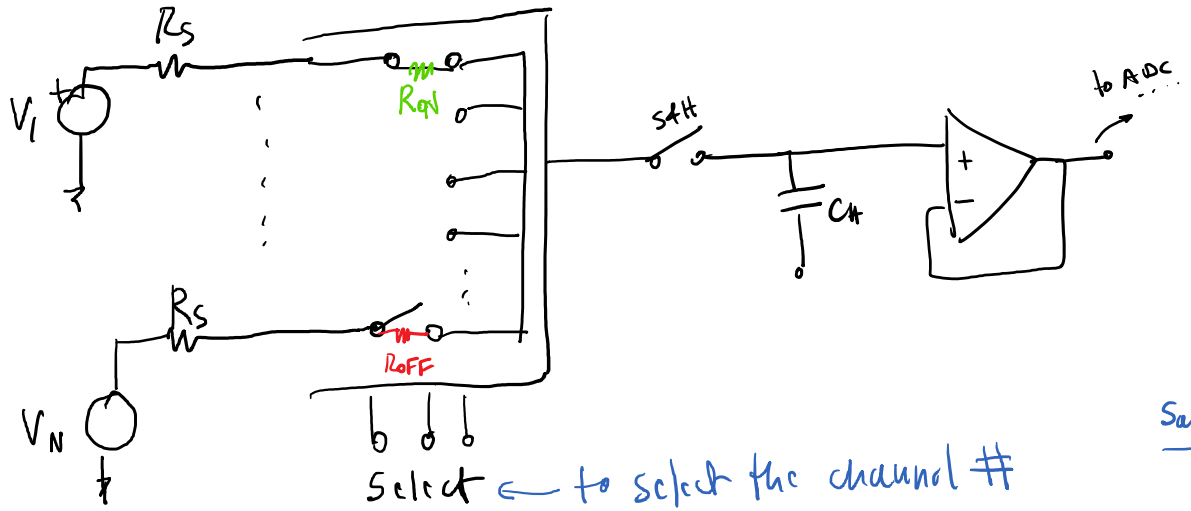
- very fast switch with diodes

Cons:

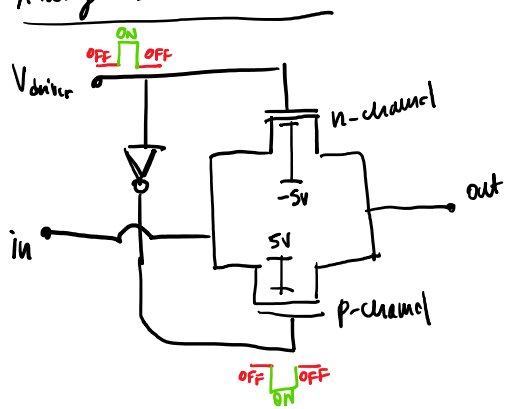
- mismatches bw components → error on V_H
- synchronization is needed bw bipolar S&H command signals

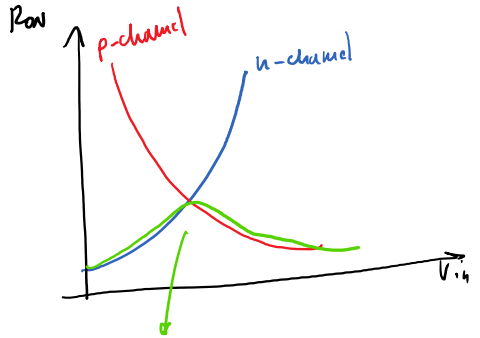
MUX

Multiplexer = acquire analog signals from various sources (channels) and process them by means of a single digital process



Analog switch for MUX: Pass-transistor





Sampling time: $t_{acq|min} = \tau_{max} \ln \frac{\Delta_{max}}{\varepsilon_{max}}$

$\tau_{max} = \left[(R_{S|max} + R_{ON|max}) \,//\, \frac{R_{OFF} + R_S}{N-1} \right] C(1+tol_{max})$

Hold time: max bw $\begin{cases} I_{OFF} = (N+1) I_{leak} + I_{bias} \\ I_{OFF} = \frac{V_{in|max}}{\frac{R_{OFF|min} + R_{S|min}}{N-1}} \end{cases} \rightarrow t_{HOLD} = \frac{q\,\varepsilon_{in}}{\frac{I_{OFF}}{C_{H|min}}}$

$f_{channel}|_{max} = \frac{f_{s\,max}}{N}$ → Shannon $f_{in,max} = \frac{f_{channel,max}}{2}$ (for each channel)

↳ Scanning for channel with wider BW:

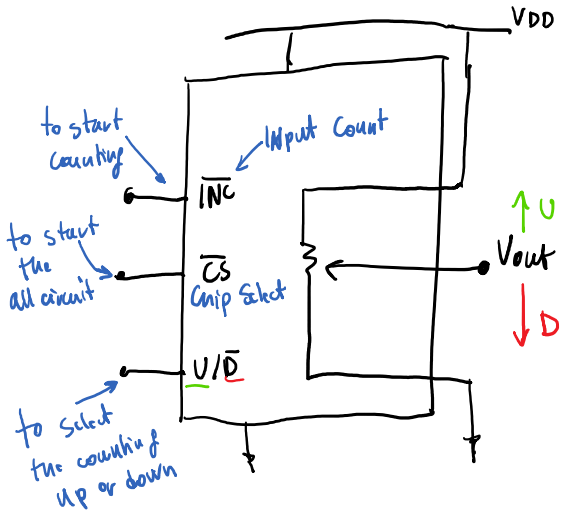
N = # channels
K = # priority wide BW channels

$f_{s,H} = \frac{f_{s\,max}}{K+1}$ $f_{s,N-K} = \frac{f_{s\,max}}{(K+1)(N-K)}$

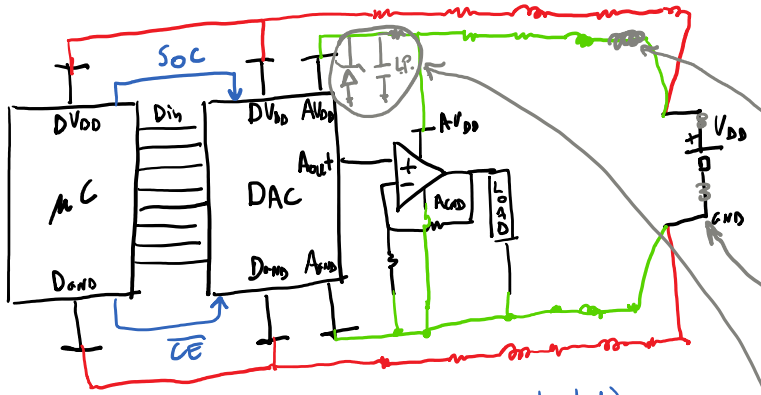
↳ Sampling freq. $T_S = t_{acq|min} + t_{HOLD}$ $f_{s|max} = \frac{1}{T_S}$ ← (throughput)

DigPot

Dig Pot = Digital Potentiometer



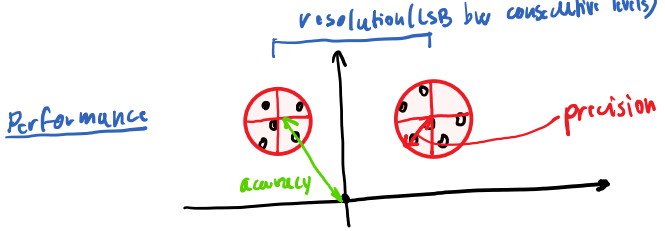
DAC



→ To avoid that the digital and analog part induce disturbances bw eachother it's better to separate the P.S.

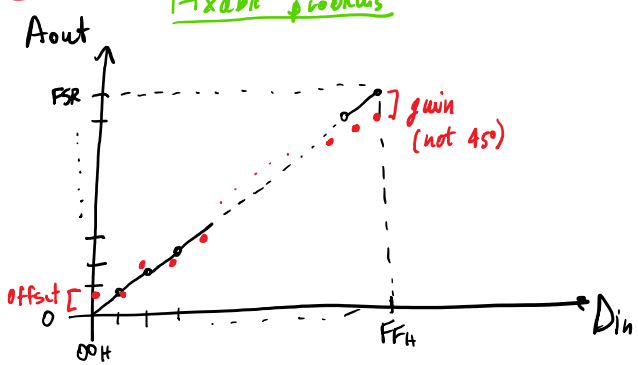
put a low value inductance  to avoid high freq. fluctuations caused by the big inductances of the P.S.

- Can put a diode to fix the voltage in case of variable battery (Also on digital part and Vref)
- can put a L.P. filter to filter out any dist.

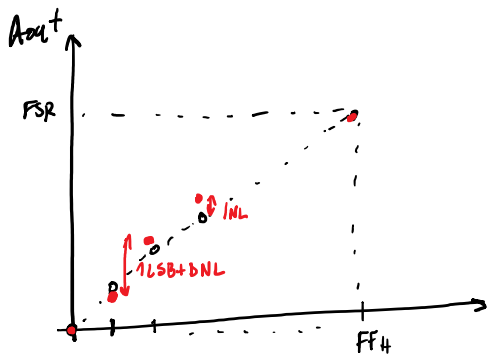


Errors

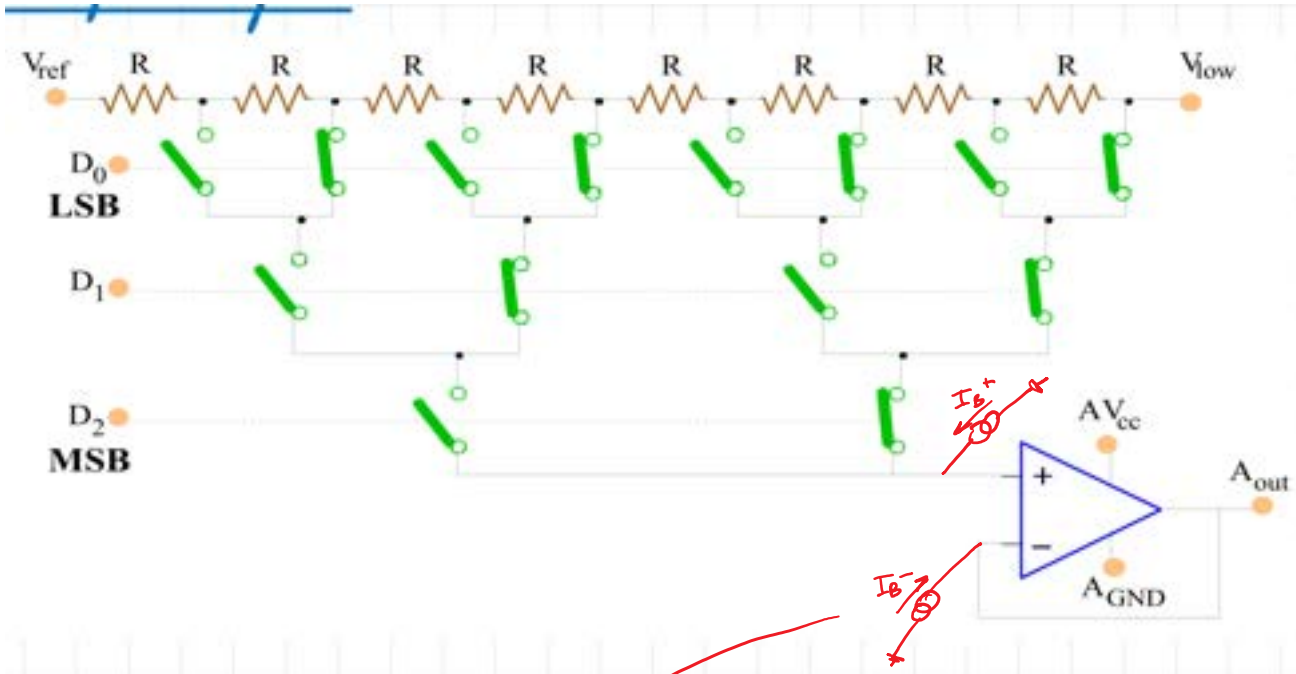
Fixable problems



Non-linear errors



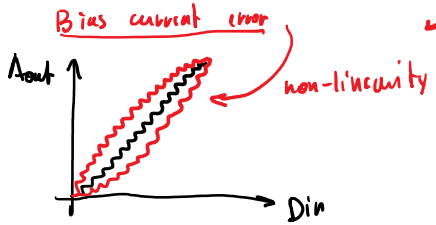
DAC: Voltage scaling DAC



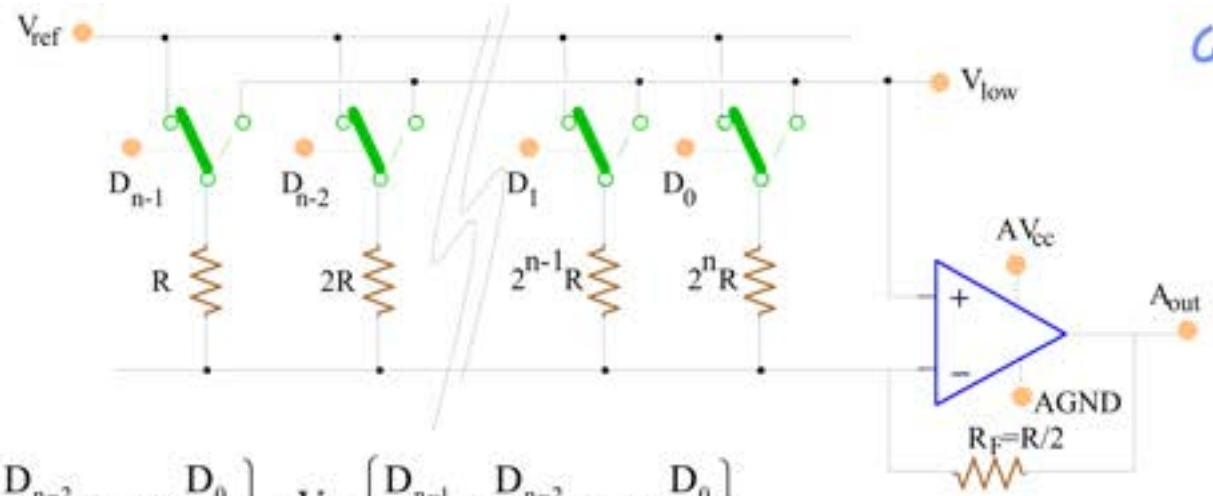
Components:
- 2^n Resistors → divide FSR in 2^n voltage level
- 2^{n+2} MOS → allow to properly select the levels
- Op Amp

Pros:
- easy scalability of all resistors
- MOS switching efficient and less expensive that A. MUX

Cons:
- large # resistors and transistors → too much space
- I_B and I_{leak} cause non-lin.
  - I_B ↓ OA
  - I_{leak} ↓ MOS



DAC: Weighted-R DAC



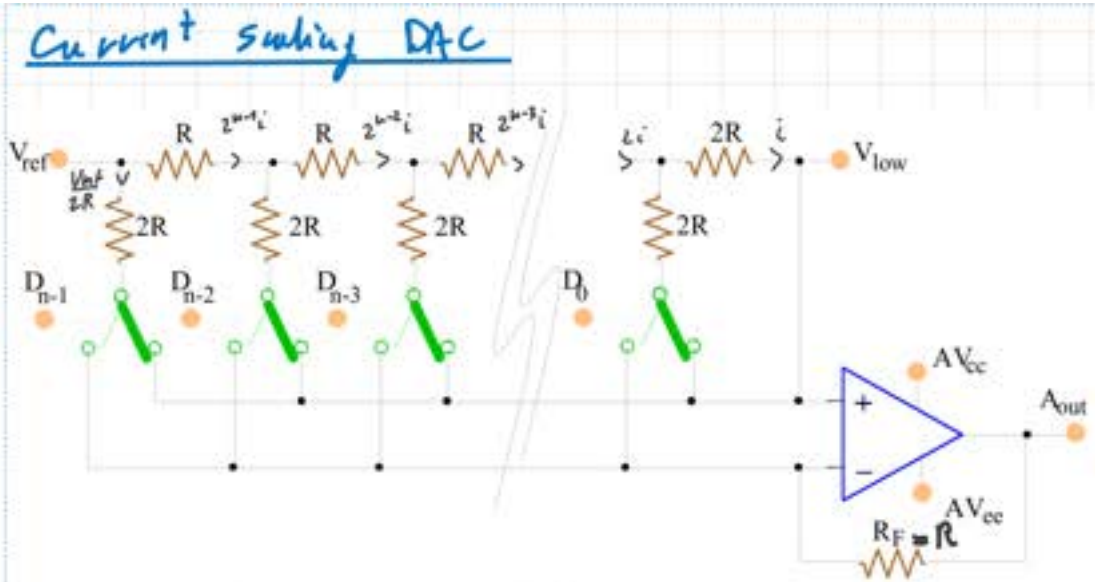
$$v_{out} = V_{ref}\frac{R_f}{R}\left\{\frac{D_{n-1}}{1}+\frac{D_{n-2}}{2}+\ldots+\frac{D_0}{2^{n-1}}\right\} = V_{ref}\left\{\frac{D_{n-1}}{2}+\frac{D_{n-2}}{2^2}+\ldots+\frac{D_0}{2^n}\right\}$$

Components:
- >n resistors → voltage levels
- 2n p/n-MOS
- OpAmp

Pros:
- simplest converter

Cons:
- different R values + tolerances
- voltage drop on R_{ON}, R_S
- variable current consumption
- large silicon area
- I_{bias} errors

DAC: Current scaling (Ladder R-2R) DAC



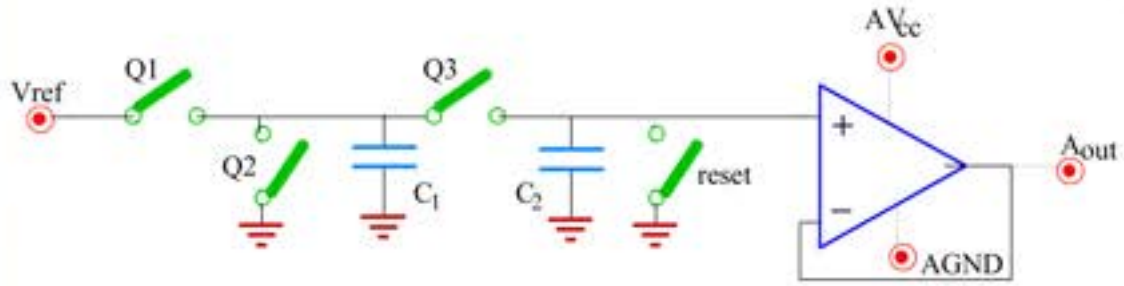
components:
- 3n resistors → current divider
- 2n nos → switches low levels
- Op Amp

Pros:
- easy scalability of resistors
- easy drive of nos switches → R_{ON} creates a const. offset (can be compensated)

Cons:
- bias currents errors

DAC: Serial input DAC

Serial input DAC



Components: • only 2 capacitors → For store (C_1) and sharing (C_2) the bit value

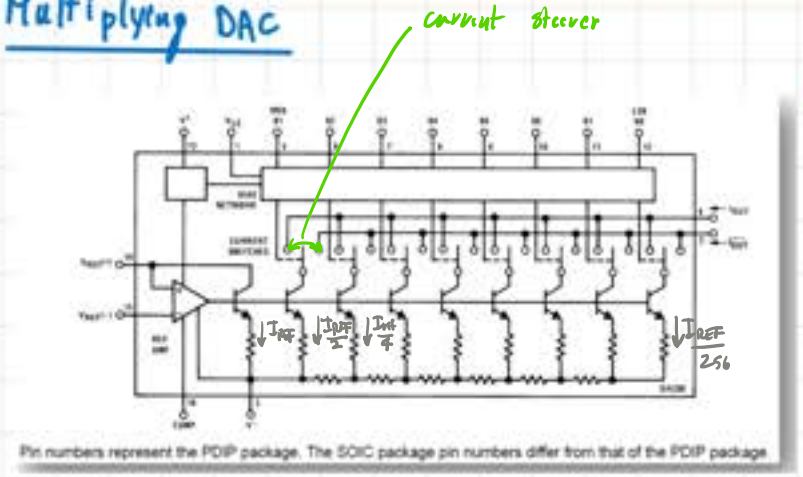
• 5 MOS → close/open to activate store/share logics

Pros: • Extremely compact and easy

Cons: • individual bits are provided sequentially (serially) → SLOW

DAC: Multiplying DAC

Multiplying DAC



Components:
- ~2n resistors
- ~n mirrors + n switches (current steerer) → to provide $\overline{I_{out}}$, I_{out}
- OpAmp → to vary V_{ref}

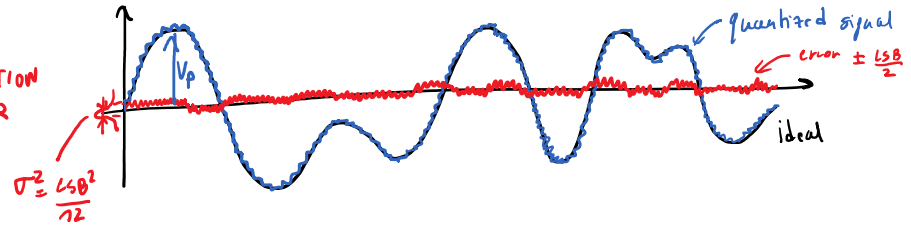
$$I_{out} = \frac{V_{ref}}{R_{ref}} \cdot \frac{D_{in}}{2^n}$$ (multiplying; $\frac{V_{ref}}{R_{ref}}$ variable, $\frac{D_{in}}{2^n}$ variable)

$$I_{out} + \overline{I_{out}} = I_{FS} = \frac{V_{ref}}{R_{ref}} \frac{255}{256}$$ (full scale)

Pros:
- We can vary V_{ref} in addition to D_{in}

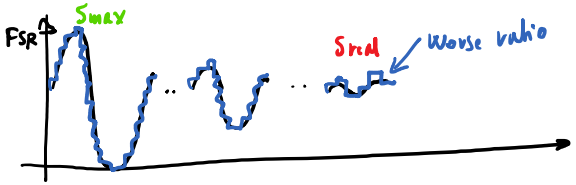
DAC: Noise analysis

- Din is quantized → Aout will be quantized → QUANTIZATION ERROR



$$\rightarrow SNR_{id} = \left.\frac{\left(\frac{V_p}{\sqrt{2}}\right)^2}{\frac{LSB^2}{12}}\right|_{dB}$$

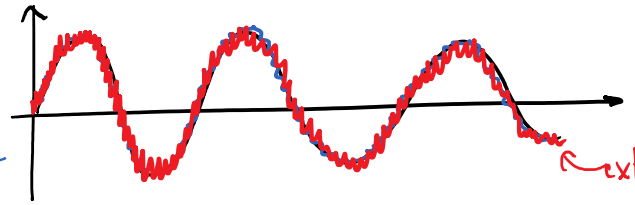
- Aout can also have bad amplification → worse ratio wrt quantization → AMPLIFICATION FACTOR



$$\rightarrow SNR_{tn} = SNR_{id} - \Delta S\,|_{dB}$$

$$\Delta S = \frac{S_{max}}{S_{real}}$$

- There can also be extra noise → EXTRA NOISE



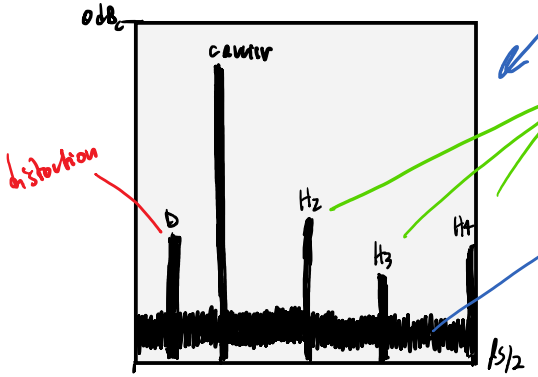
$$\rightarrow SNR_{real} = \frac{S_{real}}{N_{real}} = \frac{S_{id}\cdot\Delta S}{N_{quant}+\Delta N} = SNR_{id} - \Delta S - \Delta N\,|_{dB}$$

ep. bit:

$$\rightarrow ENOB = \frac{SNR_{real} - 1.76}{6.02}$$

Spectral performance

- S_{max} = 0 dBc ← carrier
- consider just $\frac{f_s}{2}$ and $\frac{N_{samples}}{2}$



after FFT → Harmonics

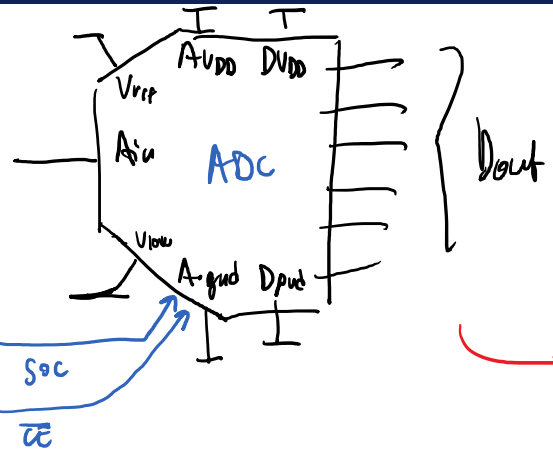
Noise floor = $\left.\frac{\text{noise}}{\frac{N_{samples}}{2}}\right|_{dBc}$

- Total Harmonic Distortion: $THD = \left.\frac{\text{power of all the harmonics}}{\text{power of useful signal}}\right|_{dB} = \frac{\sum H_i}{S_{real}}$ harm

- Signal to Noise and Distortion: $SINAD = \left.\frac{\text{power of useful signal}}{\text{tot - power of noise and harmonics}}\right|_{dB} = \frac{S_{real}}{N_{real}+D+\sum H_i}$

ADC

Analog to Digital converter = ADC

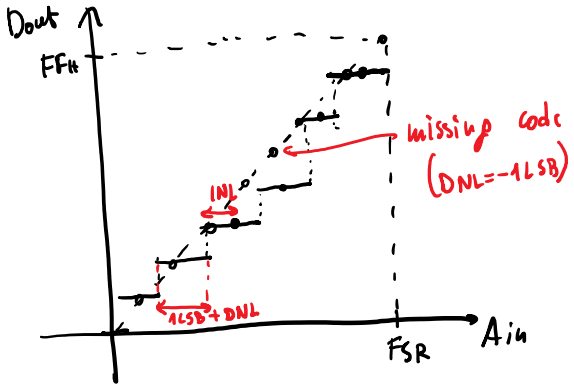


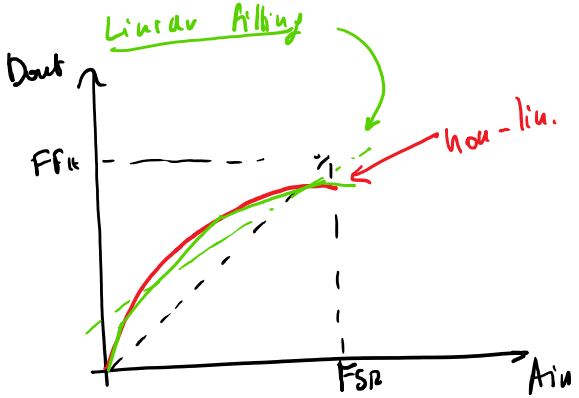
→ Compromise b/w cost of amplification stages and higher resolution ADCs to convert a small analog signal (proper conditioning based on signal, costs and requirements)

Errors

(offset, gain)

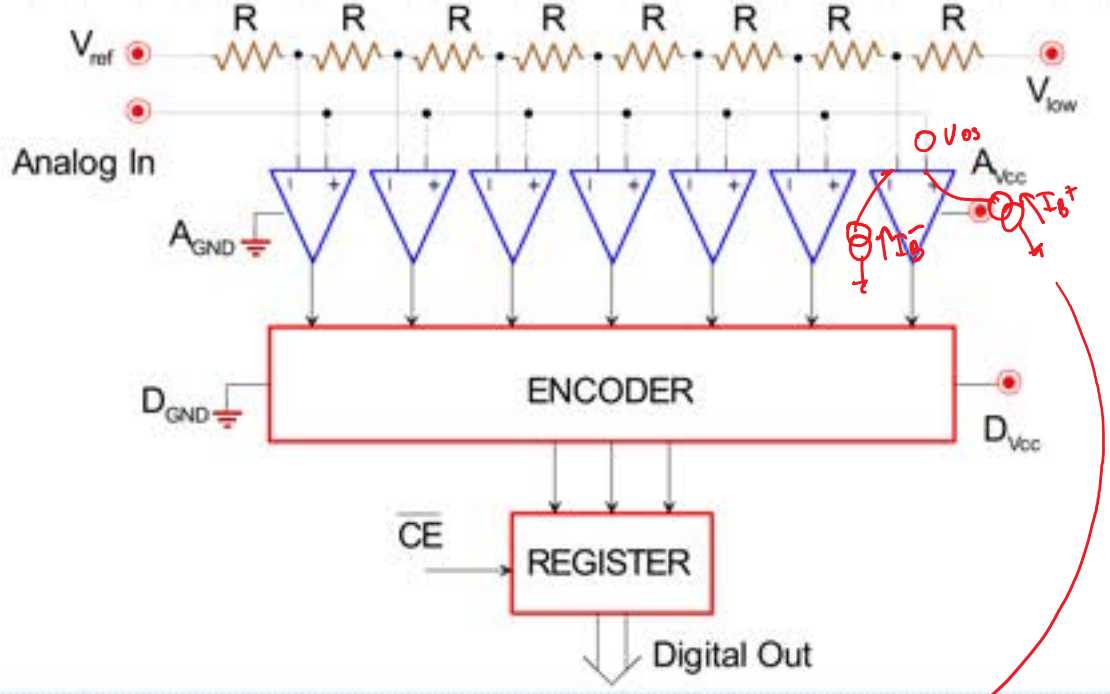
↳ Non-linear errors





ADC: Flash ADC

• Flash ADC



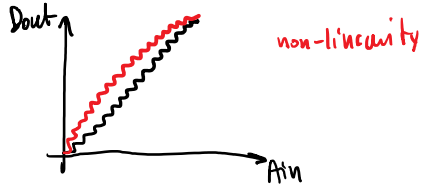
Components:
- 2^n resistors → to create 2^{n-1} quantization levels
- 2^n comparators → compares the q. levels with the input → H/L
- 1 encoder (thermometric code → binary code)
  - H/L → 0/1

Pros:
- very fast → parallel conversion
- simplicity

Cons:
- silicon area ↑ and power dissipation ↑ with n ↑
- bias and leakage currents, parasitic capacitors
  - lead to non-lin. of the ADC converter
- offset lead to incorrect switching
  - missing codes, non-monotonicity of ADC

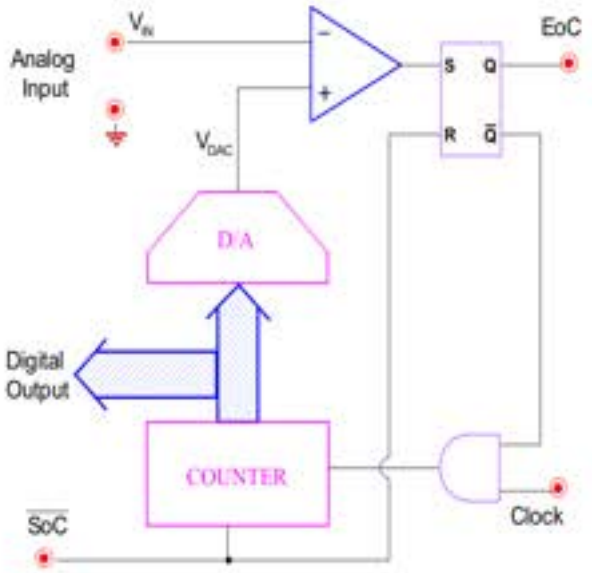
offset errors → for low value of LSB, offset can be comparable to a level and result in missing codes

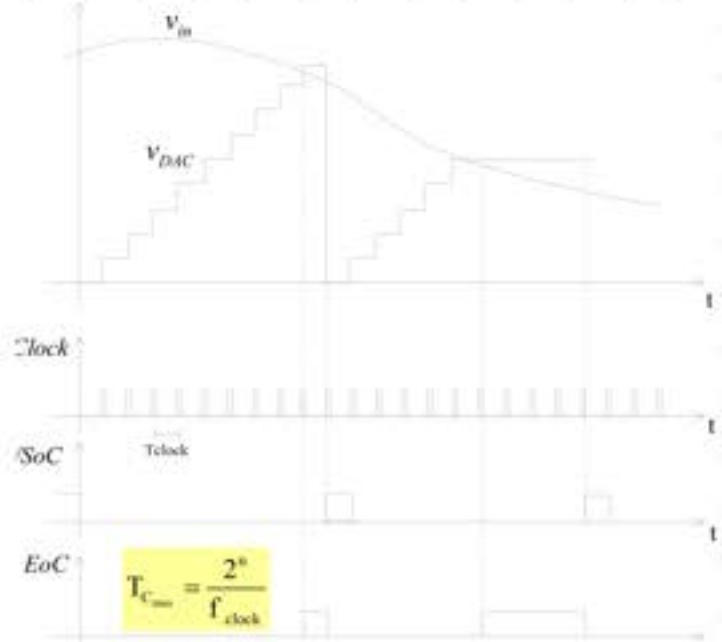
bias current errors → can change the comparator switching level and result in non-linearities



ADC: Staircase ADC

- Staircase ADC





Components:

- 1 Counter → subsequent adjustments via binary count
- 1 DAC → binary count $\xrightarrow{DAC}$ analog level to compare with Vin
- 1 comparator

Pros :

- precision depends on the DAC

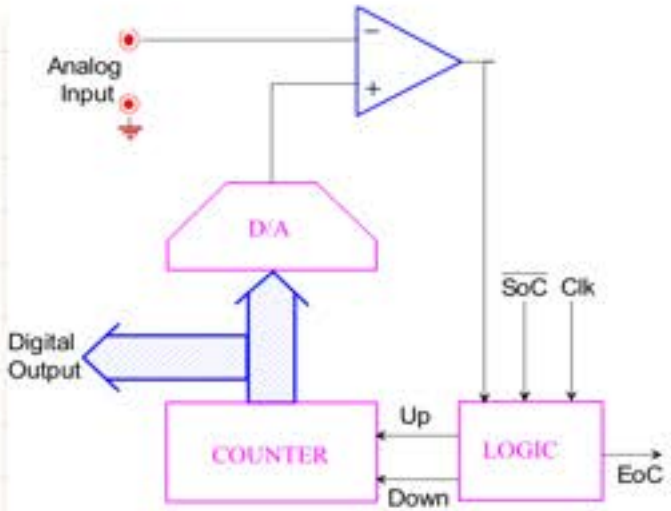
Cons :

- Conversion time depend on Vin
  - ↳ not very fast
  - ↳ sampling comb not of const. (not regular sampl. steps due to time dep. on Vin)

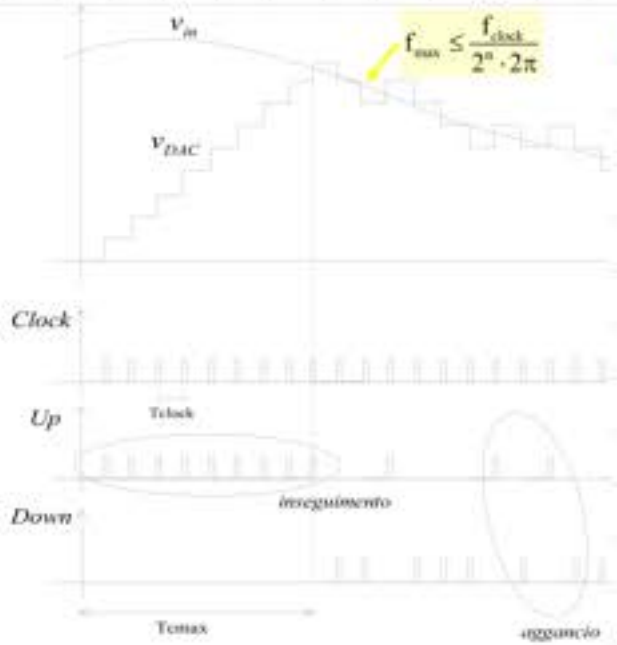
Converts in hold phase ← you can put a S&H ↳ regular before the ADC

ADC: Tracking ADC

Tracking ADC



Components: 1 DAC, 1 counter, 1 comparator, 1 up/down logic



Components:

- 1 Counter → subsequent adjustments via binary count
- 1 DAC → binary count $\xrightarrow{DAC}$ analog level to compare with Vin
- 1 comparator
- 1 up/down logic → to make the counter go up/down and "track" Vin

Pros:

- Fast → correct sample at every CLK
- precision depends on DAC
- Oversampling → use just one bit = Up/Down to stay hooked on input signal

(also called Δ modulator)

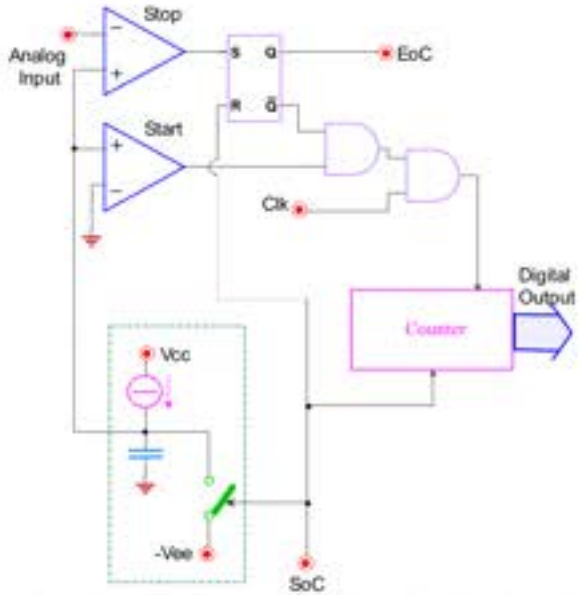
Cons:

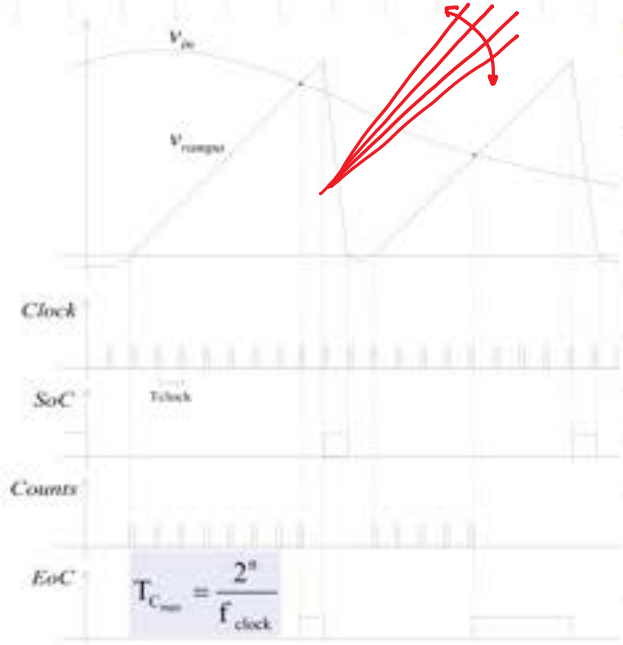
- frequency of signal $\gg f_{max}$
  - $f_{clk} \geq 2^n \pi f_{max}$

for high slope $\left.\frac{dV_{in}}{dt}\right|_{max} < \frac{LSB}{T_{clk}}$

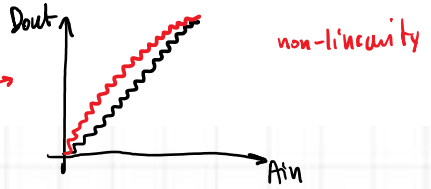
ADC: Single slope ADC

- Single-slope ADC





$\frac{dV}{dt} = \frac{I(1 \pm tol_I)}{C(1 \pm tol_C)}$



Components:
- const. current source → charges
- capacitor → linear charge → ramp
- comparator → ramp vs. Vin comparison
- counter → counts only after reaching Vin → digital output

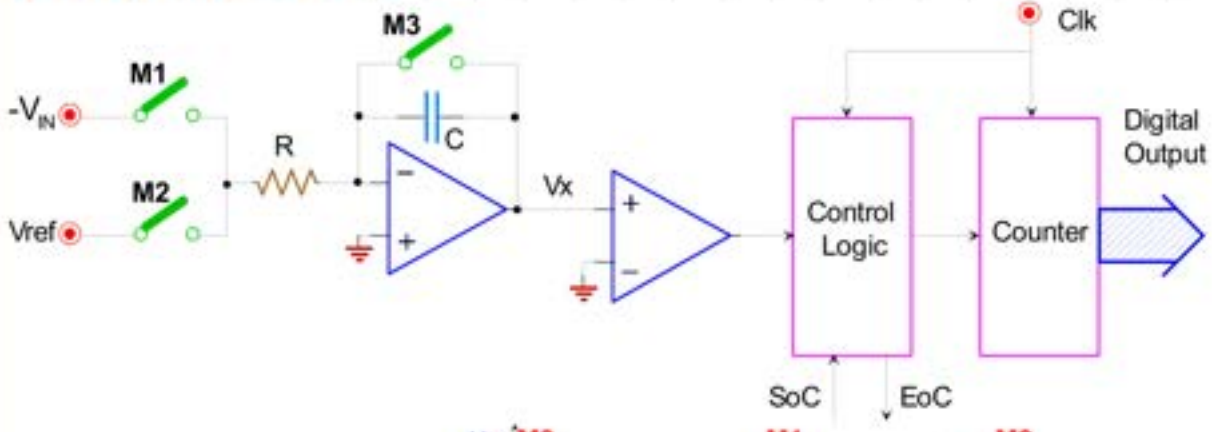
Pros:
- precision dependent on $\frac{dV}{dt} = \frac{I}{C}$ → I source, C component
- many bit ($n > 16$)

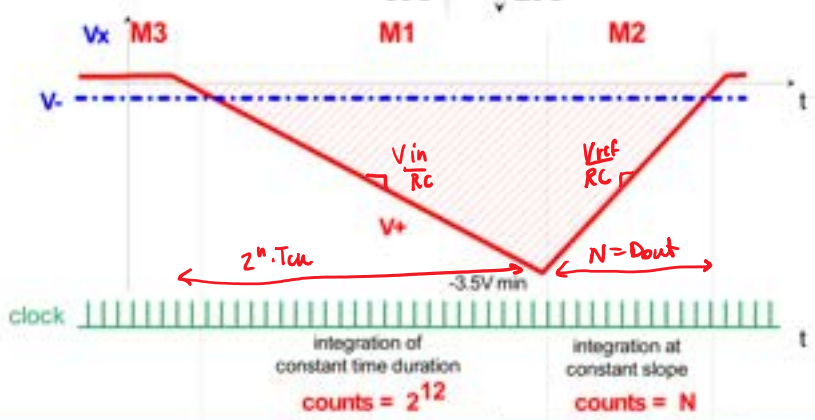
Cons:
- offset of comparator → make ramp start from slightly
- slow (like staircase problems)
- irregular sampling comb
- too sensitive to toll of C, I_{source}, CLK period
  - ↳ low conversion accuracy

better to use double ramp.

ADC: Dual slope ADC

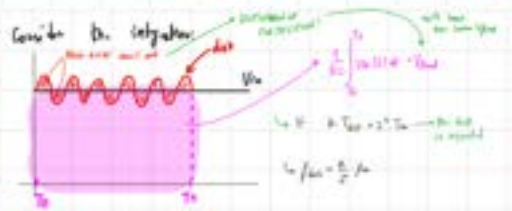
• Dual-slope ADC





↳ $\frac{V_{in}}{RC} \cdot 2^n T_{ck} = \frac{V_{ref}}{RC} \cdot D_{out} \cdot T_{ck}$

↳ $D_{out} = \frac{V_{in}}{V_{ref}} \cdot 2^n$



Components:

- integrating OpAmp → H1 (charge) → to obtain a ramp α -Vin (integration for 2^n CLK pulses)
  - discharge → M2 → to obtain a ramp from $\int V_{ref}$ (↑ const. (So const slope))
- Counter → count CLK pulses for integrations phases
- control logic → switches control / SoC / EoC
- comparator → detect when the value stored accross C is Ø again → $V_{ref} = V_{in}$

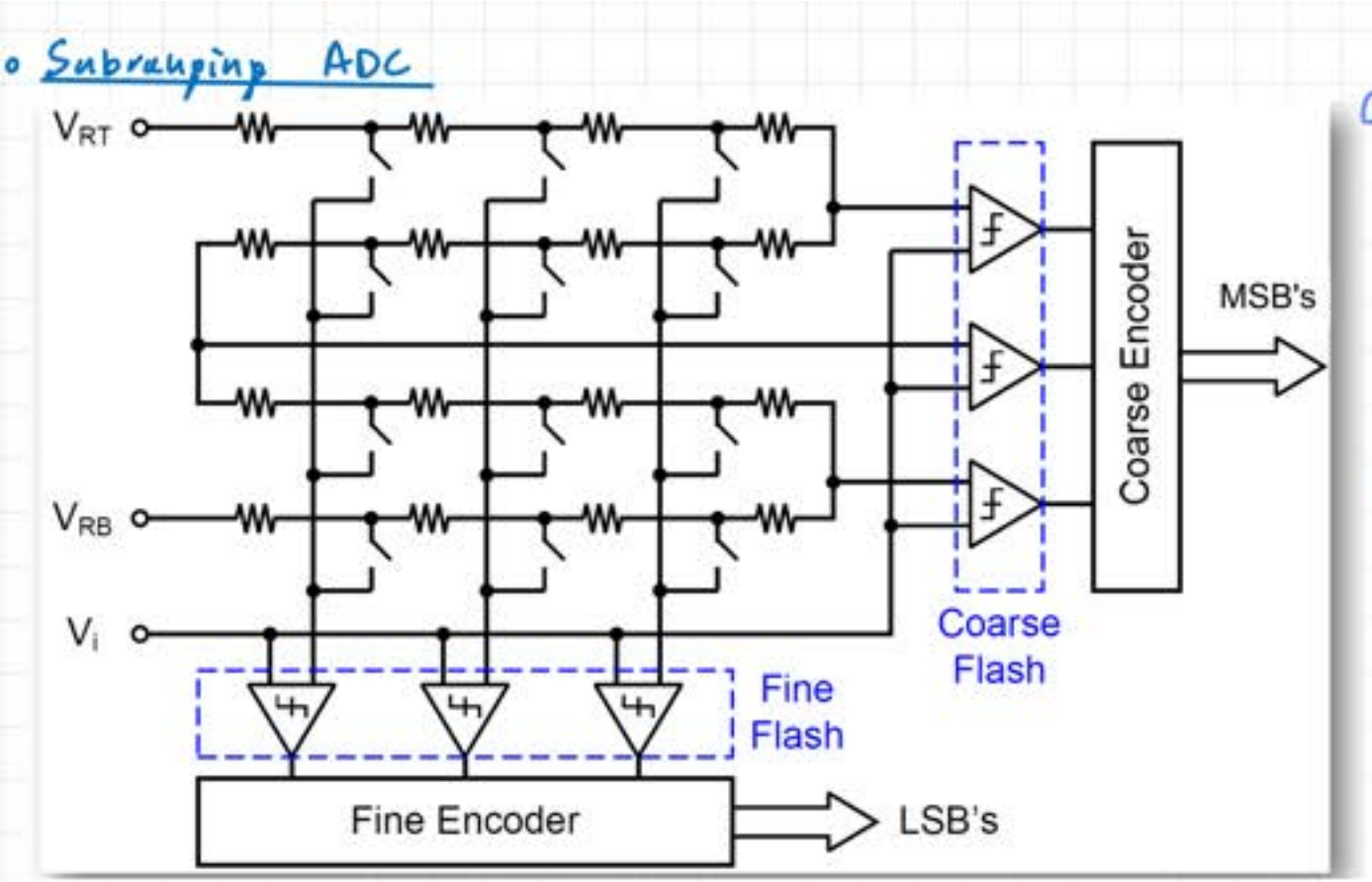
Pros:

- precision independent of R and C (their toll.)
  - ↳ both charge/discharge ramps with the same $\tau = RC$
- Disturbance rejection at freq = int. multiples of integration period
  - ↳ (NMR)

Cons:

- High conversion time → twice the one of Single-slope

Advanced ADC: Subranging ADC

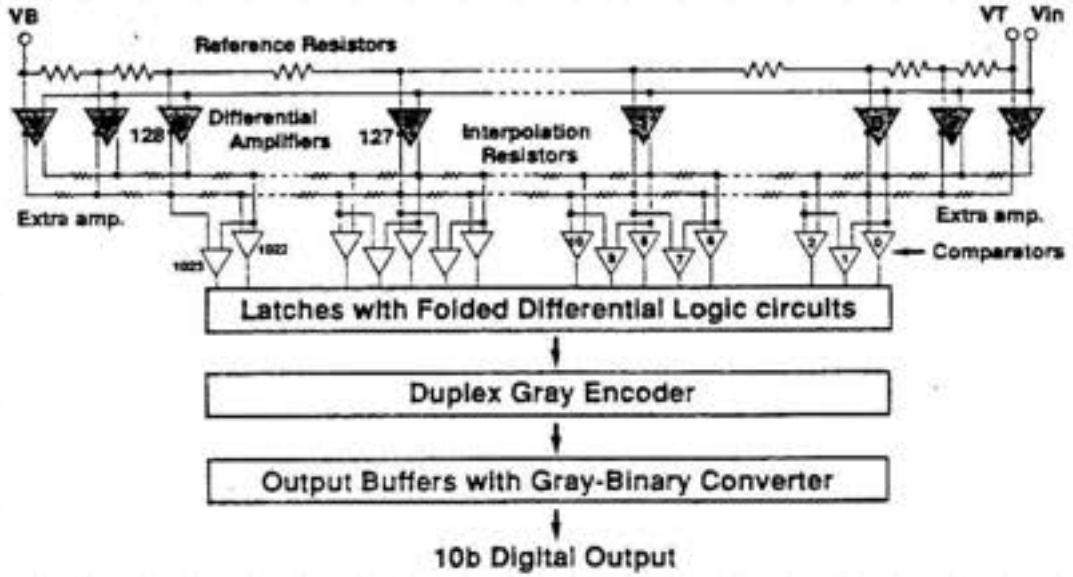


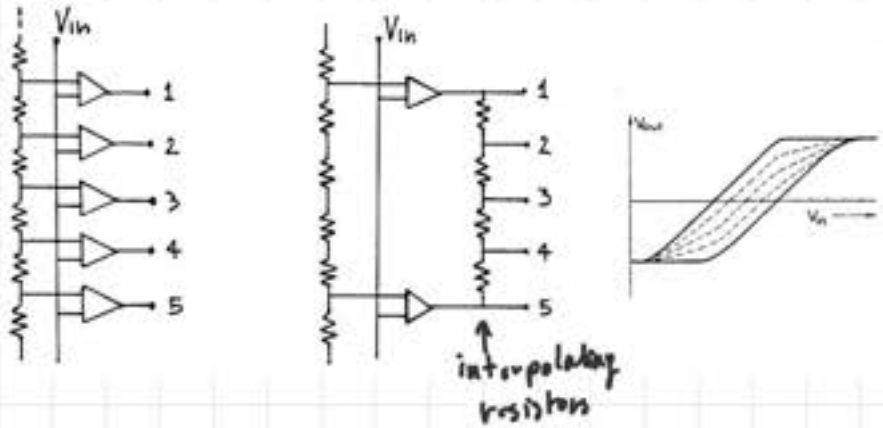
Components:
- resistors → less for coarse conversion
  - → create quantization levels
  - → more for fine conv.
- comparators → compare levels with Vin
- encoders → (thermometric → binary)

Pros:
- less waste of resources
  - when far from Vin → COARSE: less resolution
  - when near Vin → small range → FINE: more resolution

Advanced ADC: Interpolation Flash ADC

- Interpolation Flash-ADC





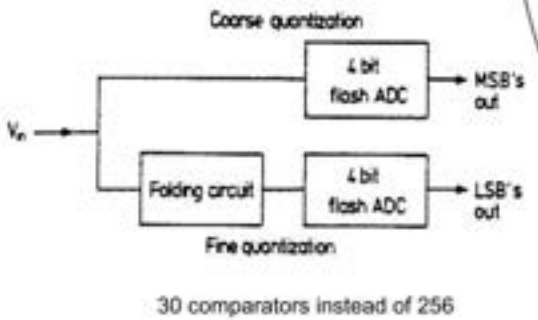
Components:
- resistors → reference
- interpolating → create levels from reference after comparison
- differential comparators → differential output

- latches with folded diff. logic circuit → sign of Vout
- Encoders

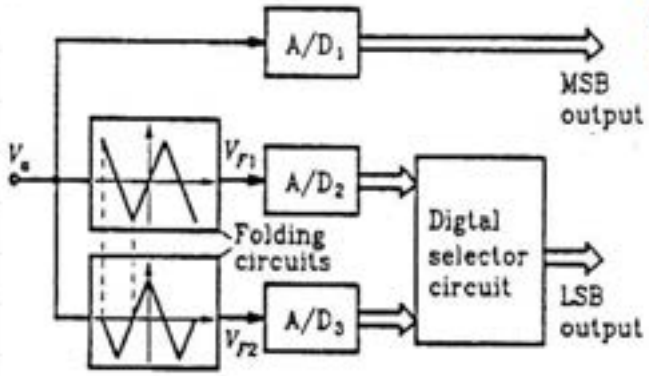
Pros:
- use less comparators without loosing levels
- huge reduction of silicon area, power dissipation, input stray C
- improved dynamic performances (settling time, speed...)

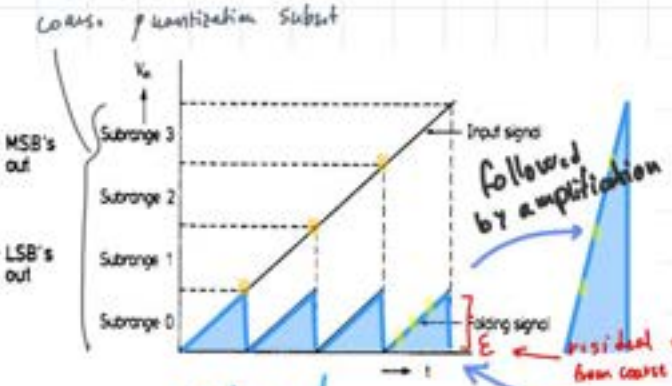
Advanced ADC: Folding Flash ADC

• Folding Flash-ADC

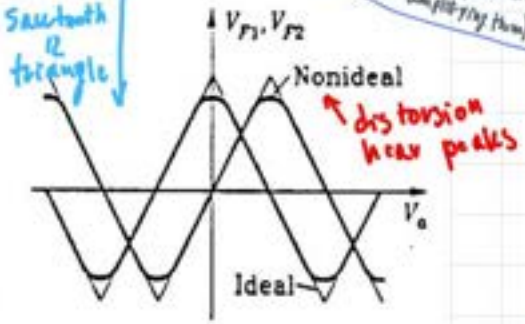


30 comparators instead of 256





not actually sawtooth or triangle

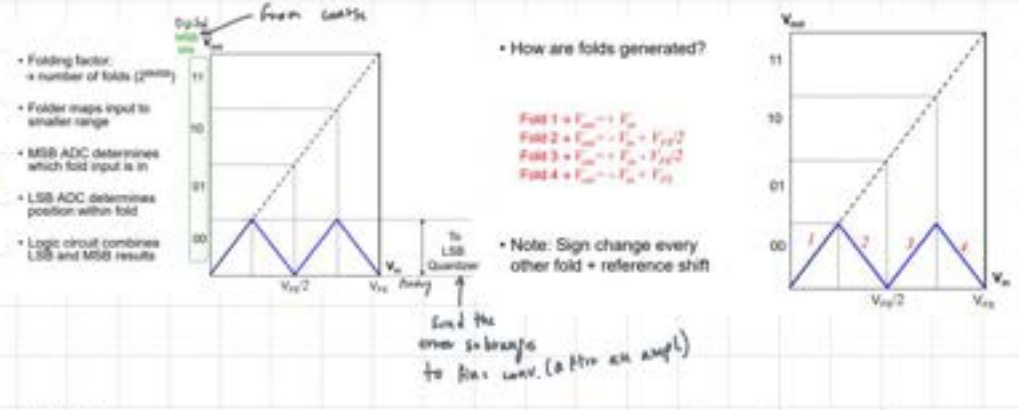


Components: . Flash ADC → for coarse conversion (MSB) and partial fine conversion (LSB)

. Folding circuit → to allow fine conversion

estimates the quantization error wrt the input signal

(Going via explore the error range (amplifying them) with less conv.

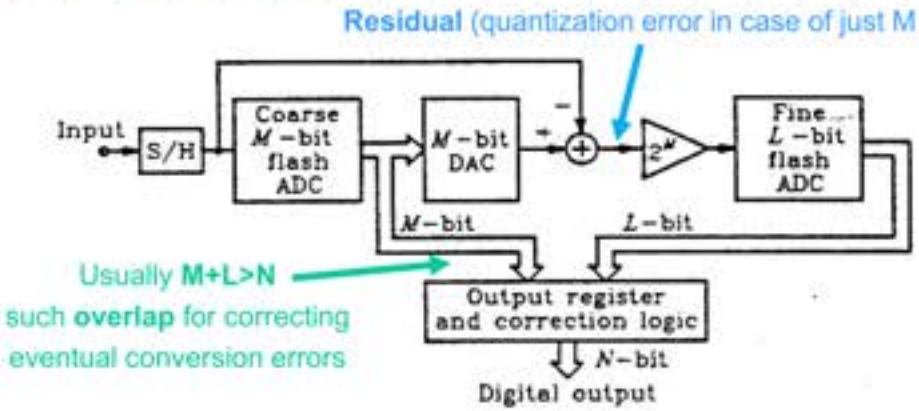


Pros: . Folding reduces the comparator number by a folding factor F (number of preamps stays the same)

Cons: . folding signals can suffer from distortion/non idealities on folding edges → use just zero-crossing

Advanced ADC: Half Flash ADC

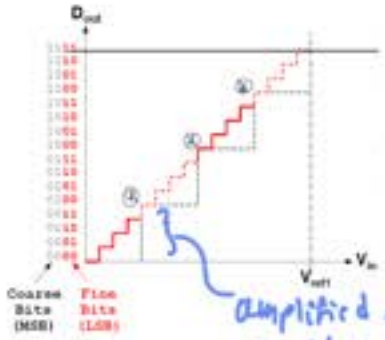
- Half-flash ADC



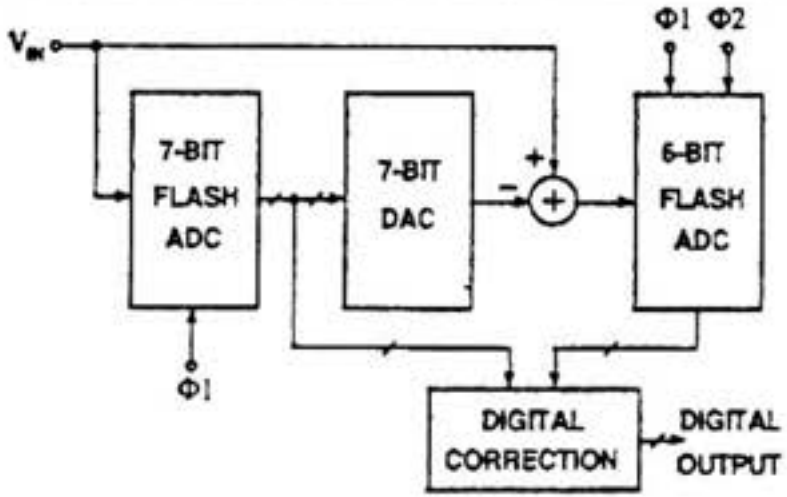
M coarse, L fine

Components:
- low bit flash converters → for conversion steps
- DAC → convert first round of MSB to an A signal to feed then the Fine ADC (accuracy of at least N total ADC)
- Amplifiers → to amplify the residual coming from M bit course ADC quantization
- sum and correction logic → for correction use M+L>N (overlapping bits correct any conversion edges)

Tot. bit



We amplify the error creating the ranges to quantize them with fine ADC)

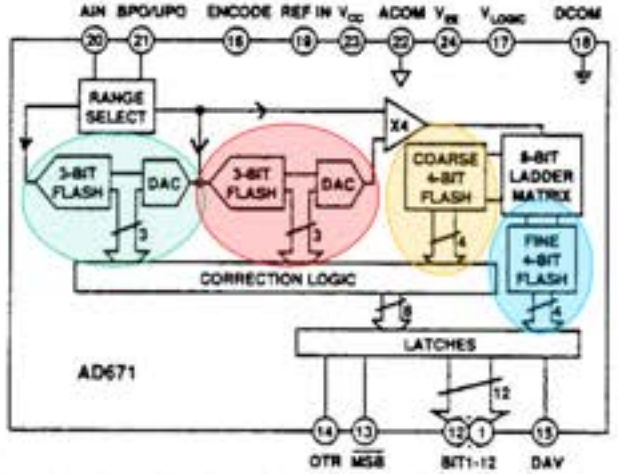


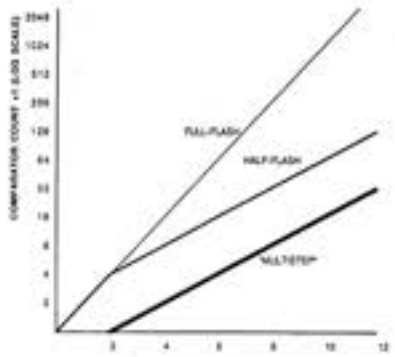
Pros:
- minimize area occupation and power consumption

Cons:
- slow conversion time

Advanced ADC: Multistep ADC

- Multistep ADC





Components: • same as previous flash solutions
↳ but not only made of 2 stages
↳ more stages in CASCADE

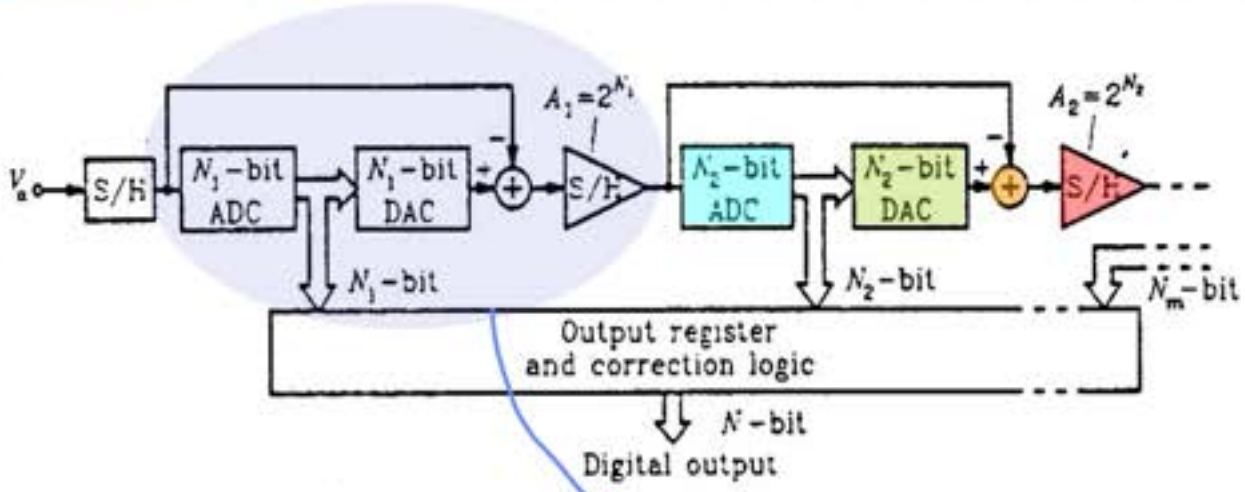
← Pros: • less comparators → (low area occupation)

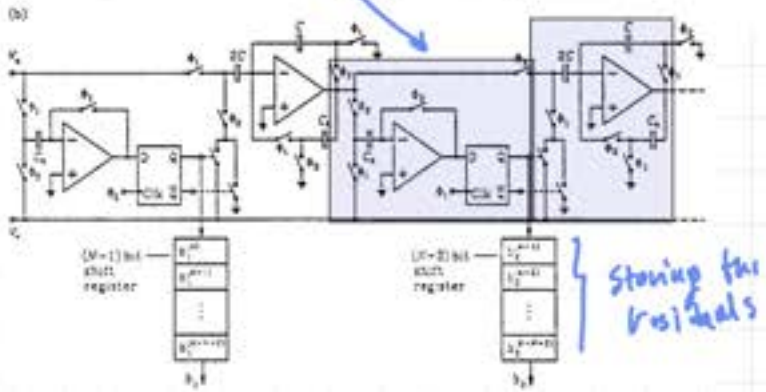
Cons: • conversion time ∝ # stages → slow!

better to use pipelined

Advanced ADC: Pipelined ADC

• Pipelined ADC





Components: • same of half flash/multistep stages

• + S&H → to put before every stage → we hold the residual value, so the stage can directly proceed with another conversion

parallel-pipelined processing

Pros: • fast conversion time

↳ wrt half-flash/multistep improves of a factor equal to # m stages of pipeline

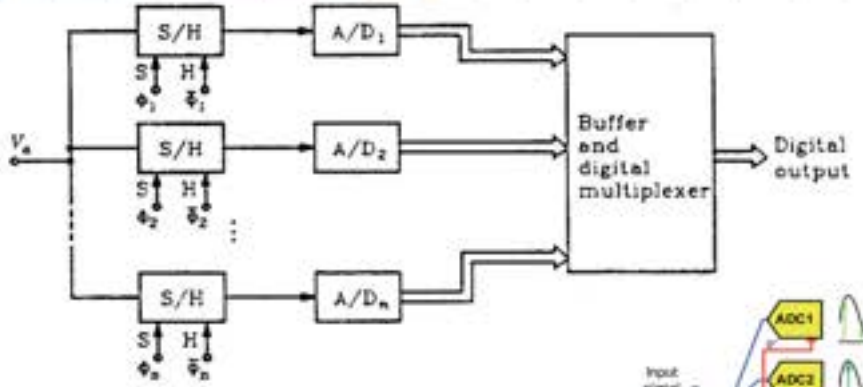
• low area occupation and power consumption

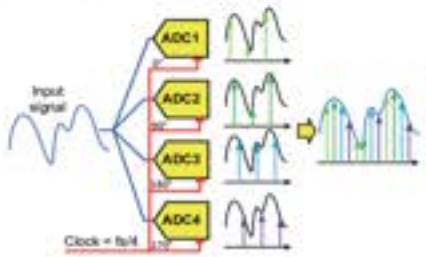
Cons: • compromises bw speed and accuracy

↳ m↑ conversion time↓ accuracy↓ (noise increases stage after stage)

Advanced ADC: Time-interleaved ADC

- Time-interleaved ADC





Components: • ADCs → put in parallel
channels operate in sequence • S&H → put before every ADC

Pros: • # stages faster wrt single channel
↳ achieve conversion speed not possible with single converters

Cons: • different channel behaviour, non regularity of sampling intervals
due to systematic errors bw channels
↓
create spurious freq. components